

**Problem 1:** Show timing diagrams verifying the latencies given in Figure 4.2 on page 224.

**Problem 2:** (The solution to this problem is based on material in section 3.9, which was not covered in class.) Show the timing of the following code fragment on the MIPS R4000 pipeline based on the pipeline stages given in Figure 3.56. Assume instructions in the RF stage stall (slip in MIPS parlance) only if there is any structural hazard in the floating point execution units or if there are any RAW hazards. (The issue rules in a MIPS R4000 processor are stricter than that. Those who are curious or need material to reinforce section 3.9 can follow [http://www.sgi.com/MIPS/products/r4400/UMan/R4000.book\\_1.html](http://www.sgi.com/MIPS/products/r4400/UMan/R4000.book_1.html), keeping in mind that actual R4000 issue rules should not be used in the solution. )

```
LD  F0, 0(R2)
NEG F0, F0           ! Negate F0. (F0 = -F0)
ADD F2, F0, F4
CGT F6, F8           ! Set FP cond to true if F6 > F8. (FP Compare.)
ADD F10, F12, F14
```