

Problem 1: A Verilog description of yet another population count module appears below.

```
module ya_pop(p,a);
  parameter N = 256;
  input [N-1:0] a;
  output      p;
  reg [8:0]    p;
  integer      i;

  always @( a ) begin
    p = 0;
    for ( i=0; i<N; i = i+1 ) p = p + a[i];
  end

endmodule
```

- (a) Sketch the synthesized hardware when N is 4.
- (b) Estimate the cost in terms of gates when N is 4 assuming that a ripple adder was inferred for the $+$ operator and that reasonable optimizations were made. For this problem assume that an XOR, and other basic gates have a cost of 1.
- (c) Making the same assumptions as in the previous part, determine the delay for arbitrary N and for $N=4$. In particular assume that optimizations were made to reduce cost but that the circuit was not re-organized to improve performance (see the next part). In your delay model use 2 for the delay of an XOR and 1 for other gates.

Problem 2: As the previous problem hinted, it is possible to obtain faster performance from the population counter (than is possible from a synthesis program that does not apply the technique described below). Faster performance can be obtained by using use several smaller population counters and adding their sums.

- (a) Briefly describe why this would result in faster performance.
- (b) Write a Verilog behavioral description of a 256-bit population count module which instantiates four 64-bit `ya_pop` modules.
- (c) Write a Verilog behavioral description of an N -bit population count module with parameters N and M , where N is a multiple of M . Unlike the module from the previous part, the module for this part should not instantiate any other modules. In procedural code it should determine the population in M parts and add them together. Solution to this problem may require Verilog's equivalent of arrays, called *memories*. See page 46 of the Verilog XL manual linked to the course's references page, <http://www.ece.lsu.edu/ee3755/ref.html>.