

EE 3755: Computer Organization

Syllabus

Where/When/Web

Room 1110 P.F. Taylor Hall

Monday Wednesday Friday 8:30–9:20 **Fall 2013**

<http://www.ece.lsu.edu/ee3755/>

Who

David M. Koppelman

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Tentative Office Hours: Monday–Friday: 14:00–15:00.

Prerequisites

EE 2740 (Digital Logic)

Topics

Introduction to Hardware Description Using Verilog

Computer Arithmetic

Integer $+$, $-$, \times , \div Hardware

IEEE 754 Floating-Point Representations

Floating-Point Addition Algorithm and Hardware

Floating-Point Multiplication and Division Algorithms

Organization and Programming of a RISC Processor (MIPS)

Registers, Memory, and Instruction Execution

Assembly Language Programming

Basic Processor Implementation Techniques

Datapath Elements (Registers, memory ports, etc.)

Basic Processor Control Techniques

Texts

“Computer organization & design,” David A. Patterson & John L. Hennessy.

Optional Verilog Texts: Brown & Vranesic, “Fundamentals of Digital Logic with Verilog Design” (The text used in EE 2720, 2730, and 2740.); Ciletti, “Advanced Digital Design with the Verilog HDL” (Only a small portion used in 3755.)

Grading

40% Midterm Exam • 40% Final Exam • 20% Homework

Final exam weight may be increased for students who show significant improvement on the final exam.

Late-homework penalty: 10% per day late deducted. Missed-midterm-exam policy: at instructor’s discretion either a makeup exam, use final exam grade for midterm grade (*i.e.*, 80% final exam weight), or use zero for midterm grade. Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class.

