

For this assignment read Chapter 4 of Patterson & Hennessy, *Computer Organization 4th Edition*, up to and including Section 4.4. These sections describe a MIPS implementation which is most similar to our functional simulation model,

http://www.ece.lsu.edu/ee3755/2012f/mips_fs.v.html, however for this assignment compare the Section 4.1-4.4 implementation to our Multi-cycle Implementation 1,

http://www.ece.lsu.edu/ee3755/2012f/mips_hc.v.html.

Problem 1: Consider how the instructions `beq` and `bne` are implemented in the two designs.

(a) How does the implementation described in Section 4.3 detect whether the `beq` and `bne` instructions are taken?

(b) How is that different than the method used by the Multicycle MIPS Implementation 1 presented in class?

Problem 2: The Section 4.4 implementation illustrated in Figure 4.15 has a `RegWrite` signal.

(a) What does that signal do?

(b) The multi-cycle implementation covered in class lacks such a signal. Explain how it gets by without it.

Problem 3: The implementation described in Section 4.4 is a *single-cycle* implementation and is most similar to our functional simulation model. The multi-cycle implementation that we are now (16 November 2012) covering has cost and performance advantages.

(Don't forget: The pipelined implementation, which will be covered in EE 4720, has even greater performance benefits. The multi-cycle implementation is both a pedagogical bridge to the pipelined implementation, but it also is a suitable implementation technique for instruction sets more complex [and not in a good way] than MIPS. Many mid 20th century computers used multi-cycle implementations, by the 80s pipelined implementations replaced them.)

(a) Consider the cost of the implementation illustrated in Figure 4.17 as compared to our multi-cycle implementation. Indicate the major units of hardware illustrated in 4.17 that are not needed in the multi-cycle implementation. (Those 4.17 units are not needed because a single unit in the multi-cycle implementation is used for different purposes over different clock cycles.)