EE 3755 **Homework 3** **Due: Not collected**

The following problems cover material that will be on the midterm. Solution to some of these may be presented in the review, especially if someone requests some of these problems for the review. This assignment will not be collected.

Problem 1: Write a Verilog description of a signed adder that adds a 30-bit signed quantity to a 10-bit signed quantity, producing a 31-bit result. The Verilog description can use the add operator but cannot use integers or reals. Other than declarations, a correct solution includes one line.

Problem 2: Show the longhand steps for dividing 101010 by 111. Identify the quotient and remainder.

Problem 3: In class both levels of a two-level CLA were themselves CLA.

(*a*) Write a Verilog description of a 40-bit two-level CLA in which both levels are CLAs. The design should use 10-bit CLAs for the first level; assume they are already designed. (The description should instantiate four 10-bit CLAs. Make up a name for them.)

(*b*) In gate delays, how fast is the two-level adder.

(*c*) Suppose the 10-bit CLAs were really ripple adders. How much cheaper and how much slower would the 40-bit adder be?

Problem 4: Modify module `streamlined_mult` so that the multiplicand is a signed number (but keeping the multiplier an unsigned number). Take advantage of the existing structure of `streamlined_mult`, don't just make it look like `streamlined_signed_mult`.

Problem 5: Show a radix-8 Booth table (in the same format as the radix-4 and -2 Booth tables in Set 7).

Problem 6: Remember the last time you bought lunch and it did not cost an even dollar amount. If you can't assume it cost $5.12.

(*a*) Convert the cost to binary. Plain, old binary, not IEEE 754. From the class account issue command "dtob 5.12" to see the answer.

(*b*) Convert the cost of lunch to binary scientific notation.

(*c*) Convert the cost of lunch to an IEEE 754 single. From the class account issue command "fp 5.12" to see the answer.