

EE 3755

Spring 2003

Homework #3

Not to be returned; (it will
not be graded).

(1)

HW#3

Please do the following problems:

1 The following computer is defined

IR[2:3]	00	01	11	10
00	ADD	CLC	X	JPL
01	OR	SEC	MULT	JEQ
11	AND	ROR	MVF	JMP
10	MVT	RTS	NOT	JSR

Mnemonic	Meaning
ADD	$AC \leftarrow AC + \text{memory}; cin = 0$
OR	$AC \leftarrow AC \vee \text{memory}$
AND	$AC \leftarrow AC \wedge \text{memory}$
MVT	$AC \leftarrow \text{memory}$
CLC	clear cff
SEC	set cff
ROR	
RTS	return from subroutine
MVF	$\text{memory} \leftarrow AC$
NOT	$AC \leftarrow \overline{AC}$
JPL	jump if nff=0
JEQ	jump if zff=1
JMP	unconditional jump
JSR	unconditional jump to subroutine
MULT	$R, AC \leftarrow AC \times \text{memory}$

0	3	4	15
opcode	address field		

Instruction format
(we only have direct addressing mode)

→ continues on next page.

(2)

Note 1:

0	3	4	11	12	15
0111	00000000	Distance			

Format of ROR. Distance
is 4-bit unsigned number

* Use counter
to count
distance

Note 2:

MULT is the instruction for multiplication. The data are considered to be signed numbers (2^2 's compl. system used for representing signed numbers). The product should be placed in R, AC (upper part in R; lower part in AC). Simple Booth (two bit examination) should be used.

Note 3:

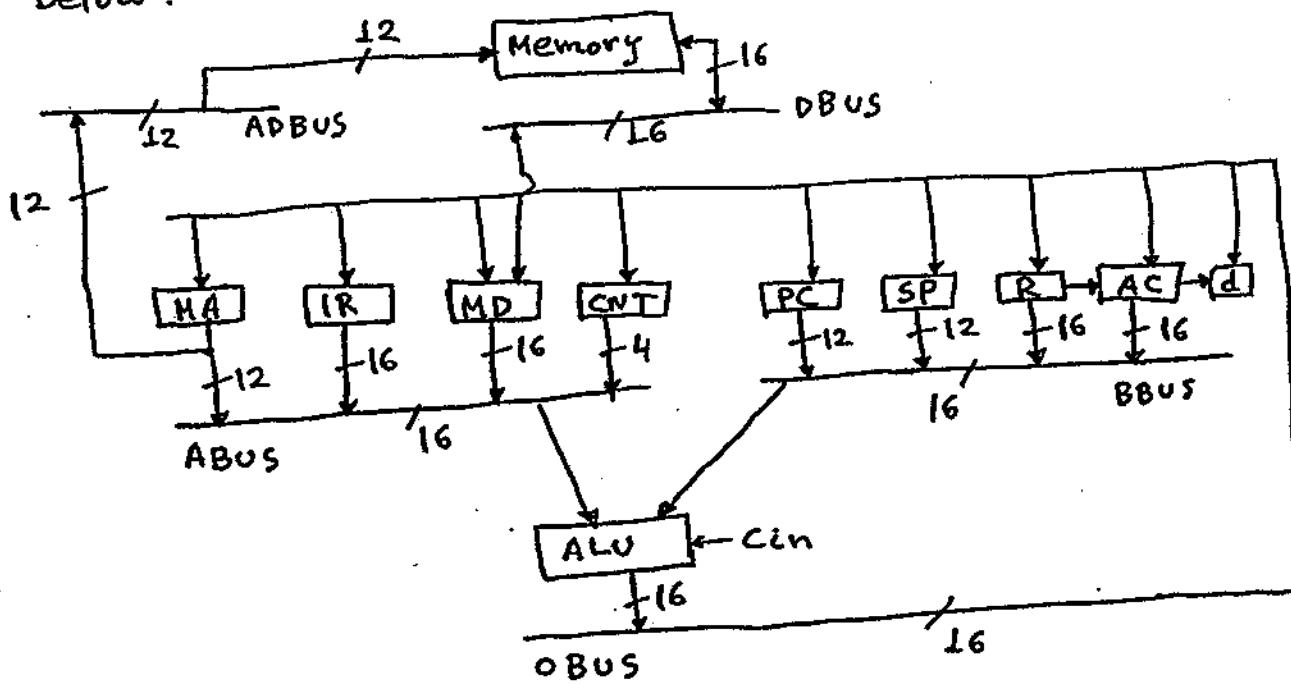
There are four flags in our computer. The carry flag cff, the negative flag nff, the zero flag zff and the overflow flag vff. These flags are affected in a similar way as those of the ~~first~~ computer (ie: ADD affects all flags, the logic instructions OR, AND, NOT affect nff and zff only).

"first example computer"

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(3)

The block diagram of the computer is given below:



CNT, is a 4-bit counting register while 'd' is a single flip-flop to be used as the dummy field for the Booth multiplication.

You Are Asked to write in AHPL the control sequence, for the computer defined above beginning with the instruction fetch up through the execution of all instructions.

(4)

- [2] Write in AHPL step 61 of the "First example computer".

See page 4 of Handout entitled "First example computer: Part ⑤" for step 61.

- [3] Rewrite all the steps (steps 0 through 101) of the "first example computer" showing explicit BUS-connections; Step 22, for example, shows explicit ~~step~~ BUS-connections.

