Fall 2011

EE 2720: Digital Logic I

Instructor:

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245 Electrical Engineering Building
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Text:

"Fundamentals of Digital Logic with Verilog Design," Second edition, Stephen Brown and Zvonko Vranesic, McGraw-Hill, 2008.

Catalog Description:

Digital Logic I (2). Prereq: MATH 1550. Boolean algebra; logic gates; minimization methods; analysis and syntheses of combinational logic networks; design examples.

Grading:

5-6 Homeworks	20%
2 Tests	50%
Final	30%

Test Policy:

If a student misses any one of tests 1 or 2 for a medical reason then the student should provide the instructor with a doctor's statement stating that the student was sick on the day of the test. In this case, a make-up test will NOT be given but instead the remaining test will count for 35%, the homework for 20%, and the final for 45%.

Homework Policy:

Late homework will not be accepted.