

EE 2720, Fall 05

HW #7

Friendly note: Due date for HW#7
will be posted on web + announced
in class

Your friend
Alex!!

Homework # 7

Problem 1: Design the prime number detector of handout #13 (see page 5 of handout #13) using:

- A decoder with uncomplemented outputs and one 7-input OR gate
- A decoder with complemented outputs and one 7-input NAND gate.
- A decoder with complemented outputs and one 9-input AND gate.
- A decoder with uncomplemented outputs and one 9-input NOR gate.
- A 16-to-1 multiplexer and nothing else.
- An 8-to-1 multiplexer and nothing else.
- Which one of the designs between these in parts (e) and (f) is better? Why?

Problem 2: Using a decoder with uncomplemented outputs and a 12-input OR gate, implement the logic function $F = (a + b + c) \cdot (b + c + d) \cdot (a + c + d)$.

Problem 3: Using a decoder with complemented outputs and a 4-input AND gate, implement the logic function of problem 2.

Problem 4: Using a decoder with uncomplemented outputs and a 6-input OR gate, implement the logic function $F = a \cdot b \cdot c + b \cdot c \cdot d + a \cdot d$.

HW# 7 cont.

Problem 5: Using a decoder with complemented outputs and a 10-input AND gate, implement the logic function of problem 4.

Problem 6: Using Karnaugh maps, derive simplified product-of-sums expressions for the outputs a, b, c, d, e, f, g of the seven-segment decoder presented in handout # 17; (Look on page 11 of handout # 17).

Problem 7: Using four 3-to-8 decoders and one 2-to-4 decoder, construct a 5-to-32 decoder. Each one of the 3-to-8 decoders as well as the 2-to-4 decoder must have an active high enable input named E. Your design must be a two-level design here.

Problem 8: Using four 2-to-4 decoders each with one active high enable input named EN1 and two active low enable inputs named EN2 and EN3, plus one inverter, construct a 4-to-16 decoder.

Problem 9: Using two 16-to-4 priority encoders each with an enable input named EI, a group select output named GS as well as an enable output named E0 plus few OR gates, construct a 32-to-5 priority encoder; (look in handout # 19 for EI, GS, E0).

HW #7 cont.

Problem 10: Using four 8-to-1 multiplexers and one 4-to-1 multiplexer, design a 32-to-1 multiplexer. This is going to be a two-level design similar to examples 1, 2 of handout # 20.

Problem 11: Using four 4-to-1 multiplexers, one inverter and one 4-input OR gate, design a 16-to-1 multiplexer. Each of the four 4-to-1 multiplexers must have one active high enable input named EN1 and two active low enable inputs named EN2 and EN3.

Problem 12: Using a 4x3 PLA with 6 product terms, implement the following functions:

$$X = \sum A, B, C, D (1, 7)$$

$$Y = \prod A, B, C, D (0, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 15)$$

$$Z = A \cdot B'$$

Note: 4x3 PLA means a PLA with 4 inputs and 3 outputs. When I say 6 product terms, I mean that the PLA contains 6 AND gates.

Problem 13: Using a 4x3 PLA with 6 product terms, implement the following functions:

$$X = A' \cdot B' \cdot C' \cdot D' + A \cdot B \cdot C \cdot D$$

$$Y = \prod A, B, C, D (2, 3, 4, 6, 7, 8, 10, 11, 12, 13, 14, 15)$$

$$Z = \sum A, B, C, D (5, 9, 12)$$

Note: From problem 12, you should know what 4x3 PLA means and what 6 product terms means.