EE 2720, Spr 05
Solutions of Homework #5

Problem 1: I first provide a logic circuit showing an AND-OR realization of F. This is shown in fig. 1 below:

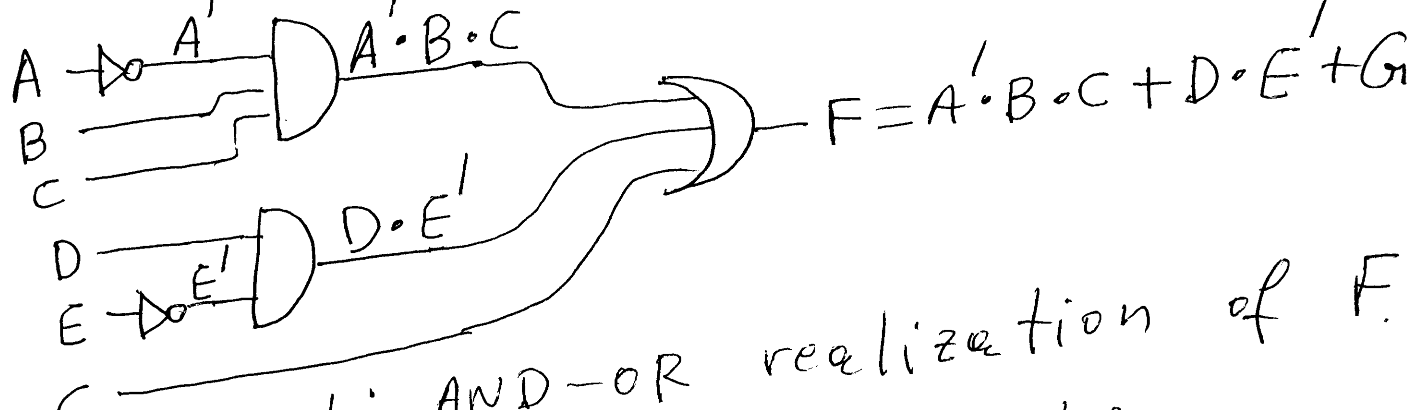

Fig. 1: AND-OR realization of F.

From the above fig. 1 we get:

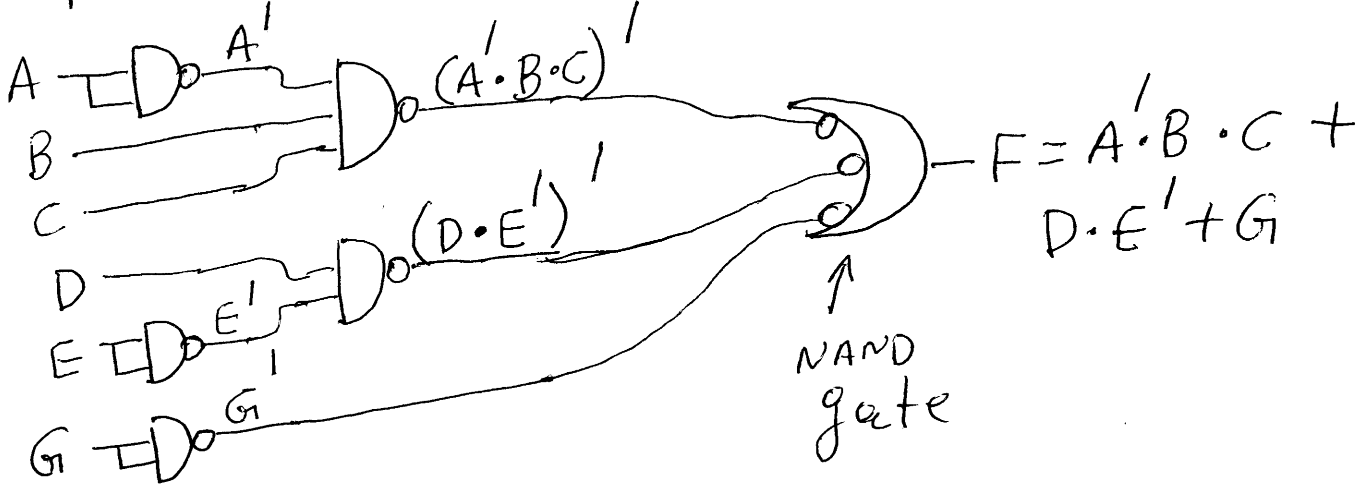

Fig. 2: Realization of F using only NAND gates.

Problem 2: I first provide a logic circuit showing an OR-AND realization of F. This is shown in figure 1 below:

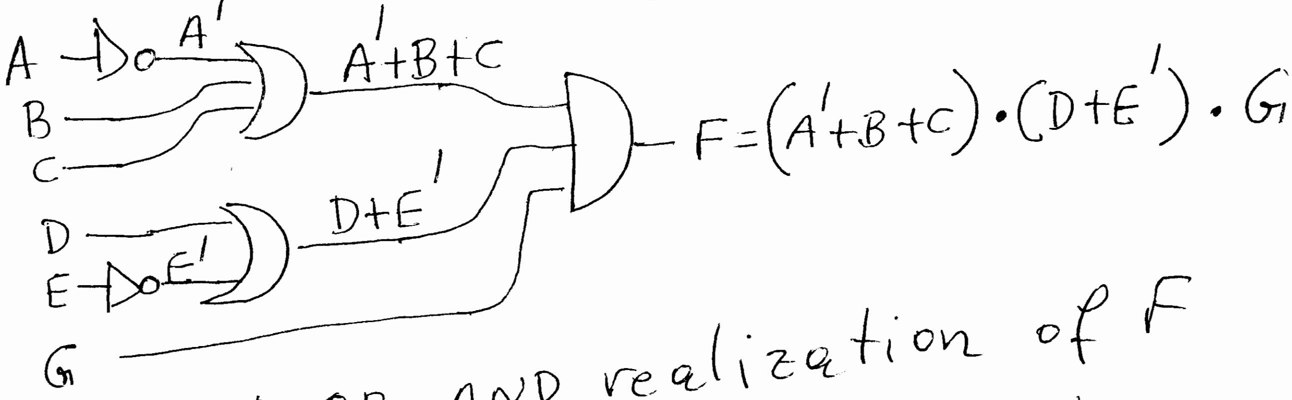

Fig. 1: OR-AND realization of F

From the above fig. 1 we get:

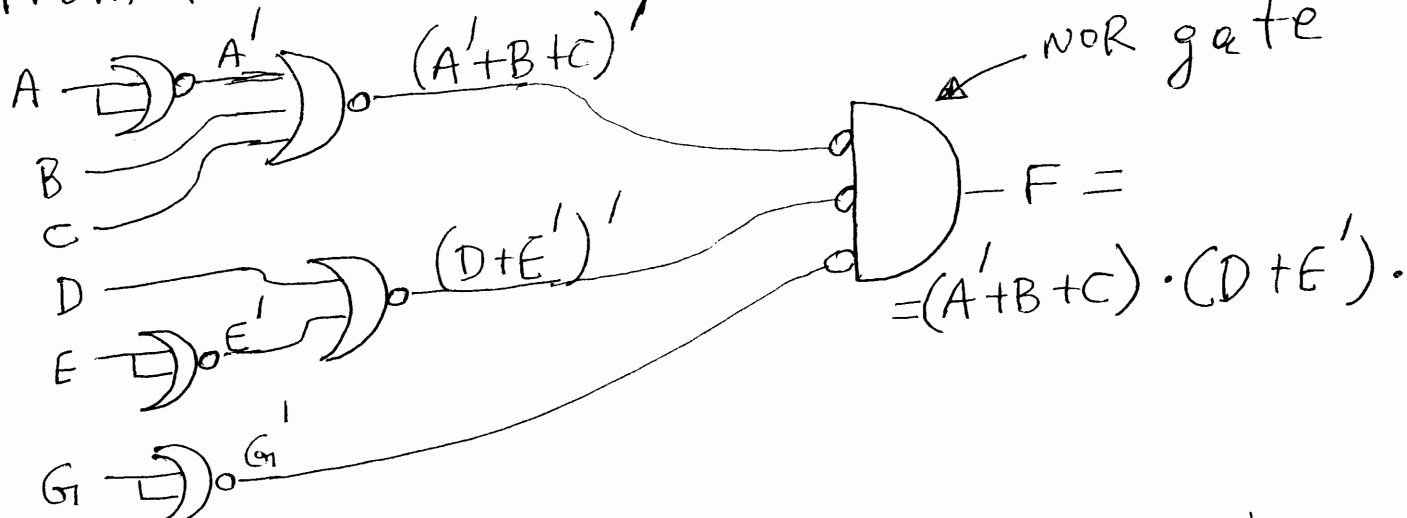

Fig. 2: Realization of F using only NOR gates

Problem 3:

$F = A'\cdot B\cdot C + D\cdot E' + G$ (1)

$= [(A'\cdot B\cdot C + D\cdot E' + G)']'$

$= [(A'\cdot B\cdot C)'\cdot(D\cdot E')'\cdot G']'$ (2)

$[(A+B'+C')\cdot(D'+E)\cdot G']'$ (3)

$= (A+B'+C')' + (D'+E)' + G$ (4)

The above equations (1), (2), (3), (4) will give us realizations # 1, 2, 3, 4 respectively shown in figures 1, 2, 3, 4 respectively.

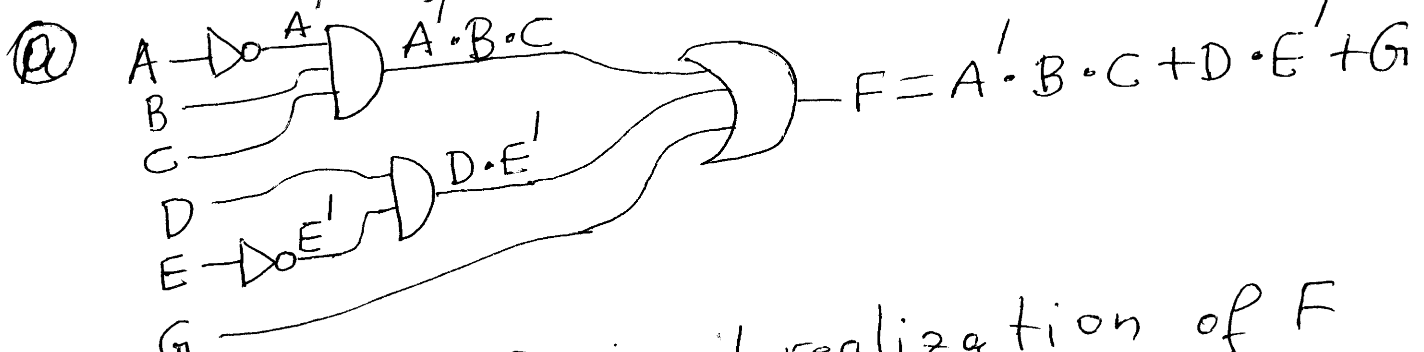

Fig.1 AND-OR circuit realization of F

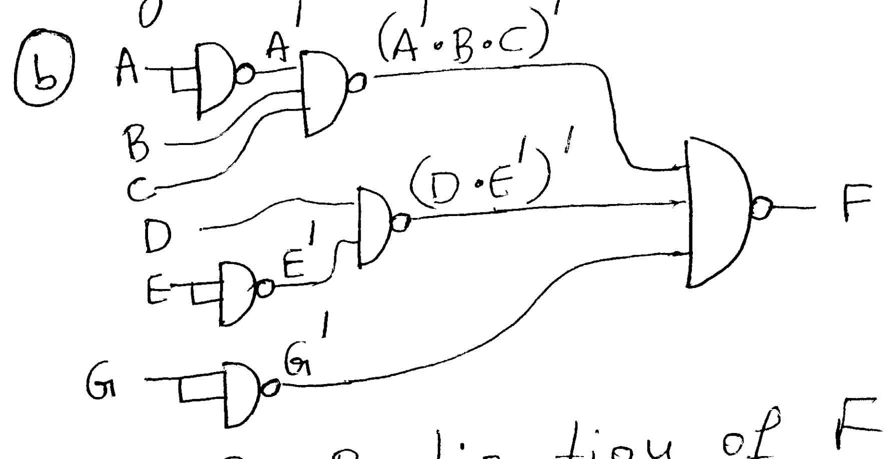

Fig.2: Realization of F using only NAND gates

Problem 3 cont.

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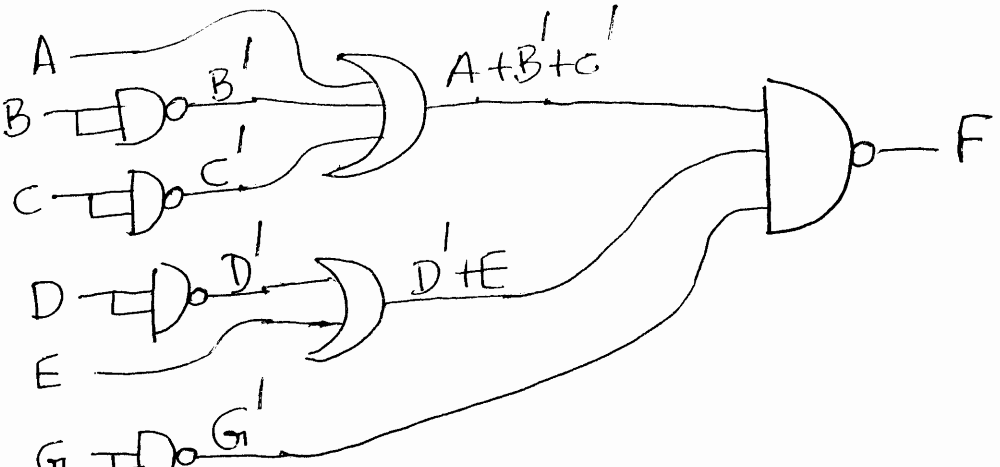

Fig. 3: Realization of F using only OR and NAND gates.

ⓓ

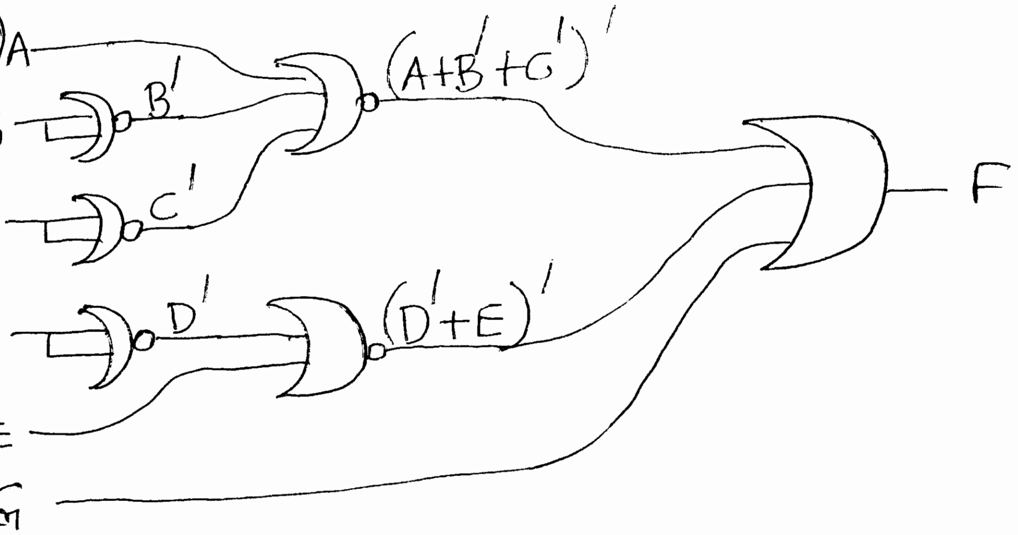

Fig. 4: Realization of F using only NOR and OR gates.

(e)

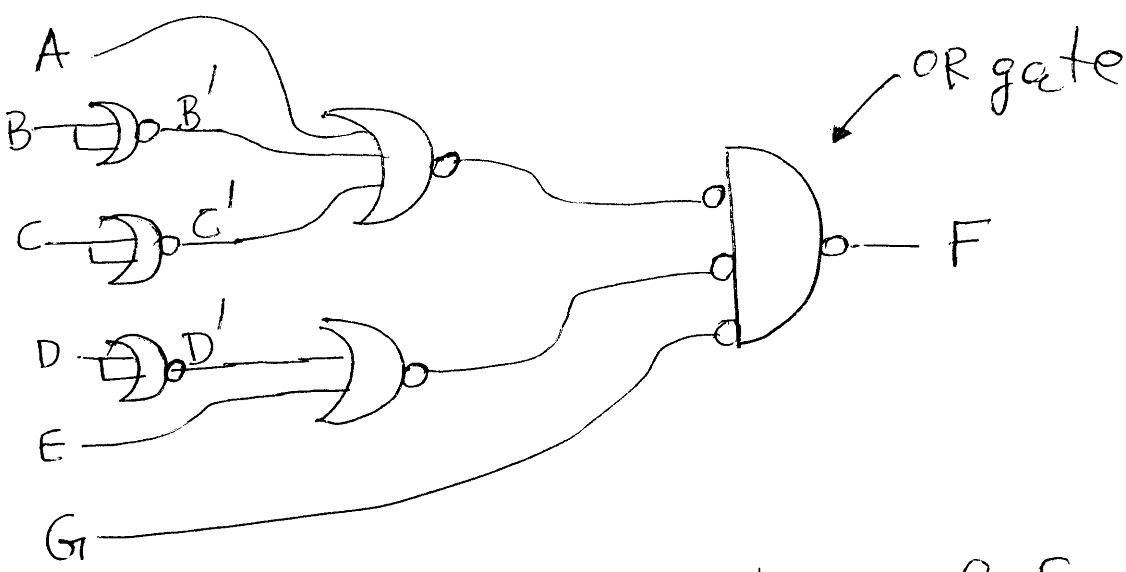

Fig. 5: Another realization of F using only NOR and OR gates.

(f)

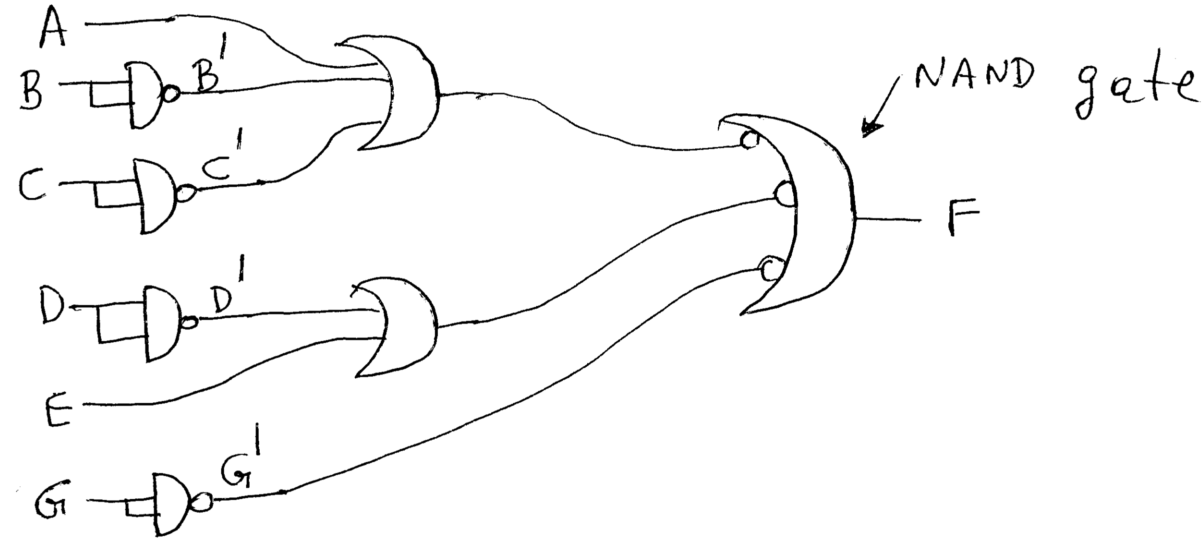

Fig. 6: Another realization of F using only NAND and OR gates.

Problem 4:

$$F = (A'+B+C)\cdot(D+E')\cdot G \quad (1)$$

$$= \left[\left[(A'+B+C)\cdot(D+E')\cdot G\right]'\right]'$$

$$= \left[(A'+B+C)'+(D+E')'+G'\right]' \quad (2)$$

$$= (A\cdot B'\cdot C'+D'\cdot E+G')' \quad (3)$$

$$= (A\cdot B'\cdot C')'\cdot(D'\cdot E)'\cdot G \quad (4)$$

Equations (1), (2), (3), (4) above will give us realizations # 1, 2, 3, 4 respectively, shown in figures 1, 2, 3, 4 respectively.

ⓐ

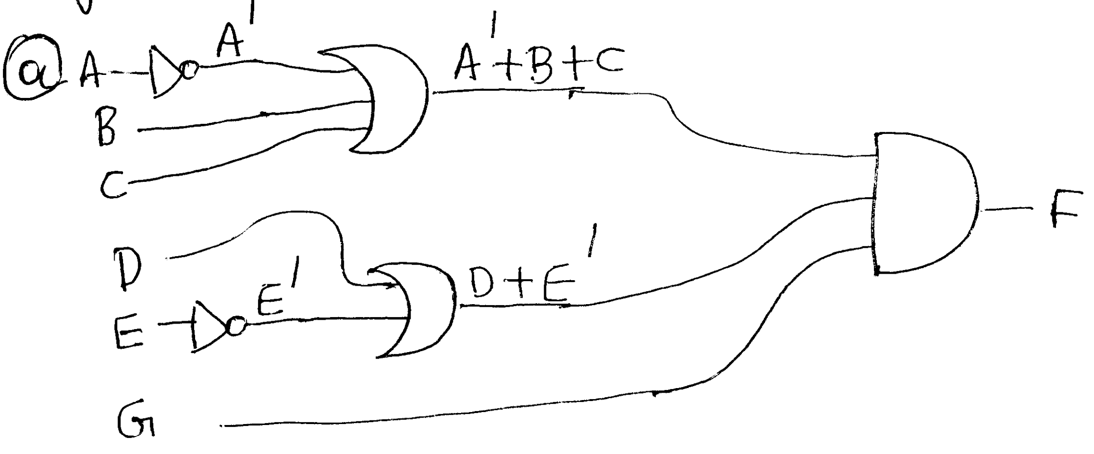

Fig. 1: OR-AND realization of F

Problem 4 cont.

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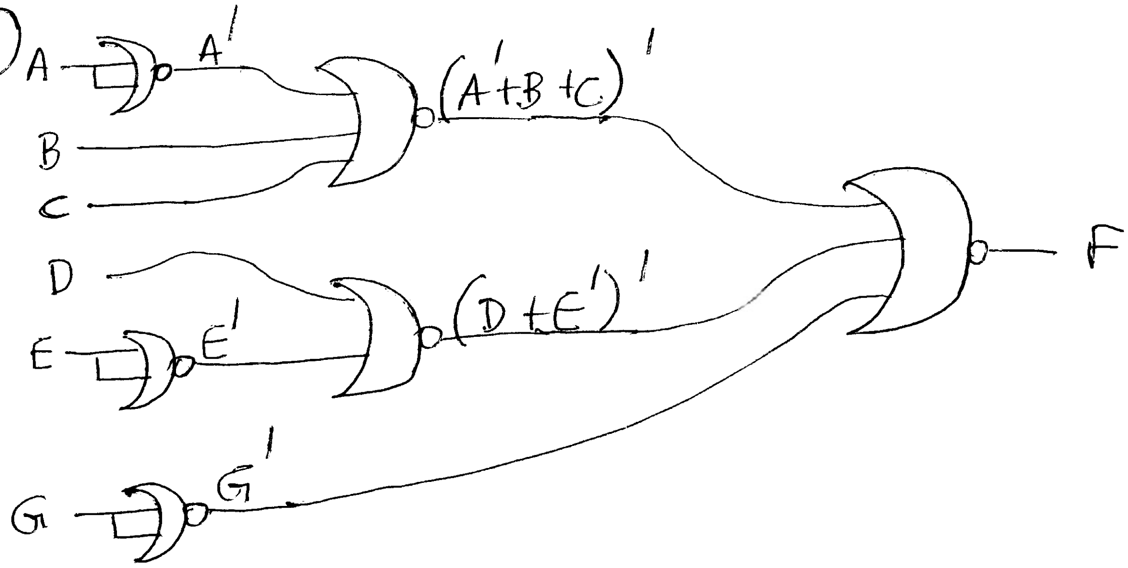

Fig. 2: Realization of F using only NOR gates.

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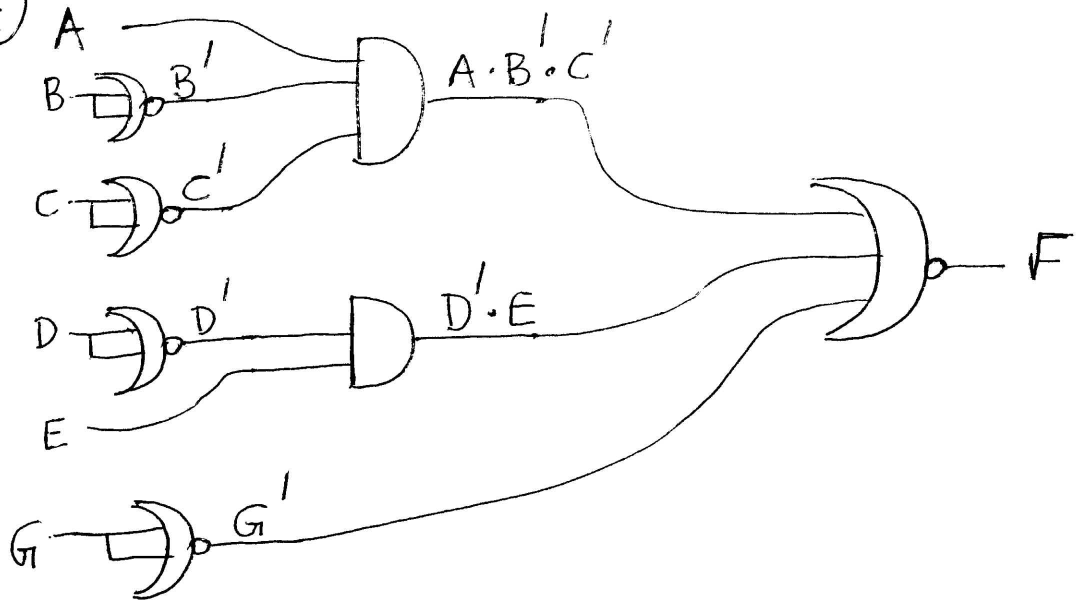

Fig. 3: Realization of F using only AND and NOR gates

Problem 4 cont.

(d)

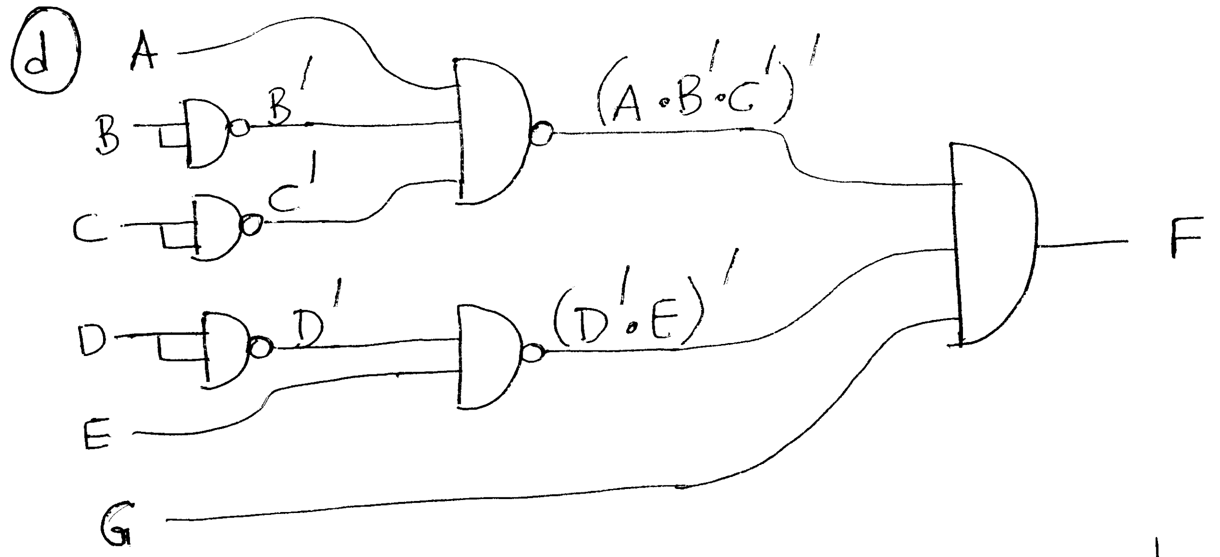

Fig. 4: Realization of F using only NAND and AND gates.

(e)

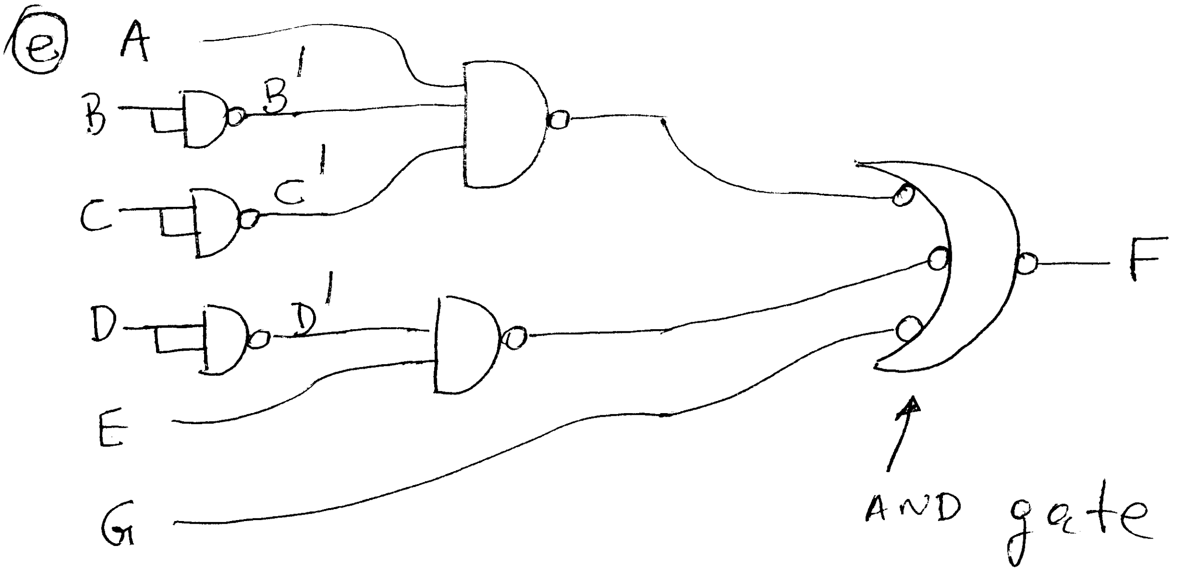

Fig. 5: Another realization of F using only NAND and AND gates.

Problem 4 cont.

(f)

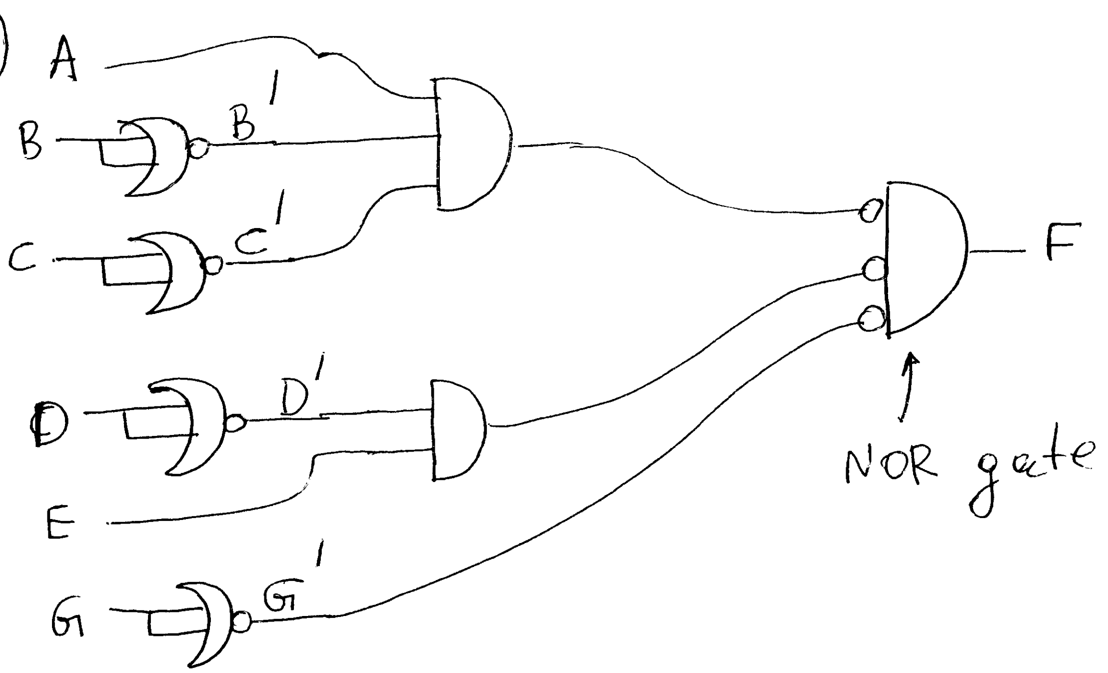

Fig. 6: Another realization of F using only AND and NOR gates.

Problem 5:

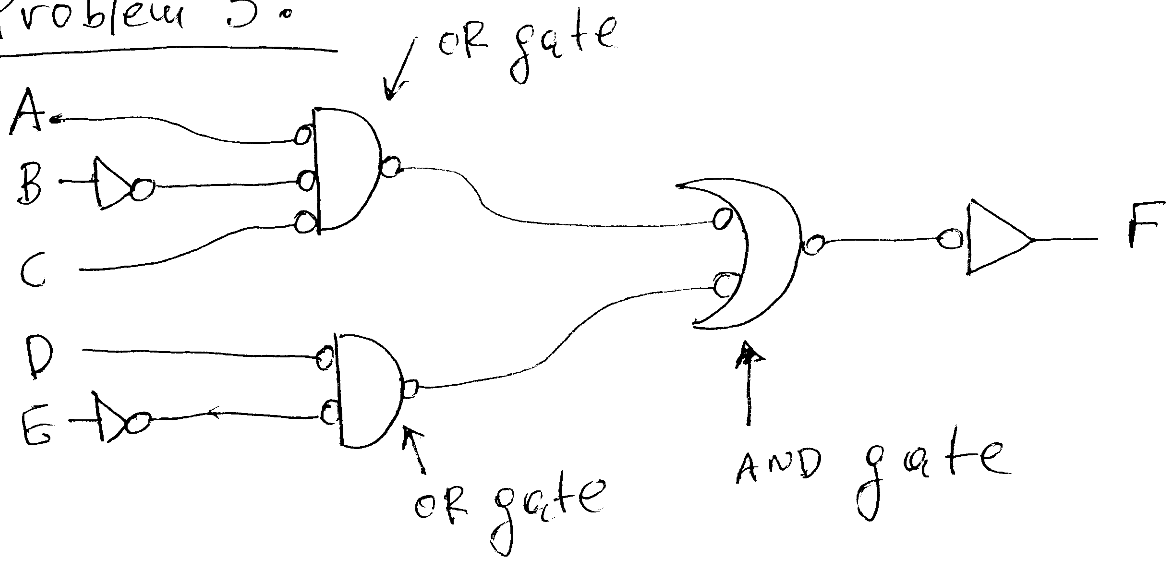

Fig 1a: The equivalent OR-AND logic circuit for F.

Problem 6:

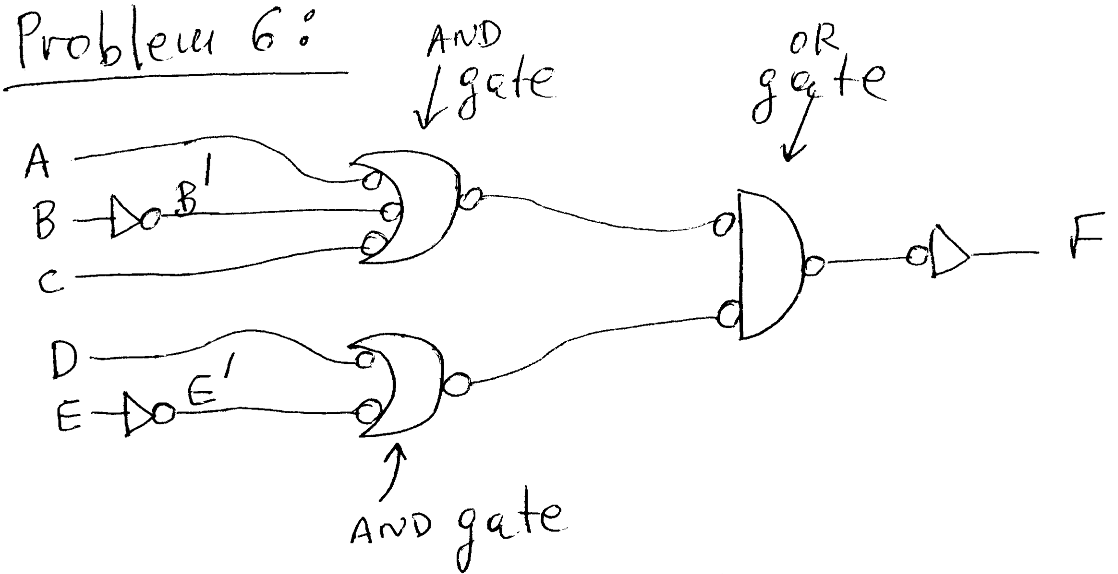

Fig 2a: The equivalent AND-OR logic circuit for F.

Problem 7:

ⓐ Proof of (5) or proof of $X \oplus 0 = X$

- Case $X=0$: $0 \oplus 0 = 0$
- Case $X=1$: $1 \oplus 0 = 1$

ⓑ Proof of (6) or proof of $X \oplus 1 = X'$

- Case $X=0$: $0 \oplus 1 = 1$
- Case $X=1$: $1 \oplus 1 = 0$

ⓒ Proof of (7) or proof of $X \oplus X = 0$

- Case $X=0$: $0 \oplus 0 = 0$
- Case $X=1$: $1 \oplus 1 = 0$

ⓓ Proof of (8) or proof of $X \oplus X' = 1$

- Case $X=0$: $0 \oplus 1 = 1$
- Case $X=1$: $1 \oplus 0 = 1$

Problem 7 cont.

Note: Eqs. (5), (6), (7), (8) can also be proved by using eq. (1) on top of page 5 of handout # 11.

ⓔ Proof of (11) or proof of

$$X\cdot(Y\oplus Z) = X\cdot Y\oplus X\cdot Z$$

The right handside of (11) is

$$X\cdot Y\oplus X\cdot Z = X\cdot Y\cdot(X\cdot Z)' + (X\cdot Y)'\cdot X\cdot Z =$$

$$= X\cdot Y\cdot(X'+Z') + (X'+Y')\cdot X\cdot Z =$$

$$= X\cdot \cancelto{0}{Y\cdot X'} + X\cdot Y\cdot Z' + \cancelto{0}{X'\cdot X}\cdot Z + Y'\cdot X\cdot Z =$$

$$= X\cdot Y\cdot Z' + X\cdot Y'\cdot Z = X\cdot(Y\cdot Z' + Y'\cdot Z)$$

$= X\cdot(Y\oplus Z)$. But we have now reached the left side of (11) so the proof is completed.