

EE 2720, Fall 05
HW# 5 solutions

Problem 1: I first provide a logic circuit showing an AND-OR realization of F. This is shown in figure 1 below:

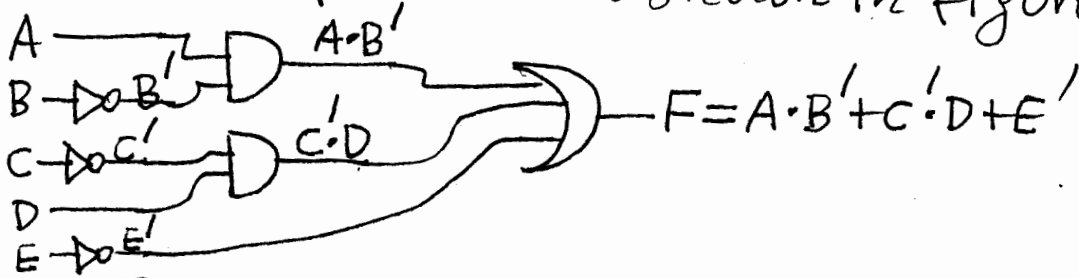


Figure 1: AND-OR realization of F

From the above fig. 1 we get:

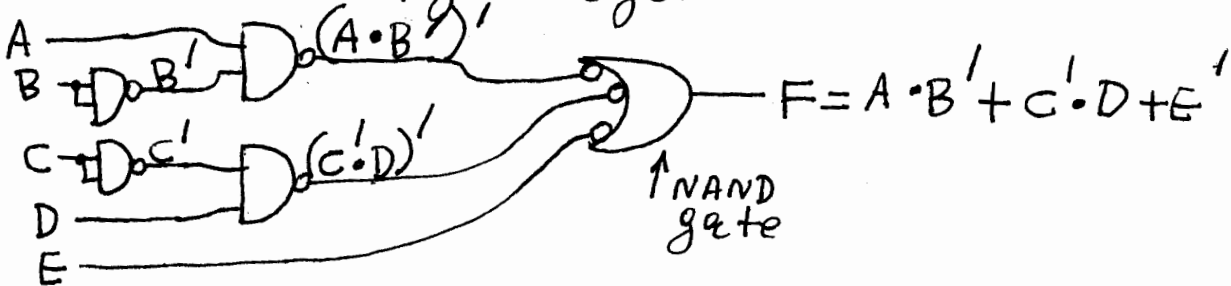


Fig. 2: Realization of F using only NAND gates.

Problem 2: I first provide a logic circuit showing an OR-AND realization of F. This is shown in figure 1 below:

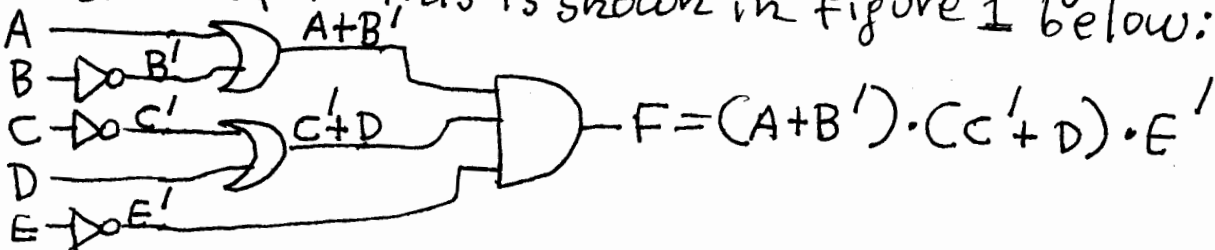


Figure 1: OR-AND realization of F

From the above fig. 1 we get:

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Problem 2 cont:

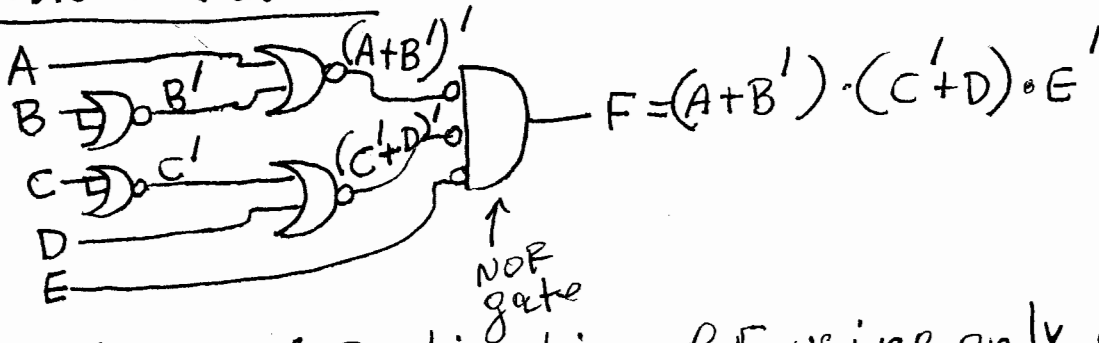


Figure 2: Realization of F using only NOR gates.

Problem 3:

$$\begin{aligned}
 F &= A \cdot B' + C' \cdot D + E' \quad (1) \\
 &= [(A \cdot B' + C' \cdot D + E')] \quad (1) \\
 &= [(A \cdot B')' \cdot (C' \cdot D)' \cdot E] \quad (2) \\
 &= [(A' + B) \cdot (C + D') \cdot E] \quad (3) \\
 &= (A' + B)' + (C + D')' + E' \quad (4)
 \end{aligned}$$

The above equations (1), (2), (3), (4) will give us realizations #1, 2, 3, 4 respectively shown in figures 1, 2, 3, 4 respectively.

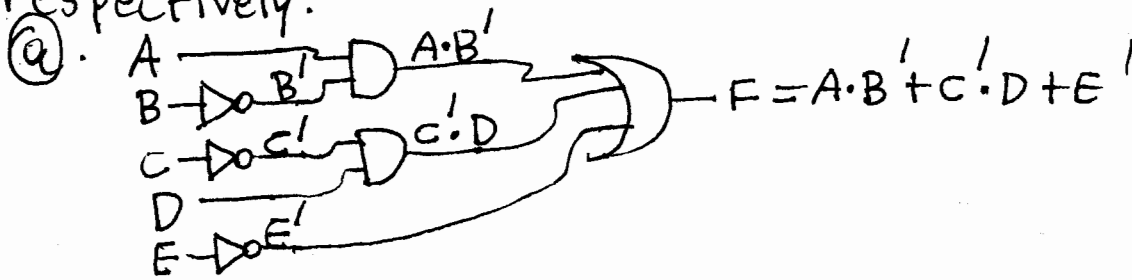


Figure 1: AND-OR circuit realization of F .

Problem 3 cont:

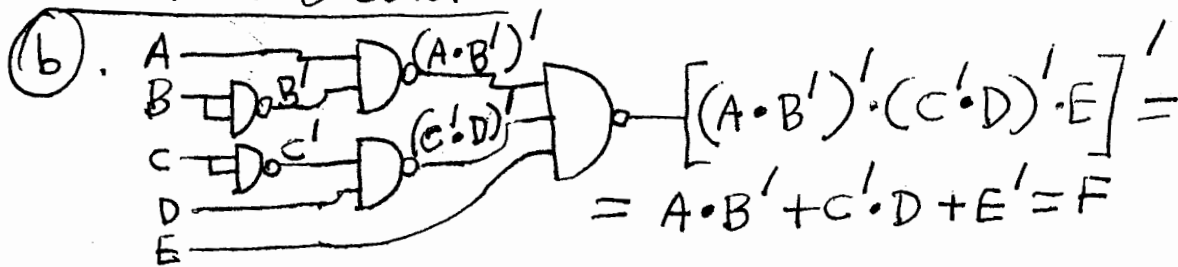


Figure 2: Realization of F using only NAND gates.

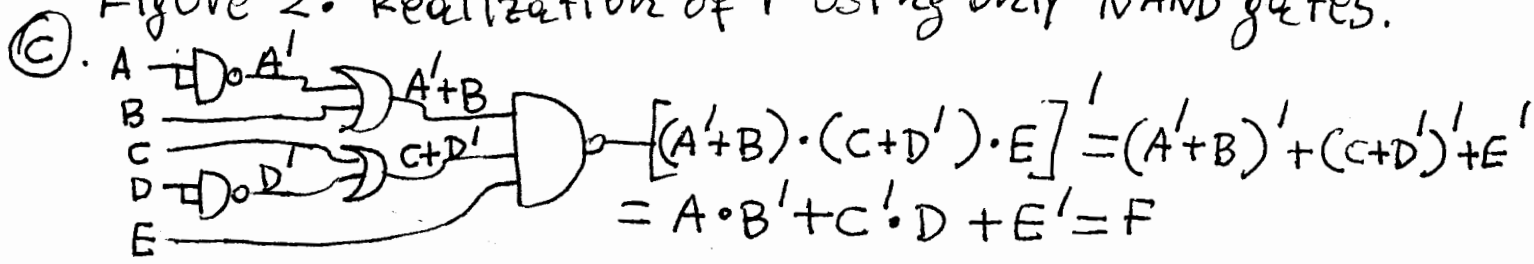


Figure 3: Realization of F using only OR and NAND gates

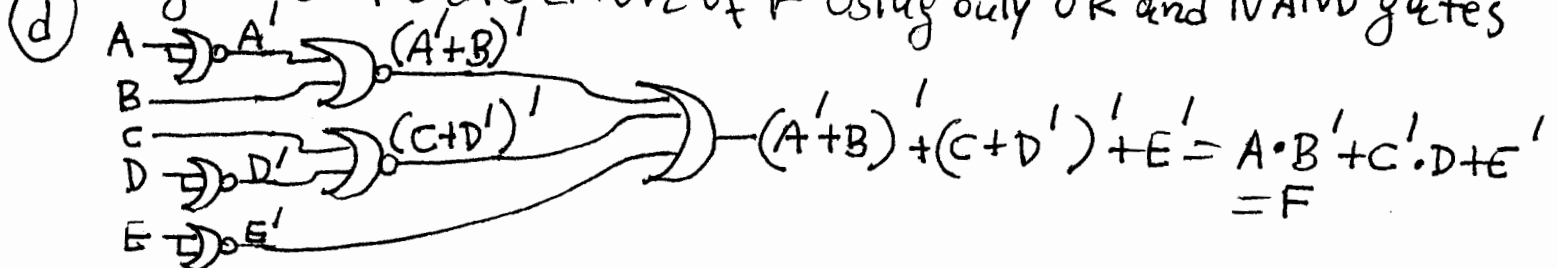


Figure 4: Realization of F using only NOR and OR gates.

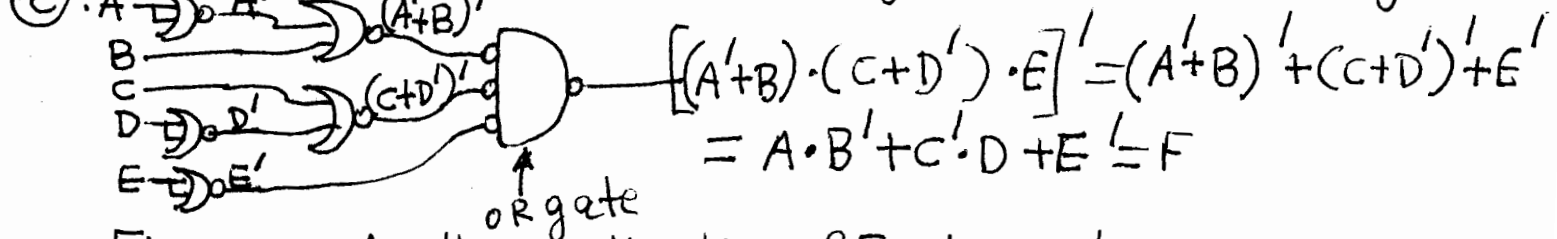


Figure 5: Another realization of F using only NOR and OR gates.

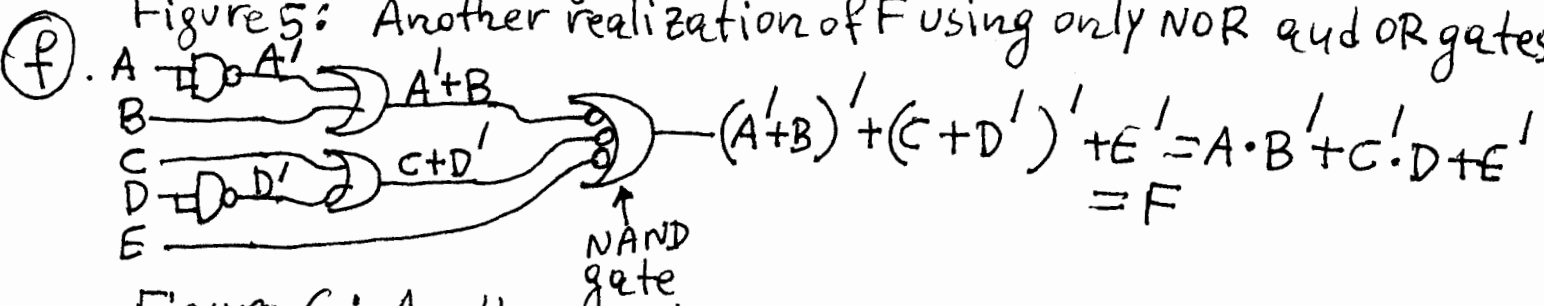


Figure 6: Another realization of F using only OR and NAND gates.

Problem 4:

$$\begin{aligned}
 F &= (A+B') \cdot (C'+D) \cdot E' \quad (1) \\
 &= \left[\left[(A+B') \cdot (C'+D) \cdot E' \right]' \right]' \\
 &= \left[(A+B')' + (C'+D)' + E \right]' \quad (2) \\
 &= (A' \cdot B + C \cdot D' + E)' \quad (3) \\
 &= (A' \cdot B)' \cdot (C \cdot D')' \cdot E' \quad (4)
 \end{aligned}$$

Equations (1), (2), (3), (4) above will give us realizations #1, 2, 3, 4 respectively, shown in figures 1, 2, 3, 4 respectively.

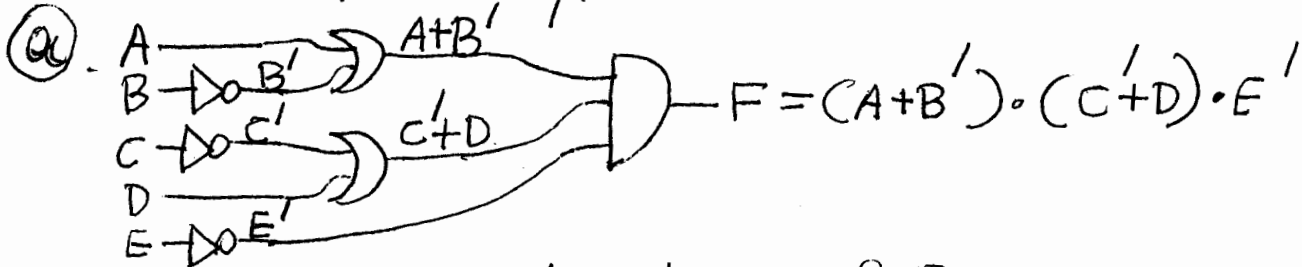


Figure 1: OR-AND realization of F.

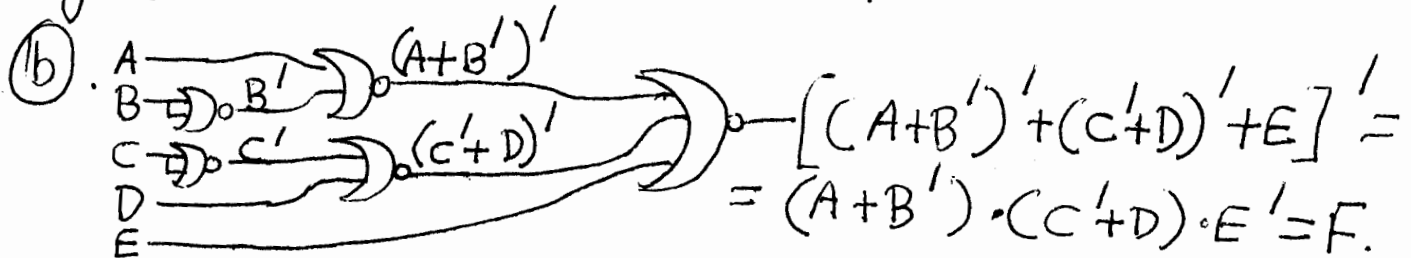


Figure 2: Realization of F using only NOR gates.

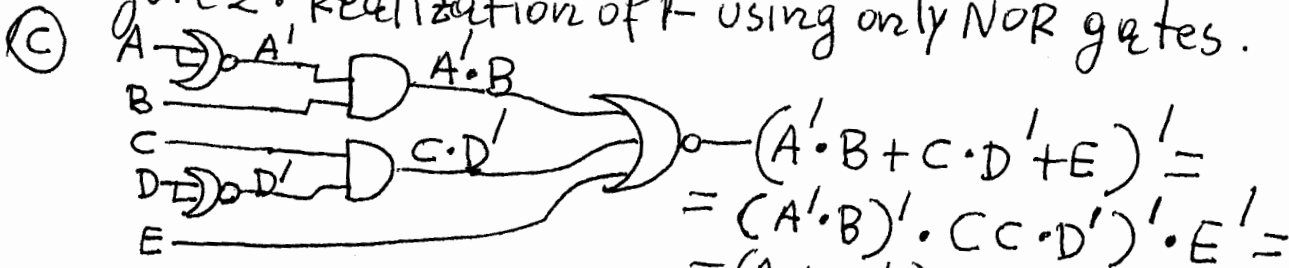


Figure 3: Realization of F using only AND and NOR gates.

Problem 4 cont.

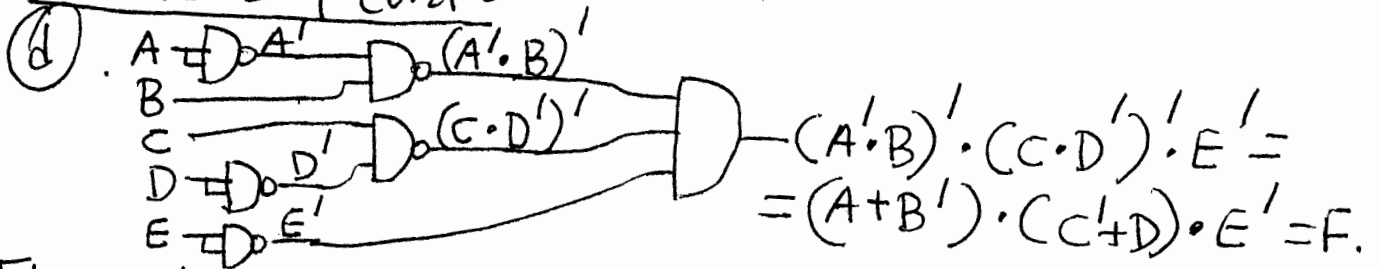


Figure 4: Realization of F using only NAND and AND gates.

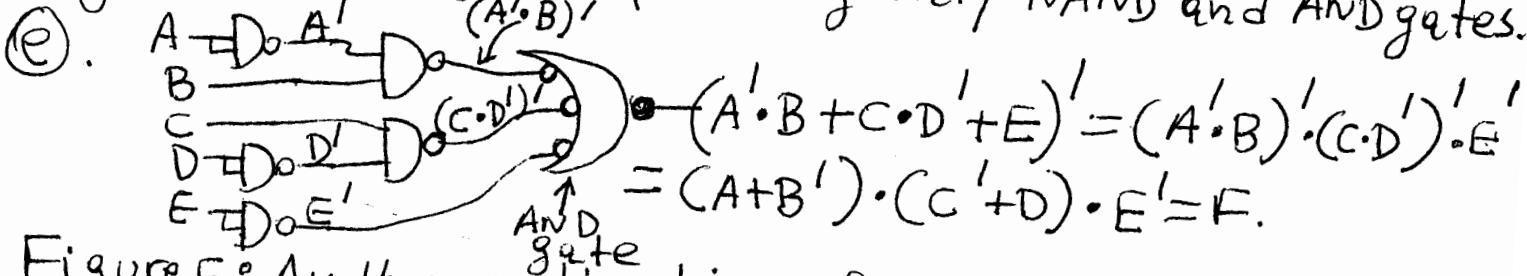


Figure 5: Another realization of F using only NAND and AND gates.



Figure 6: Another realization of F using only AND and NOR gates.

Problem 5:

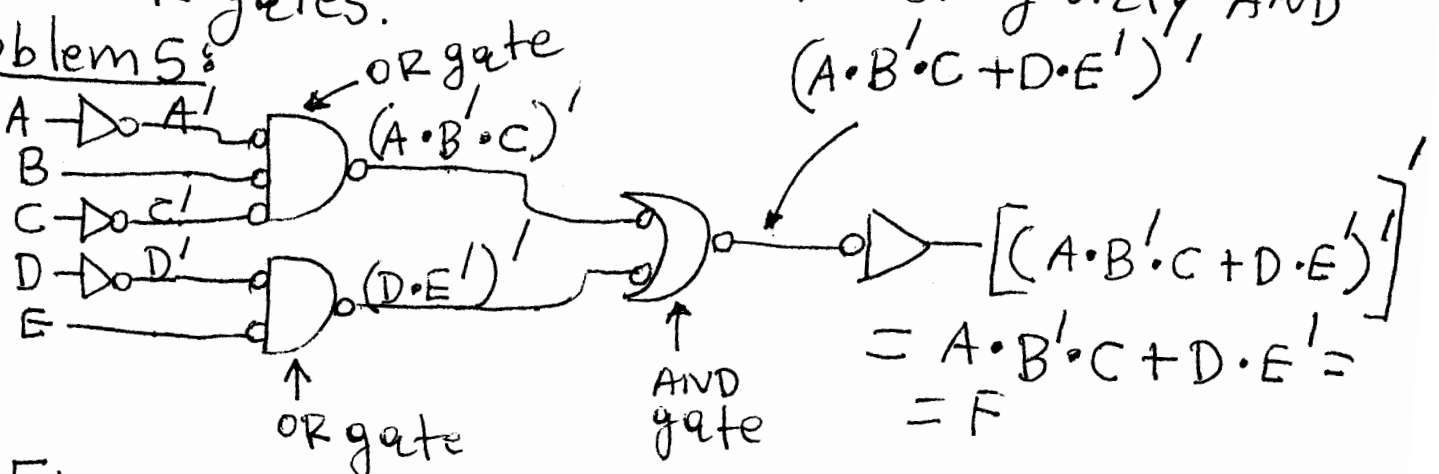


Figure 2: The equivalent OR-AND logic circuit for F.

Problem 6:

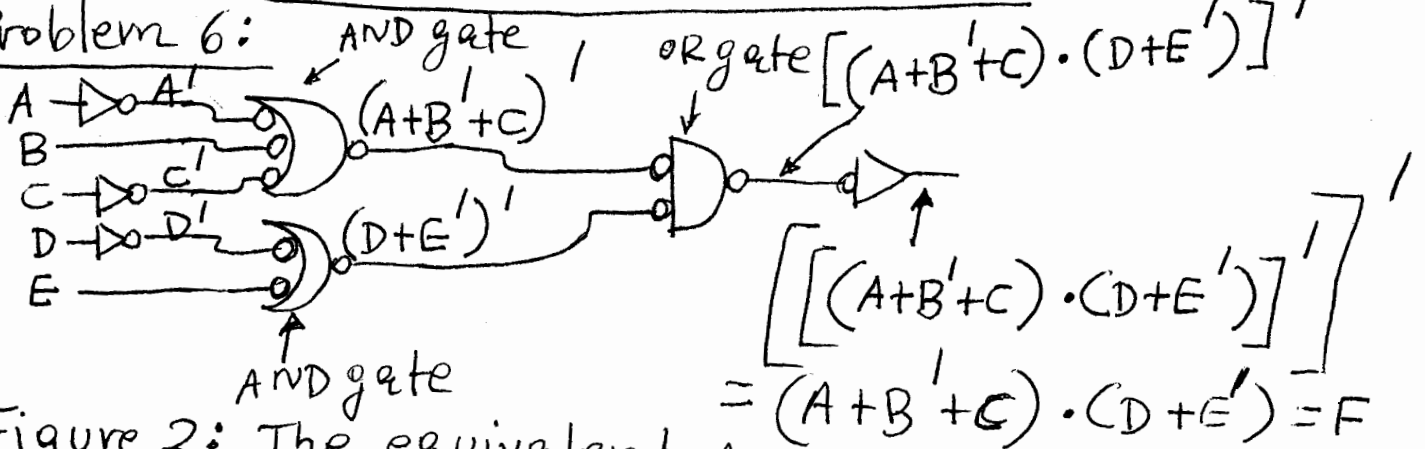


Figure 2: The equivalent AND-OR logic circuit for F.

Problem 7:

(a) Proof of (5) or proof of $X \oplus 0 = X$

- Case $X=0$: $0 \oplus 0 = 0$

- Case $X=1$: $1 \oplus 0 = 1$

(b) Proof of (6) or proof of $X \oplus 1 = X'$

- Case $X=0$: $0 \oplus 1 = 1$

- Case $X=1$: $1 \oplus 1 = 0$

(c) Proof of (7) or proof of $X \oplus X = 0$

- Case $X=0$: $0 \oplus 0 = 0$

- Case $X=1$: $1 \oplus 1 = 0$

(d) Proof of (8) or proof of $X \oplus X' = 1$

- Case $X=0$: $0 \oplus 1 = 1$

- Case $X=1$: $1 \oplus 0 = 1$

Note: The above equations (5), (6), (7), (8) can also be proved by using equation (1) on top of page 5 of handout #11.

(e) Proof of (11) or proof of

$$X \cdot (Y \oplus Z) = X \cdot Y \oplus X \cdot Z$$

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Problem 7 cont.

The right side of (11) is:

$$\begin{aligned} X \cdot Y \oplus X \cdot Z &= X \cdot Y \cdot (X \cdot Z)' + (X \cdot Y)' \cdot X \cdot Z = X \cdot Y \cdot (X' + Z') + \\ &+ (X' + Y') \cdot X \cdot Z = X \cdot Y \cdot X' + X \cdot Y \cdot Z' + X' \cdot X \cdot Z + Y' \cdot X \cdot Z \\ &= X \cdot Y \cdot Z' + X \cdot Y' \cdot Z = X \cdot (Y \cdot Z' + Y' \cdot Z) = X \cdot (Y \oplus Z). \end{aligned}$$

But we have now reached the left side of (11) so the proof is completed.

Note: In the above proof, I used eq. (1) on top of page 5 of handout #11 twice.