EE 2720, Spr. 05
Homework #5

Due Wednesday April 6 at 9:30 am
in my office (Room EE 245).

EE 2720, HW #5

Note: Please staple your homework.

Problem 1: Consider the logic function F where F is $F = A' \cdot B \cdot C + D \cdot E' + G$. Realize F using only NAND gates using the graphical approach (bubbles etc.). Show a figure.

Problem 2: Consider the logic function F where F is $F = CA' + B + C) \cdot (D + E') \cdot G$. Realize F using only NOR gates using the graphical approach (bubbles etc.). Show a figure.

Problem 3: Consider the logic function F where $F = A' \cdot B \cdot C + D \cdot E' + G$.

(a) Realize F using NOT, AND and OR gates. This is of course going to be and AND-OR realization. Call this realization, realization #1.

(b) Realize F using only NAND gates. Do <u>not</u> use the graphical approach this time. Use an algebraic approach this time. Call this realization, realization #2.

(c) Realize F using only OR and NAND gates. Call this realization, realization #3.

(d) Realize F using only NOR and OR gates. Call this realization, realization #4.

(e) Transform realization #3 into realization #4 using the graphical approach (bubbles etc.).

(f) Transform realization #4 into realization #3 using the graphical approach (bubbles etc.)

Note: You must show figures here in problem 3.

Problem 4: Consider the logic function F where F is $F = (A' + B + C) \cdot (D + E') \cdot G$.

(a) Realize F using NOT, OR and AND gates. This is of course going to be an OR-AND realization. Call this realization, realization #1.

(b) Realize F using only NOR gates. Do not use the graphical approach this time. Use an algebraic apprach instead. Call this realization, realization #2.

(c) Realize F using only AND and NOR gates. Call this realization, realization # 3.

(d) Realize F using only NAND and AND gates. Call this realization, realization #4.

(e) Transform realization # 3 into realization # 4 using the graphical approach (bubbles etc.).

(f) Transform realization # 4 into realization # 3 using the graphical approach (bubbles etc.).

Note: You must show figures here in problem 4 of course.

Problem 5: Consider the logic circuit of figure 1 on next page. It is an AND-OR logic circuit. Transform the circuit of fig. 1 into an equivalent OR-AND logic circuit by using the graphical approach (bubbles etc.). Show a figure

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Problem 5 cont:

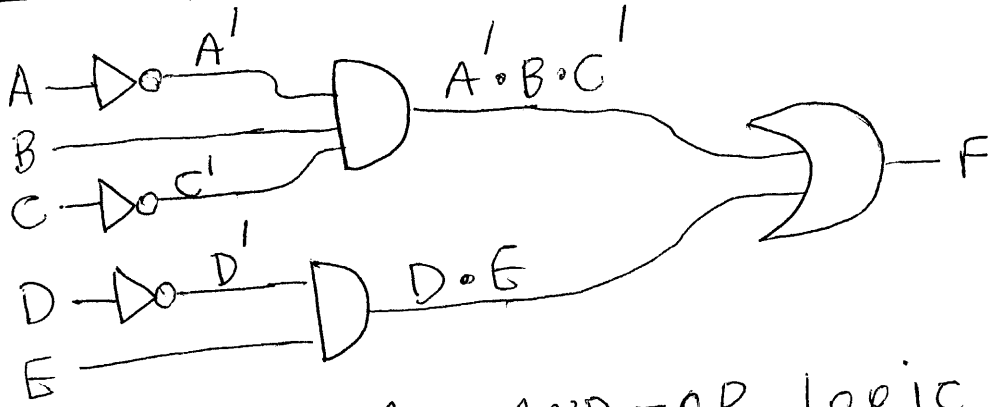

Figure 1: An AND-OR logic circuit

Problem 6: Consider the logic circuit of figure 2 below. It is an OR-AND logic circuit. Transform the circuit of figure 2 into an equivalent AND-OR logic circuit by using the graphical approach (bubbles etc). Show a figure.

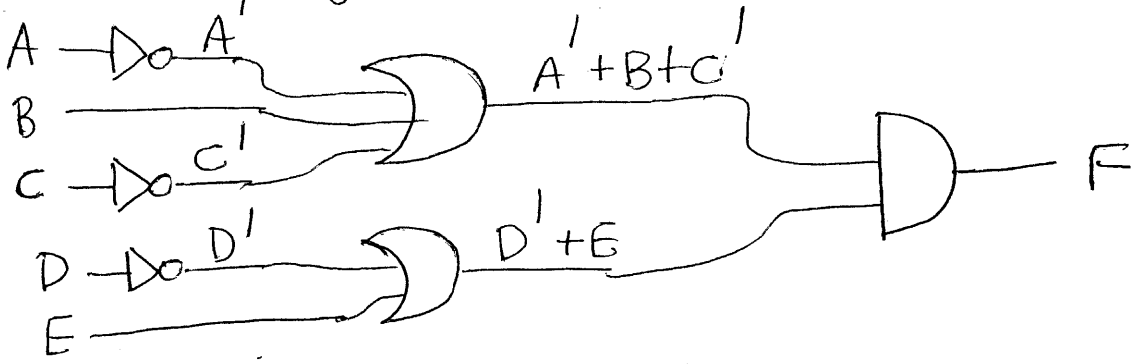

Figure 2: An OR-AND logic circuit.

Problem 7: Prove equations (5), (6), (7), (8) and (11) on page 8 of handout #11; (they relate to the XOR operator). You are not allowed to use a truth table when proving eq. (11).