Spring 2006
EE 2720 : Digital Logic I

Instructor:

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Text:

"*Digital Design: Principles & Practices(4-th Edition. Updated)*,"
John F. Wakerly.

Catalog Description:

Digital Logic I (2). Prereq: Admission to the College of Engineering. Boolean algebra; logic gates; minimization methods; analysis and synthesis of combinational logic networks; design examples.

Grading:

Test 1 : 25%
Test 2 : 25%
Homework : 15%
Quizzes : 10%
Final Exam : 25%

Test Policy :

If a student misses any one of tests 1 or 2 for a medical reason, then the student should provide the instructor with a doctor's statement stating that the student was sick on the day of the test. In this case, a make-up test will NOT be given but instead the remaining test will count for 35%, the homework for 20%, the quizzes 10% and the final for 35%.

Homework Policy :

Late homework will not be accepted.