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## EE 3755—Computer Organization

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Call Number 1701 (Fall 2001)

URL: <http://www.ece.lsu.edu/ee3755>

Offered by:

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Tentative office hours: Mon 15:00-16:00; Wed 9:30-10:30; Tue & Thr 14:00-15:30.

Should already know...

... how to design with logic.

Will learn...

... how to design a rudimentary computer.

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## Prerequisites

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Prerequisite by Course

EE 2730 (Digital Logic II) or equivalent.

Prerequisite by Topic

Logic design.

Binary number representation and arithmetic.

Programming of some kind.

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## Texts

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“Computer organization & design,” David A. Patterson & John L. Hennessy (Required).

“Verilog HDL,” Samir Palnitkar (Optional).

Additional Verilog reference material on course Web page.

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## Graded Material

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40% Midterm Exam

40% Final Exam

20% Homework (Roughly six assignments.)

Lowest grade dropped.

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## Short Course Outline

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### Hardware Description using Verilog

A commonly used language for designing digital hardware.

### Computer Arithmetic

How computers add, subtract, multiply, and divide.

Integer and floating-point.

Will use Verilog to design circuits.

### RISC Microprocessor Programming

The basics of programming an easy-to-program processor, MIPS.

### Computer Organization

Design hardware to execute MIPS programs.

This material will be continued in EE 4720.

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## Detailed Course Outline

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### Digital Design Hardware Description Languages (HDLs)

Designs for digital parts captured in a *HDL description*.

Popular HDLs: Verilog, VHDL.

An HDL description is fed to:

A simulator, to see what the design does.

(Whether it does what it's supposed to do.)

A synthesis program, to prepare the design for fabrication or downloading.

Chips may be fabricated using the synthesized description.

The synthesized description might be downloaded to a special chip (FPGA).

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### HDL Material

Language used: Verilog

Subset of the language covered.

Enough to implement processor arithmetic units and other datapath elements.

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### HDL Topics Covered

Writing structural descriptions of hardware.

Writing simple behavioral descriptions of hardware.

Relationship between descriptions and synthesized hardware.

### HDL Topics Not Covered

Less-common structural elements and delay specifiers.

Much event- and delay-related behavioral code.

Will not know enough to write a good *testbench*.

A thorough HDL treatment may be given in other courses.

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HDL Software Used

Host System

ECE Sun systems.

Simulator

Model Technology (Mentor Graphics) ModelSim SE Plus

Synthesis

Exemplar (Mentor Graphics) Leonardo Spectrum

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## Computer Arithmetic Topics

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Integer arithmetic algorithms. (Mostly review).

Ripple and carry-lookahead adder implementation.

ALU implementation.

Basic integer multiplication and division implementations.

High-speed integer multiplier implementation.

Floating-point representations.

Floating-point arithmetic algorithms.

Floating-point adder implementation.

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## RISC Microprocessor Topics

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RISC Processor

A type of processor that became popular in 80's.

RISCs simple to program and to implement (design hardware).

Simplicity allows high-speed implementation.

Starting in 80's all new major processors were RISCs ...

... until now with Intel's IA-64.

(IA-64 covered in EE 4720.)

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RISC Families:

MIPS: Ownership: Independent, then Silicon Graphics, now ??.

PA (Precision Architecture): Ownership: Hewlett-Packard.

SPARC: Ownership: Sun Microsystems / SPARC International.

POWER, PowerPC: Ownership: IBM, Apple/IBM/Motorola.

Alpha: Ownership: DEC, Compaq.

MIPS used in Patterson & Hennessy text (and so used in class).

SPARC used in ECE computers.

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Covered for the MIPS processor.

MIPS Processor organization:

What machine-language programs can access.

What machine-language instructions can do.

MIPS Programming

Subset of instructions covered.

Processors Covered in Other Courses

EE 3750 /3751: IA-32 (Intel 80x86, Pentium)

EE 4720: DLX, SPARC, some IA-64 and other architectures.

Building a “Toy” MIPS Processor

Use Verilog.

Topics

Hardware for major datapath elements: registers, program counter, etc.

Control for datapath elements.

Control for memory access instructions.

Control for conditional branches.

Material continued in EE 4720.