EE 4702-1: Digital Hardware Design Using Verilog

Syllabus

Where/When/How/URL
1112 CEBA Building
Monday Wednesday Friday 8:40–9:30 Spring 2000
Call Number 7289
http://www.ee.lsu.edu/ee4702

Who
David M. Koppelman
Room 349 Electrical Engineering Building
388-5482, koppel@ee.lsu.edu, http://www.ee.lsu.edu/koppel
Tentative Office Hours: Monday 9:40–11:10, Thursday 14:00–16:30.

Prerequisite
Credit or registration in EE 3750, or permission of instructor.

What
Drawing wires to connect logic gates may be fun (especially using a cool schematic capture program) when you’re working with half a dozen gates but is tedious when working with a larger number of components, say \(10^7\). Rather than using a schematic (graphical) representation, real systems are designed using hardware description languages (HDLs). Engineers design by writing HDL code, feeding the code to simulators to verify functionality, and feeding the code to synthesizers to complete the design.

The course will cover Verilog, one of two widely used HDLs. (The other is VHDL). Course work will include writing Verilog descriptions of circuits and testbench code, and verifying designs through simulation. PC- and Sun-hosted programs will be used.

Topics
Overview of digital design using hardware description languages.
Basic structural and behavior modeling.
Delay modeling and simulation.
Behavior modeling.
Synthesis.

Text
“Modeling, synthesis, and rapid prototyping with the Verilog HDL,” Michael D. Ciletti. A lower-cost text may be substituted.

Grading
35% Midterm Exam • 35% Final Exam • 30% Homework
Final exam weight may be increased for students who show significant improvement on the final exam.

Late-homework penalty: 10% per day late deducted. Missed-midterm-exam policy: at instructor’s discretion either a makeup exam, use final exam grade for midterm grade (i.e., 70% final exam weight), or use zero for midterm grade. Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class.