Problem 1: One instruction that MIPS lacks but many RISC ISAs have is an indexed load. Find the closest equivalent PowerPC instruction to SPARC’s `lw [%r2+%r3],%r1`.
(a) Show the instruction in PowerPC assembly language.
(b) Show how the instruction is coded, include the register numbers.

Problem 2: One instruction that MIPS lacks but that a few other RISC ISAs have is autoincrement addressing. PowerPC has an instruction that can be used for autoincrement addressing but is more powerful than the autoincrement addressing described in class. Find the PowerPC instruction.
(a) Show the assembly language for the PowerPC instruction doing the same thing as the following autoincrement instruction: `lw r1, (r2)+`.
(b) Show the coding for the instruction above.
(c) The PowerPC instruction is more powerful than an ordinary autoincrement instruction. Show a code sample using the PowerPC instruction for which an ordinary autoincrement would not be suitable. Briefly explain why an ordinary autoincrement would not do.

Problem 3: PowerPC has a wide variety of load and store instructions. Find the load instruction that is least suitable for a RISC ISA based upon the criteria discussed in class. Explain why it’s least suitable.

Problem 4: Some instructions are more difficult to implement than others, one reason is that the difficult instruction does something very different from normal instructions requiring at least a moderate amount of additional hardware. Some difficult-to-implement instructions are listed below. Explain what the difficulty is (what extra hardware or control complications would be needed).
(a) An indexed store instruction. (An indexed load instruction would not be considered difficult.)
(b) Autoincrement (or PowerPC’s version) load instructions. (The autoincrement or PowerPC version of the store instructions are not difficult.)