EE 4720: Computer Architecture

Syllabus

Where/When/How/URL
Room 1114 CEBA.
Monday Wednesday Friday 11:40–12:30 Spring 2005
Call Number 1895
http://www.ece.lsu.edu/ee4720/
RSS: http://www.ece.lsu.edu/ee4720/rss_home.xml

Who
David M. Koppelman
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Tentative Office hours: Monday–Friday: 9:00–10:00.

Topics
Instruction-Set Architecture and Microarchitecture
   Architecture and microarchitecture (implementation).
   Instruction set design and examples.

CPU Implementation
   Datapath components.
   Basic pipelining techniques.
   Basic scheduling techniques.
   Dynamic scheduling, register renaming techniques.
   Branch and target prediction, speculation, and, of course, misprediction recovery.
   Multiple instruction issue: superscalar and VLIW/EPIC.

Memory System Implementation
   Locality, the computer engineer’s best friend.
   Caches.
   Virtual memory.

Text
“Computer architecture, a quantitative approach,” John L. Hennessy & David A. Patterson, or

Grading
40% Midterm Exam • 40% Final Exam • 20% Homework
Final exam weight may be increased for students who show significant improvement on the final
exam.

Late-homework penalty: 10% per day late deducted. Missed-midterm-exam policy: at instruc-
tor’s discretion either a makeup exam, use final exam grade for midterm grade (i.e., 80% final
exam weight), or use zero for midterm grade. Daily attendance: optional, however students are
responsible for all material, instructions, and notices presented in class.