EE 3755: Computer Organization

Syllabus

Where/When/Web/RSS
Room 2142 P. Taylor Hall
Monday Wednesday Friday 9:30–10:20 Fall 2012
http://www.ece.lsu.edu/ee3755/
RSS: http://www.ece.lsu.edu/ee3755/rss_home.xml

Who
David M. Koppelman
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Tentative Office Hours: Monday–Friday: 14:00–15:00.

Topics
Introduction to Hardware Description Using Verilog

Computer Arithmetic
  Integer Add and Subtract Hardware
  Integer Multiplication Algorithms and Hardware
  Basic Integer Division Algorithm and Hardware
  IEEE 754 and Other Floating-Point Representations
  Floating-Point Addition Algorithm and Hardware
  Floating-Point Multiplication and Division Algorithms

Organization and Programming of a RISC Processor (MIPS)
  Registers, Memory, and Instruction Execution
  Assembly Language Programming

Basic Processor Implementation Techniques
  Datapath Elements (Registers, memory ports, etc.)
  Basic Processor Control Techniques

Texts
(The text used in EE 2720 and 2730.); Ciletti, “Advanced Digital Design with the Verilog HDL”
(Only a small portion used in 3755.)

Grading
40% Midterm Exam • 40% Final Exam • 20% Homework
Final exam weight may be increased for students who show significant improvement on the final exam.

Late-homework penalty: 10% per day late deducted. Missed-midterm-exam policy: at instructor’s discretion either a makeup exam, use final exam grade for midterm grade (i.e., 80% final exam weight), or use zero for midterm grade.
Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class.