Counters

- Clocked sequential circuit whose state diagram contains a single cycle.
- Modulus – number of states in the cycle.
- Counters with non-power of 2 modulus has unused states
Ripple Counters

- Ripple counter.
  - Requires fewer components than other counters.
  - Slowest one.
Synchronous Counters

- Synchronous counters.
  - The clock inputs of all flip-flops in the counter circuit are connected to a common clock signal.
- Synchronous serial counter.
Counters

- Synchronous parallel counter.
### Table 8-11: State table for a 74x163 4-bit binary counter.

<table>
<thead>
<tr>
<th>Input</th>
<th>Current State</th>
<th>Next State</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CLR</td>
<td>LD</td>
</tr>
<tr>
<td>0</td>
<td>x</td>
<td>x</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>x</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
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<td>1</td>
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</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
MSI Counters – 74x163
74x163 – Free Running Mode
74x163 – Modulo 11 Counters
74x163 – Cascading Counters

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Digital Design Principles and Practices, 3/e
74x163 – Modulo 193 Counter

[Diagram of a 74x163 Modulo 193 Counter circuit]

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74x163 – Modulo 8 Counter With Decoder

CLOCK_L
S0_L
S1_L
S2_L
S3_L
S4_L
S5_L
S6_L
S7_L
COUNT
0 1 2 3 4 5 6 7 0 1 2
Modulo 8 counter with decoder and glitch-free outputs.
Shift Registers

- $N$-bit register with the provision for shifting its stored data by a bit position each tick of the clock.
- Serial input – specifies a new bit to be shifted into the register.
- Serial output – specifies the bits being shifted out of the register.
Shift Registers

- **Parallel input** – specifies a new set of bits to be entered into the register, all at once during a single clock tick.

- **Parallel output** – specifies the bits at the output of every flip-flop in the register.
Shift Registers

- Serial-in, parallel-out shift register.

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Shift Registers

- Parallel-in, serial-out shift register.
Shift Registers

- **MSI Shift Registers.**
  - 74x164 – serial-in, parallel-out with asynchronous clear input.
  - 74x166 – parallel-in, serial-out with asynchronous clear input.
  - 74x194 – universal shift register.

<table>
<thead>
<tr>
<th>Function</th>
<th>Inputs S1 S0</th>
<th>Next state QA* QB* QC* QD*</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hold</td>
<td>0 0</td>
<td>QA  QB  QC  QD</td>
</tr>
<tr>
<td>Shift right</td>
<td>0 1</td>
<td>RIN QA QB QC</td>
</tr>
<tr>
<td>Shift left</td>
<td>1 0</td>
<td>QB  QC QD LIN</td>
</tr>
<tr>
<td>Load</td>
<td>1 1</td>
<td>A   B  C    D</td>
</tr>
</tbody>
</table>
Shift Registers
Shift Registers

- **Shift register counter** – a circuit formed by a shift registers and combinational logic. The state diagram for this state machine is cyclic. This circuit does not necessarily count in ascending or descending order.

- **Ring Counter** – the simplest shift register counter. This circuit uses a $n$-bit shift register to obtain a counter with $n$ states.
Shift Registers

The circuit diagram shows a 74x194 shift register with inputs for CLOCK, RESET, and data inputs A, B, C, D. The outputs are labeled Q0 through Q3, with Q0 being the least significant bit. The diagram indicates that the circuit is wired as a shift-left shift register, meaning that the data is shifted to the left with each clock pulse.

The state diagram illustrates the transition between states S1 to S4, with the corresponding Q0 through Q3 values shown for each state. The circuit is designed to process digital signals in a sequential manner, making it useful in applications requiring data shifting, such as serial communication interfaces.
Shift Registers
A self correcting counter is designed so that all abnormal states have transitions leading to normal states.
Shift Registers

- Twisted-ring, Moebius or Johnson counter is a $n$-bit shift register whose serial input receives the complement of serial output.

- This counter has $2^n$ states.
Shift Registers

- Digital telephony.
  - Central offices samples analog voice 8000 times/sec (once every 125 μs).
  - Then the COs transmit them digitally over a 64kbps serial channel.
  - 64kbps is much less than can be achieved by a single digital line, therefore several 64kbps signals are multiplexed onto a single wire.
Shift Registers
Shift Registers

CLOCK  (2.048 MHz)

SYNC

SDATA timeslot 31 timeslot 0 timeslot 1 \ldots timeslot 31 timeslot 0

256 clock ticks per 125 μsec frame

488 nsec

32 timeslots per frame

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Shift Registers

CLOCK
SYNC_L
from source
SDATA

+5 V
R

74x163
CLK
CLR
LD
ENP
ENT
A
B
C
D
QA
QB
QC
QD
RCO

74x164
CLK
CLR
SER
SERB
QA
QB
QC
QD
RD0
RD1
RD2
RD3
RD4
RD5
RD6
RD7

74x377
CLK
G

U5
U6
U4
U3

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Shift Registers