EE 2723  Spring 2012

Homework #7 and solution of HW #7

Not to be returned (it will not be graded)
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Problem: Write an explicit structural Verilog description to implement \( x = (a \oplus b) + c \). Here \( \oplus \) denotes EXCLUSIVE-OR operation and \( + \) denotes OR operation. You are not allowed to instantiate one Exclusive-OR gate. Use AND, OR, NOT gates instead. Your module should be complete including module name, port list, declaration of inputs and outputs, declaration of wires and proper gate instantiation.

b) Write an implicit structural Verilog description to implement \( x = (a \oplus b) + c \).
Solution: \( x = (a \oplus b) + c = a' \cdot b + a \cdot b' + c \)

module alex(x, a, b, c);
input a, b, c;
output x;
wire na, nb, na_b, a_nb;
not n1(na, a);
not n2(nb, b);
and a1(na_b, na, b);
and a2(a_nb, a, nb);
or o1(x, na_b, a_nb, c);
endmodule

module george(x, a, b, c);
input a, b, c;
output x;
assign x = (a \land b) \lor c;
endmodule