EE 2728  Spr. 2012

Homework #5

Due Monday  April 16, 2012, in class
Problem 1: (a) Using a decoder with complemented outputs and a NAND gate implement the logic function
\[ F = \Sigma_{A,B,C,D} (0, 3, 4, 6, 9, 11, 13, 14, 15) \]
(b) Using a decoder with complemented outputs and an AND gate implement the logic function of part (a) above.
(c) Using a decoder with uncomplemented outputs and an OR gate implement the logic function of part (b) above.
(d) Using a decoder with uncomplemented outputs and a NOR gate implement the logic function of part (c) above.

Problem 2: Using a decoder with uncomplemented outputs and an OR gate implement the logic function
\[ F = (A' + B + C') \cdot (B + C' + D) \cdot (A + C' + D') \]
Problem 3: Using a decoder with complemented outputs and an AND gate implement the logic function of problem 2.

Problem 4: Using a decoder with complemented outputs and an AND gate implement the logic function

\[ F = A'B'C' + B'C'D + A'C'D' \]

Problem 5: Using a decoder with uncomplemented outputs and an OR gate implement the logic function of problem 4.