

Hierarchical Pipeline Optimization of Coarse Grained Reconfigurable Processor for Multimedia Applications

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Overview of REMUS-II

Coarse Grain Reconfigurable architecture developed by Southeast University, Tsinghua University, etc



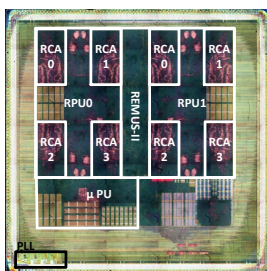
Targeting at domain specific applications with inherent data parallelism and computation intensive requirements

H.264
MPEG-4/AVC

MPEG2
AVS



layout: TSMC 65nm



Low Power Design:
Dual V_{dd} , DVFS, etc.

Computer Vision:
face recognition, face detection

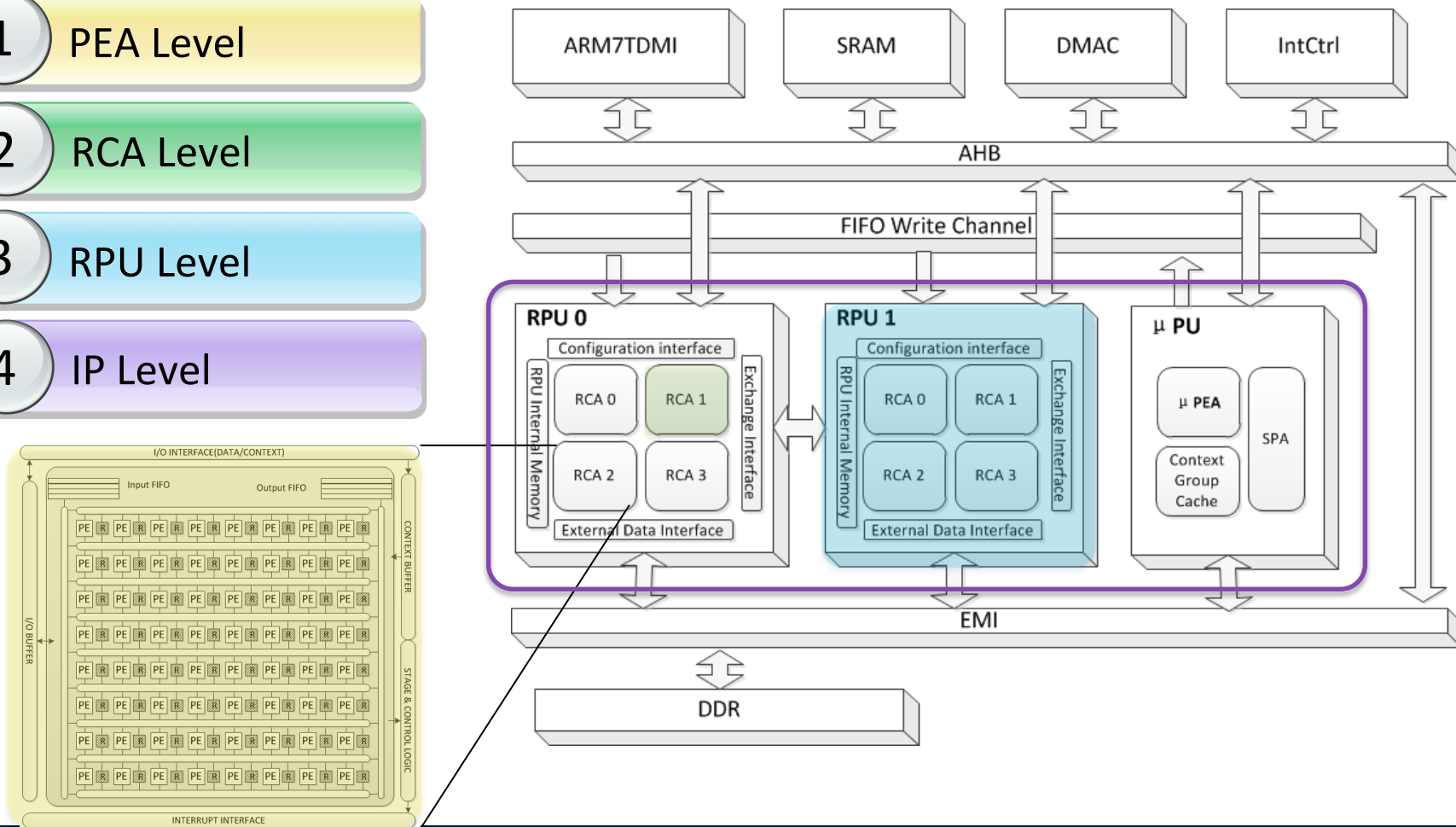


Soft-Define Radio:

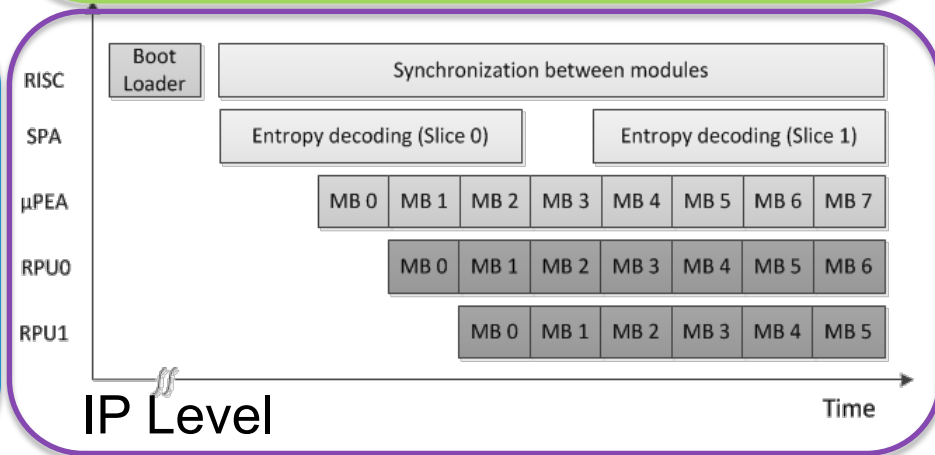
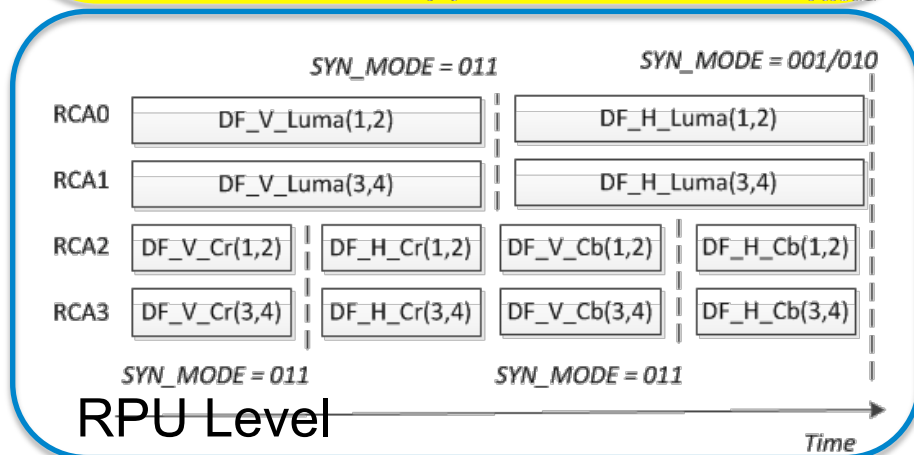
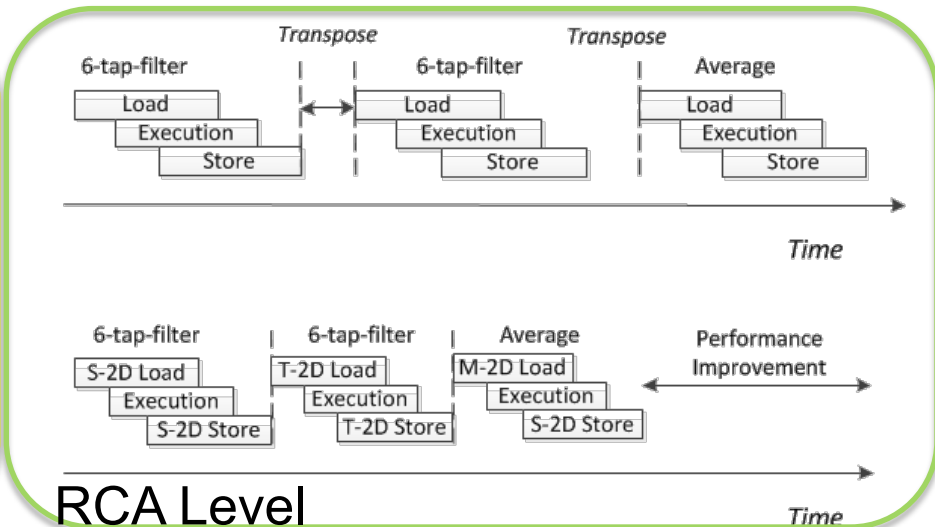
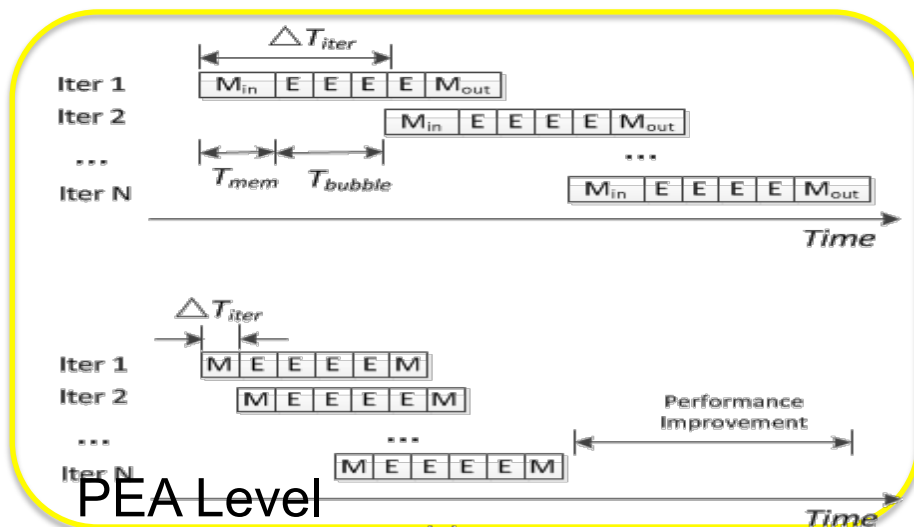


The Hierarchy of REMUS-II

- 1 PEA Level
- 2 RCA Level
- 3 RPU Level
- 4 IP Level

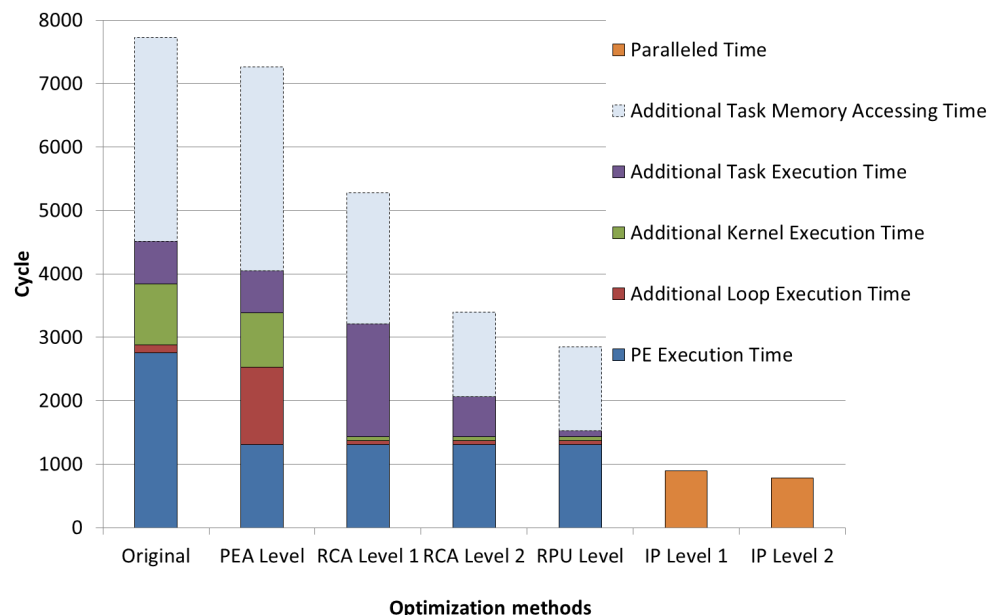


Hierarchical Pipeline Optimization of Different Levels



Experimental Results

**H.264/AVC EXAMPLE:
THE AVERAGE DECODING CYCLES OF REDUCE
2.93 TIMES ON THE REMUS-II.**



MULTIMEDIA DECODING RESULT COMPARISON BETWEEN THE REMUS-II AND OTHER ARCHITECTURES

Architecture	Technology & Die Size	Working Frequency	Power Consumption	Multimedia decoding Performance
CGRA This paper REMUS-II	65 nm 48.9mm ²	200 MHz	201 mW	H.264/AVC: High Profile 1080p@30fps AVS: Jizhun Profile 1080p@39fps MPEG-2: Main Profile 1080p@41fps
CGRA ADRES	NA	333 MHz	NA	H.264/AVC: Main Profile 1080p@30fps
CGRA XPP	90nm 42.5 mm ²	450 MHz	2043mW@150Hz	H.264/AVC: Main Profile 1080p@24fps
SIMD AnySP	90nm 25.17 mm ²	300 MHz	1347 mW	H.264/AVC: Basic Profile 4CIF@30fps
SIMD	NA	359 MHz	NA	AVS: D1@25fps
DSP Davinci	NA	600 MHz	558 mW	H.264/AVC: Main Profile D1@25fps
Multi-Core: CELL	NA	2.4 GHz 3.2 GHz	~4 W	H.264/AVC: Main Profile 1080p@20fps MPEG-2: D1@120fps
Multi-Core: cortex A9 dual	NA	400 MHz	500 mW	H.264/AVC: High Profile 720p@30fps

Thank You!

More details will show in the Interactive Session.