RAW 2011

The 18th Reconfigurable Architectures Workshop

Advance Program

DAY 1-May 16, 2011

8:00-8:45 Registration

8:45-9:00 Chair's Welcome

9:00-10:00 **RAW Keynote 1: Tim Mattson, Intel Corporation, "It's all about the Software; Everything else is a Secondary Concern", (Session Chair: Jürgen Becker)**

10:00-10:45 Coffee break

Session1: Novel Approaches for MPSoC and Multicore Architectures (Session Chair: René Cumplido)

10:45-11:10 "A High-Level Power Model for MPSoC on FPGA", Roberta Piscitelli and Andy Pimentel

11:10-11:35 "Modular Framework for Multi-Level Multi-Device MPSoC Simulation", Christoph Roth, Gabriel Marchesan Almeida, Oliver Sander, Luciano Ost, Nicolas Hebert, Gilles Sassatelli, Pascal Benoit, Lionel Torres and Jürgen Becker

11:35-12:00 "A Heterogeneous Multicore System on Chip with Run-Time Reconfigurable Virtual FPGA Architecture", Michael Hübner, P. Figuli, R. Girardey, D. Soudris, K. Siozios and J. Becker

12:00-13:30 Lunch

Session 2: New Architectures for Reconfigurable Computing (Session Chair: Lilian Bossuet)

13:30-13:55 "A Scalable Microarchitecture Design that Enables Dynamic Code Execution for Variable-Issue Clustered Processors", Ralf Koenig, Timo Stripf and Jürgen Becker

13:55-14:20 "CRM: Configurable Range Memory for Fast Reconfigurable Computing", Jongkyung Paek, Jongeun Lee and Kiyoung Choi

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14:20-15:00 **POSTER SESSION 1** / Coffee break (list of papers at the end)

Session 3: Methods and Design Techniques for Partially Reconfigurable Architectures (Session Chair: Christophe Bobda)

15:00-15:25 “Tuple Spaces in Hardware for Accelerated Implicit Routing”, Zachary Baker and Justin Tripp

15:25-15:50 “High Speed Partial Run-Time Reconfiguration Using Enhanced ICAP Hard Macro”, Simen Gimle Hansen, Dirk Koch and Jim Tørresen

15:50-16:15 “Online Routing of FPGA Clock Networks for Module Relocation in Partial Reconfigurable Multi Clock Designs”, Christian Schuck, Bastian Haetzer, Michael Hübner and Jürgen Becker

16:15-16:45 **POSTER SESSION 1** / Coffee break (list of papers at the end)

Session 4: Improving Security of Reconfigurable Systems (Session Chair: Peter Athanas)

16:45-17:10 “Securing Boot of an Embedded Linux on FPGA,” Florian Devic, Lionel Torres and Benoît Badrignans

17:10-17:35 “Hyperelliptic Curve Cryptoarchitecture for Fast Execution of Schnorr and Okamoto Authentication Protocols”, Alexander Klimm, Sebastian Vogel and Jürgen Becker

17:35-18:00 “A Reconfigurable Multi-core Cryptoprocessor for Multi-Channel Communication Systems”, Michael Grand, Lilian Bossuet, Guy Gogniat, Bertrand Le Gal, Jean-Philippe Delahaye and Dominique Dallet

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DAY 2-May 17, 2011

8:00-9:30 IPDPS Keynote

9:30-10:00 Coffee Break

10:00-11:00 **RAW Keynote 2 - Tarek El-Ghazawi, George Washington University, "The Challenges of Computing with FPGAs" (Session Chair: Viktor Prasanna)**

Session 5: Tools for Partially Reconfigurable FPGAs (Session Chair: Michael Hübner)

11:00-11:25 "Migrating Static Systems to Partially Reconfigurable Systems on Spartan-6 FPGAs", Christian Beckhoff, Dirk Koch and Jim Tørresen

11:25-11:50 "ReBit: A Tool to Manage and Analyse FPGA-Bbased Reconfigurable Systems", Marco D Santambrogio, Andrea Cazzaniga, Alessandra Bonetto and Donatella Sciuto

11:50-12:15 "OpenPR: An Open-Source Partial-Reconfiguration Toolkit for Xilinx FPGAs", Ali Asgar Sohanghpurwala, Peter Athanas, Tannous Frangieh and Aaron Wood

12:15-13:45 Lunch

Session 6: Emerging Methods for Coarse grain Reconfigurable Architectures (Session Chair: Pascal Benoit)

13:45-14:10 "Occam-pi as a High-level Language for Coarse-Grained Reconfigurable Architectures", Zain Ul-Abdin and Bertil Svensson

14:10-14:35 "Dynamic Reconfiguration for Irregular Code using FNC-PAE Processor Cores," Eberhard Schüler, Martin Vorbach, Frank May and Markus Weinhardt

14:35-15:15 **POSTER SESSION 2** / Coffee break (list of papers at the end)

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Session 7: Task Management in Reconfigurable Systems (Session Chair: Marco D. Santambrogio)

15:15-15:40 "A Replacement Technique to Maximize Task Reuse in Reconfigurable Systems", Juan Antonio Clemente, Javier Resano and Daniel Mozos

15:40-16:05 "Integrated Temporal Planning, Module Selection and Placement of Tasks for Dynamic Networks-on-Chip", Philipp Mahr, Steffen Christgau, Christian Haubelt and Christophe Bobda

16:05-16:30 "Enhancing Resource Utilization with Design Alternatives in Runtime Reconfigurable Systems", Alexander Wold, Dirk Koch and Jim Tørresen

16:30-17:00 **POSTER SESSION 2** / Coffee break (list of papers at the end)

Session 8: Improving Computing Efficiency in FPGAs based systems (Session Chair: René Cumplido)

17:00-17:25 "Asymmetric Large Size Signed Multipliers Using Embedded Blocks in FPGAs", Shuli Gao, Dhamin Al-Khalili and Noureddine Chabini

17:25-17:50 "Just-in-time Instruction Set Extension - Feasibility and Limitations for an FPGA-based Reconfigurable ASIP Architecture", Mariusz Grad and Christian Plessl

17:50-18:00 Closing Remarks

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Poster Session 1

"Improving Reconfigurable Hardware Energy Efficiency and Robustness via DVFS-Scaled Homogeneous MP-SoC", Roberto Airoldi, Fabio Garzia and Jari Nurmi

"Compression Based Efficient and Agile Configuration Mechanism for Coarse Grained Reconfigurable Architectures", Syed M. Asad Hassan Jafri, Ahmed Hemani, Kolin Paul, Juha Plosila and Hannu Tenhunen

"Fast hardware computation of x mod z", Jon Butler and Tsutomu Sasao

"Native Double-Precision LINPACK Implementation on a Hybrid Reconfigurable CPU", Thang Viet Huynh, Manfred Mücke and Wilfried Gansterer

"FeatureVerilog: Extending Verilog to support Feature-Oriented Programming", Jun Ye, Qingping Tan, Tun Li and Guorong Cao

"A FPGA-based Accelerator to Speed-up Matrix Multiplication of Floating Point Operations", Bruno Holanda, Rodrigo Pimentel, João Paulo, Rodrigo Camarotti, João Cleber, Viviane Souza, Julio Ferraz, Abel Silva-Filho and Manoel Lima

Poster Session 2

"The SecretBlaze: A Configurable and Cost-Effective Open-Source Soft-Core Processor", Lyonel Barthe, Luís Vitório Cargnini, Pascal Benoit and Lionel Torres

"Bitonic Sorting on Dynamically Reconfigurable Architectures", Josef Angermeier, Eugen Sibirko, Rolf Wanka and Jürgen Teich

"Distributed Resource Management in Massively Parallel Processor Arrays", Vahid Lari, Frank Hannig and Jürgen Teich

"Reconfigurable Instruction Decoding for a Wide-Control-Word Processor", Alen Bardizbanyan, Magnus Själander and Per Larsson-Edefors

"Distributed Security for Communications and Memories in a Multiprocessor Architecture", Pascal Cotret, Jérémie Crenne, Guy Gogniat, Jean-Philippe Diguet, Lubos Gaspar and Guillaume Duc

"On an Hybrid and General Control Scheme for Algorithms Represented as a Polytope", Roberto Pérez-Andrade, César Torres-Huitzil, René Cumplido and Juan M. Campos

"A Multi-level Reconfigurable Architecture for a Wireless Sensor Node Coprocessing Unit", François Philipp and Manfred Glesner