Reconfigurable Architectures Workshop - RAW 2008

Final Program

Monday 14th April

0830 - 1000 Session 1

Session Chair - Juergen Becker, University of Karlruhe

0830 Chairman's Welcome

0835 Keynote Address by Professor Donatella Sciuto

"Design methodology for partial dynamic reconfiguration: a new degree of freedom in the HW/SW codesign"

0935 Marco Domenico Santambrogio and Vincenzo Rana and Donatella Sciuto and Fabio Cancarè

"A Design Flow Tailored for Self Dynamic Reconfigurable Architecture"

1000 - 1100 Morning Tea and Poster Session Day One

1100-1215 Session 2

Session Chair - Jerry Morris, ERDC MSRC

1100 Amirhossein Alimohammad and Saeed Fouladi Fard and Bruce Cockburn and Christian Schlegel

"On the Efficiency and Accuracy of Hybrid Pseudo-Random Number Generators for FPGA-Based Simulations"

1125 Zachary Baker and Reid Porter

"Rotationally Invariant Sparse Patch Matching on GPU and FPGA"

1150 Sean Whitty and Rolf Ernst

"A Bandwidth Optimized SDRAM Controller for the MORPHEUS Reconfigurable Architecture"

1215-1345 Lunch

1345-1500 Session 3

Session Chair - Luigi Carro, Instituto de Informática da UFRGS

1345 Gayatri Mehta and Colin Ihrig and Alex Jones

"Reducing Energy by Exploring Heterogeneity in a Coarse-grain Fabric"

1410 Yoonjin Kim and Rabi N. Mahapatra

"Reusable Context Pipelining for Low Power Coarse-Grained Reconfigurable Architecture"

1435 Nick Mould and Brian Veale and John Antonio and Monte Tull and John Junger

"Design of Steering Vectors for Dynamically Reconfigurable Architectures"

1500 - 1530 Afternoon Tea

1530-1740 Session 4

Session Chair - Marco Santambrogio, Milan Polytechnic

1530 Josef Angermeier and Jürgen Teich

"Heuristics for Scheduling Reconfigurable Devices with Consideration of Reconfiguration Overheads"

1555 Justin Teller and Fusun Ozguner and Robert Ewing

"Scheduling Reconfiguration at Runtime on the TRIPS Processor"

1620 Julio Septien and Daniel Mozos and Hortensia Mecha and Jesus Tabero and Miguel Angel García

"Perimeter Quadrature-based metric for estimating FPGA fragmentation in 2D HW multitasking"

1645-1650 Short Break

1650 Mao Nakajima and Daisaku Seto and Minoru Watanabe

"A 937.5ns multi-context holographic configuration with a 30.75us retention time"

1715 Alexander Klimm and Lars Braun and Juergen Becker

"An Adaptive And Scalable Multiprocessor System For Xilinx FPGAs Using Minimal Sized Processor Core"

1740 CLOSE DAY 1

Tuesday 15th April

0800-0930 IPDPS Keynote

0930 - 1030 Morning Tea and Poster Session Day Two

1030 - 1130 Session 5

Session Chair - R. (Vaidy) Vaidyanathan, Louisiana State University

1030 Keynote Address by Dr Fabio Campi

"(Re-) Configurable Solution for the high-volume ASIC market"

1130-1245 Session 6

Session Chair - Masanori Hariyama, Tohoku University

1130 Michael Huebner and Lars Braun and Diana Goehringer and Juergen Becker

"Run-Time Reconfigurable Adaptive Multilayer Network-On-Chip For FPGA-Based Systems"

1155 Faizal Arya Samman and Thomas Hollstein and Manfred Glesner

"Flexible Parallel Pipeline Network-on-Chip based on Dynamic Packet Identity Management"

1220 Leandro Fiorin and Slobodan Lukovic and Gianluca Palermo

"Implementation of a Reconfigurable Data Protection Module for NoC-based MPSoC"

1245-1345 Lunch

1345-1500 Session 7

Session Chair - Brian Veale, IBM Systems & Technology Group

1345 Alessio Montone and Vincenzo Rana and Marco Domenico Santambrogio and Donatella Sciuto

"HARPE: a Harvard-based Processing Element Tailored for Partial Dynamic Reconfigurable Architectures"

1410 Diana Goehringer and Michael Huebner and Volker Schatz and Juergen Becker

"Runtime Adaptive Multi-Processor System-on-Chip: RAMPSoC"

1435 Florian Dittmann, Stefan Frank and Simon Oberthür

"Algorithmic Skeletons for the Design of Partially Reconfigurable Systems"

1500 - 1530 Afternoon Tea

1530-1645 Session 8

Session Chair - Ying Chen, San Francisco State University

1530 Mateus Beck Rutzig and Antonio Carlos Schneider Beck and Luigi Carro

"Balancing Reconfigurable Data Path Resources According to Application Requirements"

1555 Deepak Sreedharan and Ali Akoglu

"A Hybrid Processing Element based Reconfigurable Architecture for Hashing Algorithms"

1620 Yi Lu and Thomas Marconi and Georgi Gaydadjiev and Koen Bertels

"A Self-adaptive on-line Task Placement Algorithm for Partially Reconfigurable Systems"

1645 CLOSE DAY 2

POSTER PAPERS DAY ONE

Poster Session Chair - Michael Huebner, University of Karlsruhe

Santheeban Kandasamy and Andrew Morton and Wayne Loucks:

"Configuration Scheduling Using Temporal Locality and Kernel Correlation"

Fabio Garzia and Claudio Brunelli and Davide Rossi and Jari Nurmi:

"Implementation of a floating-point matrix-vector multiplication on a reconfigurable architecture"

Volker Hampel and Peter Sobe and Erik Maehle:

"Designing Coprocessors for Hybrid Compute Systems"

Joachim Becker:

"A high-bandwidth field programmable analog array for reconfigurable communication front-ends"

Matthias Kuehnle and Christian Schuck and Michael Huebner and Juergen Becker:

"A framework for dynamic 2D placement on FPGAs"

Manish Birla and Krishna Vikram:

"Partial Run-time Reconfiguration of FPGA for Computer Vision Applications"

Shenchih Tung and Alex Jones

"Physical Layer Design Automation for RFID Systems"

Oliver Sander and Alexander Klimm and Benjamin Glas and Juergen Becker and Klaus Mueller-Glaser:

"A self adaptive interfacing concept for consumer device integration into automotive entities"

POSTER PAPERS DAY TWO

Poster Session Chair - Michael Huebner, University of Karlsruhe

Eunjung Cho and Anu Bourgeois and José Fernández-Zepeda:

"Efficient and accurate FPGA-based simulator for Molecular Dynamics"

Henrik Svensson and Thomas Lenart and Viktor Öwall:

"Modelling and Exploration of a Reconfigurable Array using SystemC TLM"

Yi-Gang Tai and Chia-Tien Dan Lo and Kleanthis Psarris:

"Accelerating Matrix Decomposition with Replications"

Ruchika Verma and Ali Akoglu:

"A Coarse Grained and Hybrid Reconfigurable Architecture with Flexible NOC Router for Variable Block Size Motion Estimation"

Ying Yu and Raymond Hoare and Alex Jones:

"A CAM-based Intrusion Detection System for Single-packet Attack Detection"

Christopher Vutsinas and Tarek Taha and Kenneth Rice:

"A Neocortex Model Implementation on Reconfigurable Logic with Streaming Memory"

Pradeep Fernando and Hariharan Sankaran and Srinivas Katkoori and Didier Keymeulen and Adrian Stoica and Ricardo Zebulum and Ramesham Rajeshuni:

"A Customizable FPGA IP Core Implementation of a General Purpose Genetic Algorithm Engine"

Masanori Hariyama and Kensaku Yamashita and Michitaka Kameyama:

"FPGA Implementation of a Vehicle Detection Algorithm Using Three-Dimensional Information:

Kouji Shinohara and Minoru Watanabe:

"Defect tolerance of holographic configurations in ORGAs"
