Call for Participation

RAW 2007

14th Reconfigurable Architectures Workshop

March 26–27, 2007
Renaissance Long Beach Hotel
Long Beach - California, USA
www.ece.lsu.edu/vaidy/raw

Schedule – Monday, March 26th 2007

08:00 - 08:15 Welcome & Opening

08:15 - 09:00 Keynote I

Problem-Oriented Configurable and Reconfigurable Architectures,
Gordon Brebner, Xilinx

09:00 - 10:00 Dynamic and Partial Reconfiguration I

(Session Chair: G. Sassatelli)
A new framework to accelerate VirtexII Pro dynamic partial self-reconfiguration,
Christopher Claus, Florian H. Müller, Johannes Zeppenfeld, Walter Stechele

Partial dynamic reconfiguration in a multi-FPGA clustered architecture based on Linux,
Vincenzo Rana, Marco Santambrogio, Donatella Sciuto, Boris Kettelhoit, Markus Koester, Mario Porrmann, Ulrich Rückert

Communication Architectures for Dynamically Reconfigurable FPGA Designs,
Thilo Pionteck, Carsten Albrecht, Roman Koch, Erik Maehle, Michael Hübner, Jürgen Becker

10:00 – 10:30 Coffee Break

10:30 – 11:50 Methods and Tools for reconfigurable Architectures

(Session Chair: R. Vaidyanathan)
Optimization of Area and Performance by Processor-Like Reconfiguration,
Tobias Oppold, Sven Eisenhardt, Wolfgang Rosenstiel

Splice: A Standardized Peripheral Logic and Interface Creation Engine,
Justin Thiel, Ron Cytron

Exploiting Communication Concurrency for Efficient Deadlock Free Routing in Reconfigurable NoC Platforms,
Maurizio Palesi, Shashi Kumar, Rickard Holsmark, Vincenzo Catania

Power-Aware Routing for Well-Nested Communications On The Circuit Switched Tree,
Hatem El-Boghdadi

11:50 - 13:20 Lunch Break

13:20 - 14:20 Coarse grained Processing and Architectures I

(Session Chair: L. Torres)
QUKU: An FPGA Based Flexible Coarse Grain Architecture Design Paradigm using Process Networks,
Sunil Shukla, Neil W. Bergmann, Juergen Becker

Interconnect Prediction and Customization for a Coarse-grained Reconfigurable Fabric,
Alex Jones, Gayatri Mehta, Justin Stander, Mustafa Baz, Brady Hunsaker

A Modulo Scheduling Algorithm for a Coarse-Grain Reconfigurable Array Template,
Akira Hatanaka, Nader Bagherzadeh

14:20 - 15:00 Architectures I

(Session Chair: S.Shukla)
A CAM Emulator Using Look-Up Table Cascades,
Hiroki Nakahara, Tsutomu Sasao, Munehiro Matsuura

A Reconfigurable Computing Engine for Wavelet Transforms,
Kang Sun, Xuezeng Pan, Jiebing Wang, Zugen Liu

15:00 – 15:30 Coffee Break

15:30 – 16:10 Simulation

(Session Chair: M.Santambrogio)
Using an FPGA for Fast Bit Accurate SoC Simulation,
Pascal T. Wolkotte, Philip K.F. Holzenspies, Gerard J.M. Smit

A General Purpose Partially Reconfigurable Processor Simulator (PReProS),
Alisson V Brito, Matthias Kuehnle, Elmar U K Melcher, Juergen Becker

16:10 – 17:10 Domain specific Architectures

(Session Chair: T. Pionteck)
CONFETTI : A reconfigurable hardware platform for prototyping cellular architectures,
Fabien Vannel, Pierre-André Mudry, Gianluca Tempesti, Daniel Mange

A Reconfigurable Load Balancing Architecture for Molecular Dynamics,
Jonathan Phillips, Matthew Areno, Chris Rogers, Aravind Dasu, Brandon Eames

Fast SEU Detection and Correction in LUT Configuration Bits of SRAM-based FPGAs,
Hamid R. Zarandi, Seyed Ghassem Miremadi, Dhiraj K. Pradhan, Costas Argyrides

17:10 – 17:20 Short Break

17:20 – 18:00 Coarse grained Architecture Application

(Session Chair: C. Valderrama)
Radiation Hardened Coarse-Grain Reconfigurable Architecture for Space Applications,
Sajid Baloch, Tughrul Arslan, Adrian Stoica

A cryptographic coarse grain reconfigurable architecture robust against DPA attacks,
Daniel Mesquita, Lionel Torres, Michel Robert, Fernando Moraes, Benoît Badrignans

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09:00 - 10:00 IPDPS Keynote

10:00 – 10:30 Coffee Break

10:30 – 11:50 Coarse grained Processing and Architectures II

(Session Chair: B.Veale)

Hierarchical Cluster Assignment for Coarse-Grained Reconfigurable Coprocessors,
Martino Sykora, Davide Pavoni, Joel Cambonie, Roberto Costa, Stefano Crespi Reghizzi

Using Rewriting Logic to Match Patterns of Instructions from a Compiler Intermediate Form to Coarse-Grained Processing Elements,
Carlos Morra, Joao Cardoso, Juergen Becker

SPEEDUPS AND ENERGY SAVINGS OF MICROPROCESSOR PLATFORMS WITH A COARSE-GRAINED RECONFIGURABLE DATA-PATH,
Michalis Galanis, Gregory Dimitroulakos, Costas Goutis

Cost-Driven Hybrid Configuration Prefetching for Partial Reconfigurable Coprocessor,
Ying C hen, Simon Y. Chen

11:50 - 13:20 Lunch Break

13:20 - 14:05 Keynote 2

Programming Models for Reconfigurable Systems,
Satnam Singh, Microsoft

14:05 - 15:05 Dynamic and Partial Reconfiguration II

(Session Chair: M.Santambrogio)

A Reconfiguration Aware Circuit Mapper for FPGAs,
Markus Rullmann, Renate Merker

Miss Ratio Improvement for Real-Time Applications using Fragmentation-Aware Placement,
Ahmed AbulFarag, Hatem El-Boghdadi, Samir Shaheen

Managing dynamic reconfiguration on MIMO Decoder,
Hongzhi Wang, Jean-Philippe Delahaye, Pierre Leray, Jacques Palicot

15:05 – 15:30 Coffee Break

15:30 – 16:30 High Level Synthesis

(Session Chair: E. Bozorgzadeh)

Model and Methodology for the Synthesis of heterogeneous and partially reconfigurable systems,
Florian Dittmann, Marcelo Götz, Achim Rettberg

An Architectural Framework for Automated Streaming Kernel Selection,
Nikolaos Bellas, Sek Chai, Malcolm Dwyer, Dan Linzmeier

High-Level Synthesis of HW Tasks Targeting Run-Time Reconfigurable FPGAs,
Maik Boden, Thomas Fiebig, Steffen Rülke, Jürgen Becker

16:30 – 17:10 Architectures II

(Session Chair: R. Vaidyanathan)

A multi-contexts holographic memory recording system for Optically Reconfigurable Gate Arrays,
Rio Miyazaki, Minoru Watanabe, Fuminori Kobayashi

Code Compression and Decompression for Instruction Cell Based Reconfigurable Systems,
Nazish Aslam, Mark Milward, Ioannis Nousias, Tughrul Arslan, Ahmet Erdogan

17:10 – 17:20 Short Break

17:20 – 18:00 System Specification and Design

(Session Chair: C.Morra)

C++ based System Synthesis of Real-Time Video Processing Systems targeting FPGA Implementation,
Najeem Lawal, Mattias O'Nils, Benny Thörnberg

A Study of Design Efficiency with a High-Level Language for FPGAs,
Zain Ul-Abdin, Bertil Svensson

18:00 – 18:15 Closing Remarks