RAW 2006

13th Reconfigurable Architectures Workshop

April 26 – 27, 2006 Rodos Palace Resort Hotel, Rhodes Island, Greece
http://www.ece.lsu.edu/vaidy/raw06/

Call for Papers

Submission Deadline: October 25, 2005

The 13th Reconfigurable Architectures Workshop (RAW 2006) will be held in Rhodes April 2006. RAW 2006 is associated with the 20th Annual International Parallel & Distributed Processing Symposium (IPDPS 2006) and is sponsored by the IEEE Computers Society's Technical Committee on Parallel Processing. RAW 2006 is one of the major meetings for researchers to present ideas, results, and on-going research on both theoretical and practical advances in Reconfigurable Computing.

Run-Time Reconfiguration & Adaptive Computing: Architectures, Algorithms, Technologies

Run-Time and Dynamic Reconfiguration are characterized by the ability of underlying hardware architectures or devices to rapidly alter (on the fly) the functionalities of its components and the interconnection between them to suit the problem. Key to this ability is reconfiguration handling and speed. Though theoretical models and algorithms for them have established reconfiguration as a very powerful computing paradigm, practical considerations make these models difficult to realize. On the other hand, commercially available devices (such as FPGAs and new coarse-/multi-grain devices) appear to have more room for exploiting run-time reconfiguration (RTR). An appropriate mix of the theoretical foundations of dynamic reconfiguration, and practical considerations, including architectures, technologies and tools supporting RTR is essential to fully reveal and exploit the possibilities created by this powerful computing paradigm. RAW 2005 aims to provide a forum for creative and productive interaction between all these disciplines.

Topics of Interest

Authors are invited to submit manuscripts of original unpublished research in all areas of dynamic and runtime reconfiguration (foundations, algorithms, hardware architectures, devices, systems-on-chip (SoC), technologies, software tools, and applications). The topics of interest include, but are not limited to:

Models & Architectures
- Theoretical Interconnect & Computational Models
- RTR Models and Systems
- RTR Hardware Architectures
- Optical Interconnect Models
- Simulation and Prototyping
- Bounds and Complexity Issues

Algorithms & Applications
- Algorithmic Techniques
- Mapping Parallel Algorithms
- Distributed Systems/Networks
- Fault Tolerance Issues
- Wireless & Mobile Systems
- Automotive Applications
- Infotainment & Multimedia
- Biology Inspired Applications

Design, Technologies & Tools
- Configurable Systems-on-Chip
- Energy Efficiency Issues
- Devices and Circuits
- Reconfiguration Techniques
- High Level Design Methods
- System Support
- Adaptive Runtime Systems
- Organic Computing

Submission Guidelines:

Authors should submit and register their paper by October 25, 2005 through our web-interface that will be accessible after September 1, 2005 at: http://www-raw06.itiv.uni-karlsruhe.de

All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript (not to exceed 8 pages of single spaced text, including figures and tables) or, in special cases, may be a summary of relevant work. Submissions should be in pdf-format (preferred), or alternatively in Postscript (level 2) format. Authors should make sure that the submission can be viewed using ghostscript and will print on standard letter size paper (8.5" x 11"). IEEE CS Press will publish the IPDPS symposium and workshop abstracts as a printed volume. The complete symposium and workshop proceedings will also be published by IEEE CS Press as a CD-ROM disk.

Important Dates:

Manuscript due:	October 25, 2005
Notification of acceptance:	December 17, 2005
Final version due:	January 21, 2006

Organization:

Workshop Chair: Serge Vernalde, IMEC, Belgium (vernalde@imec.be)

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Program Committee (to be confirmed):

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Mark Jones	Virginia Tech	Stamatis Vassiliadis	Delft University of Technology
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