

11th Reconfigurable Architectures Workshop

Monday, 26 April – Tuesday, 27 April, 2004
Eldorado Hotel
Santa Fé, New Mexico, USA
<http://www.ece.lsu.edu/vaidy/raw04/>

1st Call For Papers

Submission Deadline: October 30, 2003
For more information e-mail: info@ipdps.org



The 11th Reconfigurable Architectures Workshop (RAW 2004) will be held at the Eldorado Hotel Santa Fé, New Mexico on Monday, April 26, 2004. RAW 2004 is associated with the 18th Annual International Parallel & Distributed Processing Symposium (IPDPS 2004) and is sponsored by the IEEE Computers Society's Technical Committee on Parallel Processing. RAW 2004 is one of the major meetings for researchers to present ideas, results, and on-going research on both theoretical and practical advances in Reconfigurable Computing.

Run-Time & Dynamic Reconfiguration: Architectures, Algorithms, Technologies

Run-Time and Dynamic Reconfiguration are characterized by the ability of underlying hardware architectures or devices to rapidly alter (on the fly) the functionalities of its components and the interconnection between them to suit the problem. Key to this ability is reconfiguration handling and speed. Though theoretical models and algorithms for them have established reconfiguration as a very powerful computing paradigm, practical considerations make these models difficult to realize. On the other hand, commercially available devices (such as FPGAs and new coarse-grain FPFAs) appear to have more room for exploiting run-time reconfiguration (RTR). An appropriate mix of the theoretical foundations of dynamic reconfiguration, and practical considerations, including architectures, technologies and tools supporting RTR is essential to fully reveal and exploit the possibilities created by this powerful computing paradigm. RAW 2004 aims to provide a forum for creative and productive interaction between all these disciplines.

Topics of Interest:

Authors are invited to submit manuscripts of original unpublished research in all areas of dynamic and run-time reconfiguration (foundations, algorithms, hardware architectures, devices, systems-on-chip (SoC), technologies, software tools, and applications). The topics of interest include, but are not limited to:

Models & Architectures	Algorithms & Applications	Technologies & Tools
<ul style="list-style-type: none"> Theoretical Models (R-Mesh, etc.) RTR Models and Systems RTR Hardware Architectures Optical Interconnect Models Simulation and Prototyping Bounds and Complexity Issues 	<ul style="list-style-type: none"> Algorithmic Techniques Mapping Parallel Algorithms Distributed Systems & Networks Fault Tolerance Issues Wireless and Mobile Systems Automotive Applications, etc. 	<ul style="list-style-type: none"> Configurable Systems-on-Chip Energy Efficiency Issues Devices and Circuits Reconfiguration Techniques High Level Design Methods System support

Submission Guidelines:

Authors should submit per email an electronic version of their work by October 30, 2003 to Serge Vernalde, IMEC, Belgium (vernalde@imec.be) AND register their paper through our web-interface at: <http://www.ece.lsu.edu/vaidy/raw04/>

All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript (not to exceed 8 pages of single spaced text, including figures and tables) or, in special cases, may be a summary of relevant work. Submissions should be in pdf-format (preferred), or alternatively in Postscript (level 2) format. Authors should make sure that the submission can be viewed using ghostscript and will print on standard letter size paper (8.5" x 11").

IEEE CS Press will publish the IPDPS symposium and workshop abstracts as a printed volume. The complete symposium and workshop proceedings will also be published by IEEE CS Press as a CD-ROM disk.

Important Dates:

Manuscript due: October 30, 2003
Notification of acceptance/rejection: November, 2003
Final version due: January, 2004

Organization:

Workshop Chair: Jürgen Becker, Universität Karlsruhe (TH), Germany
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