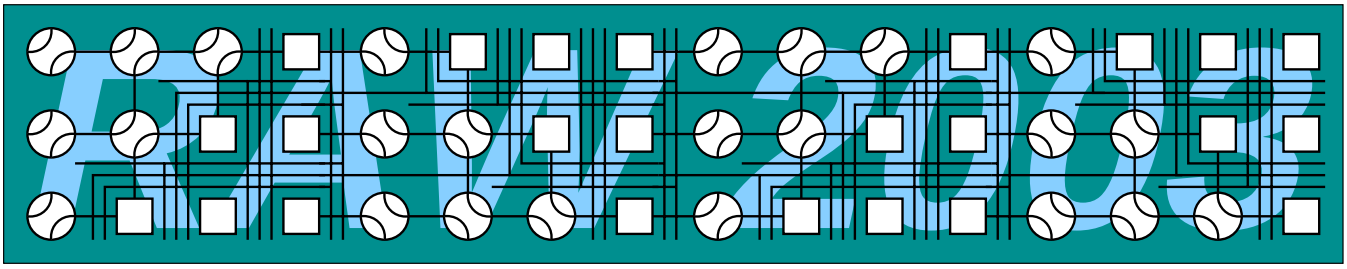
Deadline Extended to Nov 3

Call For Papers



10th Reconfigurable Architectures Workshop (RAW 2003)

Tuesday, April 22, 2003, Nice Acropolis Convention Center, Nice,France

http://www.ece.lsu.edu/vaidy/raw03/

The 10th Reconfigurable Architectures Workshop (RAW 2003) will be held at the Nice Acropolis Convention Center, Nice, France, on Tuesday, April 22, 2003. RAW 2003 is associated with the 17th Annual International Parallel & Distributed Processing Symposium (IPDPS 2003) and is sponsored by the IEEE Computers Society 's Technical Committee on Parallel Processing . RAW 2003 is one of the major meetings for researchers to present ideas, results, and on-going research on both theoretical and practical advances in Reconfigurable Computing.

Main Focus of Workshop

Run-Time & Dynamic Reconfiguration: Architectures, Algorithms, Technologies

Run-Time and Dynamic Reconfiguration are characterized by the ability of underlying hardware architectures or devices to rapidly alter (on the fly) the functionalities of its components and the interconnection between them to suit the problem. Key to this ability is reconfiguration handling and speed. Though theoretical models and algorithms for them have established reconfiguration as a very powerful computing paradigm, practical considerations make these models difficult to realize. On the other hand, commercially available devices (such as FPGAs and new coarse-grain FPFAs) appear to have more room for exploiting run-time reconfiguration (RTR). An appropriate mix of the theoretical foundations of dynamic reconfiguration, and practical considerations, including architectures, technologies and tools supporting RTR is essential to fully reveal and exploit the possibilities created by this powerful computing paradigm. RAW 2003 aims to provide a forum for creative and productive interaction between all these disciplines

Topics of Interest

Authors are invited to submit manuscripts of original unpublished research in all areas of dynamic and run-time reconfiguration (foundations, algorithms, hardware architectures, devices, systems-on-chip (SoC), technologies, software tools, and applications). The topics of interest include, but are not limited to:

Models & Architectures	Algorithms & Applications	Technologies & Tools
• Theoretical Models (R-Mesh, etc.)	• Algorithmic Techniques	• Configurable Systems-on-Chip
• RTR Models and Systems	• Mapping Parallel Algorithms	• Energy Efficiency Issues
• RTR Hardware Architectures	• Distributed Systems & Networks	• Devices and Circuits
• Optical Interconnect Models	• Fault Tolerance Issues	• Reconfiguration Techniques
• Simulation and Prototyping	• Wireless and Mobile Systems	• High Level Design Methods
• Bounds and Complexity Issues	• Automotive Applications, etc.	• System support

Submission Guidelines

Authors should submit by email an electronic version of their work for review **by November 3, 2002** to
Juergen Becker, Universitaet Karlsruhe (TH): becker@itiv.uni-karlsruhe.de
AND register their paper through our web-interface at http://www.ece.lsu.edu/vaidy/raw03/

All manuscripts will be reviewed by at least three members of the program committee. Submissions should be a complete manuscript (not to exceed 8 pages of single spaced text, including figures and tables) or, in special cases, may be a summary of relevant work. Submissions should be in pdf-format (preferred), or alternatively in Postscript (level 2) format. Authors should make sure that the submission can be viewed using ghostscript and will print on standard letter size paper (8.5" x 11").

IEEE CS Press will publish the IPDPS symposium and workshop abstracts as a printed volume. The complete symposium and workshop proceedings will also be published by IEEE CS Press as a CD-ROM disk.

Important Dates

Manuscript due:	November 3, 2002
Notification of acceptance/rejection:	December 5, 2002
Final version due:	January 24, 2003

Organization

Workshop Chair:	Serge Vernalde, IMEC, Belgium	vernalde@imec.be
Steering Chair:	Viktor K. Prasanna, University of Southern California, USA	prasanna@ganges.usc.edu
Program Chair:	Juergen Becker, Universitaet Karlsruhe (TH), Germany	becker@itiv.uni-karlsruhe.de
Publicity Chair:	Ramachandran Vaidyanathan, Louisiana State University, USA	vaidy@ece.lsu.edu

Program Committee

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Oliver Diessel	University of New South Wales, Australia
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Hossam ElGindy	The University of New South Wales, Australia
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George Milne	The University of Western Australia, Australia
Toshiaki Miyazaki	NTT Network Innovation Labs, Japan
Amar Mukherjee	University of Central Florida, USA
Dietmar Mueller	Technische Universitaet Chemnitz, Germany
Koji Nakano	Japan Advanced Inst. of Science & Tech., Japan
Bernard Pottier	Universit de Bretagne Occidentale, France
Michel Renovell	LIRMM, Montpellier, France
Peter Roth	IBM, Germany
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Juergen Teich	University of Paderborn, Germany
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