LSU EE 4755 **Homework 3** **Due: 4 October 2017**

Problem 1: Solve 2016 EE 4755 Final Exam Problem 2, in which timings are requested for individual units, such as a BFA and more complex circuits made from individual units.

In the simple timing model 2-input AND and OR gates each have a delay of 1 unit, and NOT gates have a delay of 0 units. AND and OR gates with more than two inputs have the delay obtained with a reduction tree of 2-input gates. That is, n-input AND and OR gates have a delay of $\lceil \lg n \rceil$ units.

Problem 2: Solve 2016 EE 4755 Final Exam Problem 4, in which the cost of some circuits is to be computed.

In the simple cost model NOT gates have a cost of 0 units and n-input AND and OR gates each have a cost of $n-1$ units. The cost of other gates is the cost of the AND, OR, and NOT gates needed to implement them.