EE 4755—Digital Design Using Hardware Description Languages

Midterm Exam Review

When / Where

Wednesday, 28 October 2015, 11:30-12:20 CDT

2228 Patrick F. Taylor Hall (Here)

Conditions

Closed Book, Closed Notes

Bring one sheet of notes (both sides), 216 mm × 280 mm.

No use of communication devices.

Format

Several problems, short-answer questions.

Resources

Lecture slides and examples used in class: `http://www.ece.lsu.edu/koppel/v/ln.html`

Study Guides

Synthesis: `http://www.ece.lsu.edu/koppel/v/guides/syn.pdf`

Solved tests and homework:. `http://www.ece.lsu.edu/koppel/v/prev.html`

Topics for Exam

Everything up to and including the pipelined multiplier.

Material in lecture slides and homework.

Study Recommendations

Study this semester's homework assignments. Similar problems may appear on the exam.

Study last semester's homework.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for brief hints and to check your own solutions.

Previous Exams

Study 2014 midterm exam.

Study 2014 final exam, but start at Problem 3 and save Problems 1 and 2 for last.

Course Material Areas

Verilog

The System Verilog language, including structural and behavioral code.

Synthesis

How common tools convert Verilog HDLs to hardware.

Digital Design

The functioning of the circuits covered in class.

How to design digital circuits.

Tools

How to run the Verilog and synthesis tools.

Should understand what commands do, but don't have to memorize them.

Verilog Topics and Info

References

The SystemVerilog standard.

Topics

Data types, logic v. wire, vectors, arrays, etc.

Module instantiation, parameters, etc.

`always` and `initial`.

`generate` statements

Elaboration.

Delays and nonblocking assignments.

Event control. (@).

The event queue.

Emphases, Key Skills

Verilog—Key Skills

Given a design in one form, write design in another:

- Explicit Structural
- Implicit Structural
- Synthesizable Behavioral
- Logic Diagram

Use generate statements to interconnect modules.

Synthesis Key Skills

Given Verilog code:

Show inferred hardware (before optimization).

Show expected optimizations.

Logic Design Skills

Given a design, be able to:

Compute Cost

Compute Delay

Synthesis Topics

Difference between inference v. optimization.

Inference of combinational logic.

Inference of registers.

Optimization of combinational logic.

Design goals.

Digital Design Topics

Specific Circuits

Multiplier structure.

Maxrun circuit.

Digital Design Techniques

Pipelining.

Tools

Synthesis (RTL Encounter).

- `read_hdl`, `elaborate`
- `define_clock`
- `synthesize -to_generic`
- `synthesize -to_mapped`
- `report area`, `timing`