EE 4755—Digital Design using Hardware Description Languages

Where/When/Web/RSS

Room 2228 Patrick F. Taylor Hall Monday Wednesday Friday 11:30-12:20 Fall 2014 http://www.ece.lsu.edu/koppel/v/

Who

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Tentative Office Hours: Monday-Friday: 14:00-15:00.

Prerequisites

By Course: EE 3755. By Topic: Logic design, computer organization, programming (C, C++, Java, etc.).

Topics

- EDA Overview: Definitions of typical workflow and tools that are involved.
- Structural Descriptions: Representation of logic levels; primitives; expressions; modules.
- Basic Synthesis Tool Usage: Design targets, timing and area constraints, design tuning.
- Procedural Language Features: Variables and types, procedural constructs, event queue, etc. Testbench coding.
- Behavioral Descriptions: Coding common building blocks. Inference of behavioral code by synthesis tools.
- Design Examples: Coverage of design techniques and features through a medium-sized design.
- Exams and Review: In-class midterm exam, review for midterm and final exams.

Texts

IEEE Standard for SystemVerilog—Unified Hardware Design, Specification, and Verification Language, IEEE 1800-2012. (For a free copy visit

http://standards.ieee.org/getieee/1800/download/1800-2012.pdf.) For those who need to review digital logic and basic Verilog: Brown & Vranesic, "Fundamentals of Digital Logic with Verilog Design" (The text used in EE 2720 and 2730.);

Grading

Homework assignments, including HDL coding assignments, 30%; Midterm Exam, 35%; Final Exam, 35%. Final exam weight may be increased for students who show significant improvement on the final exam.

Late-homework penalty: 10% per day late deducted. Missed-midterm-exam policy: at instructor's discretion either a makeup exam, use final exam grade for midterm grade (i.e., 70% final exam weight), or use zero for midterm grade. Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class.

