Midterm Exam Review

When / Where

Monday, 10 November 2014, 11:30-12:20 CST

2228 Patrick F. Taylor Hall (Here)

Conditions

Closed Book, Closed Notes

Bring one sheet of notes (both sides), 216 mm × 280 mm.

No use of communication devices.

Format

Several problems, short-answer questions.

Resources

Lecture “slides” used in class: `http://www.ece.lsu.edu/koppel/v/ln.html`

Study Guides

Solved tests and homework:. `http://www.ece.lsu.edu/koppel/v/prev.html`

Topics for Exam

Everything before the content addressable memory example.

Material in lecture slides and homework.

Study Recommendations

Study this semester's homework assignments. Similar problems may appear on the exam.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for brief hints and to check your own solutions.

Previous Midterms

Be sure to look at previous midterms and final exams, but note differences in coverage.

Course Material Areas

Verilog

The System Verilog language, including structural and behavioral code.

Synthesis

How common tools convert Verilog HDLs to hardware.

Digital Design

The functioning of the circuits covered in class.

How to design digital circuits.

Tools

How to run the Verilog and synthesis tools.

TCL scripting.

Verilog Topics and Info

References

The SystemVerilog standard.

Topics

Data types, logic v. wire, vectors, arrays, etc.

Module instantiation, parameters, etc.

always and initial.

generate statements

Elaboration.

Delays and nonblocking assignments.

Event control. (@).

The event queue.

Emphases, Key Skills

Verilog—Key Skills

Given a design in one form, write design in another:

Explicit Structural

Implicit Structural

Synthesizable Behavioral

Logic Diagram

Use generate statements to interconnect modules.

Synthesis Key Skills

Given Verilog code:

Show inferred hardware (before optimization).

Show expected optimizations.

Logic Design Skills

Given a design, be able to:

Compute Cost

Compute Delay

Synthesis Topics

Difference between inference v. optimization.

Inference of combinational logic.

Inference of registers.

Optimization of combinational logic.

Design goals.

Digital Design Topics

Specific Circuits

Multiplier structure.

Maxrun circuit.

Digital Design Techniques

Pipelining.

Tools

Synthesis (RTL Encounter).

`read_hdl`, `elaborate`

`synthesis -to_generic`

`synthesis -to_mapped`

`report area`, `timing`

`define_clock`

TCL

Understand how TCL script controls Encounter.

Be able to read TCL code.