Final Exam Review

When / Where

Monday, 8 December 2014, 10:00-12:00 CST

2228 Patrick F. Taylor Hall (Here)

Conditions

Closed Book, Closed Notes

Bring one sheet of notes (both sides), 216 mm × 280 mm.

No use of communication devices.

Format

Several problems, short-answer questions.

Resources

Lecture "slides" used in class: `http://www.ece.lsu.edu/koppel/v/ln.html`

Study Guides

Solved tests and homework:. `http://www.ece.lsu.edu/koppel/v/prev.html`

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Study Recommendations

Study this semester's homework assignments. Similar problems may appear on the exam.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for brief hints and to check your own solutions.

Previous Exams

Be sure to look at previous midterm and final exams, but note differences in coverage.

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Course Material Areas

Verilog

The System Verilog language, including structural and behavioral code.

Synthesis

How common tools convert Verilog HDLs to hardware.

Digital Design

The functioning of the circuits covered in class.

How to design digital circuits.

Tools

How to run the Verilog and synthesis tools.

TCL scripting.

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Verilog Topics and Info

References

The SystemVerilog standard.

Topics

Data types, logic v. wire, vectors, arrays, etc.

Module instantiation, parameters, etc.

always and initial.

generate statements

Elaboration.

Delays and nonblocking assignments.

Event control. (@).

The event queue.

Emphases, Key Skills

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Verilog—Key Skills

Given a design in one form, write design in another:

- Explicit Structural
- Implicit Structural
- Synthesizable Behavioral
- Logic Diagram

Use generate statements to interconnect modules.

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Synthesis Key Skills

Given Verilog code:

Show inferred hardware (before optimization).

Show expected optimizations.

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Logic Design Skills

Given a design, be able to:

Estimate Cost

Estimate Delay

Describe optimizations that the synthesis program is likely to make.

Describe optimizations that the synthesis program ought to make ...
... but that should be double checked.

Describe optimizations that the synthesis program is unlikely to make ...
... and for which the Verilog description should be modified.

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Synthesis Topics

Difference between inference v. optimization.

Inference of combinational logic.

Inference of registers.

Optimization of combinational logic.

Optimization *goals* and optimization *constraints*.

Goals are what to minimize (usually cost).

Constraints are conditions that must be met (usually timing).

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Digital Design Topics

Specific Circuits

Multiplier structure.

Maxrun circuit.

Content-addressable memory (CAM). New!

The Homework 4 stream compressor (`asc_to_int`). New!

Digital Design Techniques

Pipelining.

Multi-cycle operations. New!

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Tools

Synthesis (RTL Encounter).

- `read_hdl`, `elaborate`
- `synthesis -to_generic`
- `synthesis -to_mapped`
- `report area`, `timing`
- `define_clock`
- `external_delay` New!

TCL

Understand how TCL script controls Encounter.

Be able to read TCL code.