

EE 3060: Verilog Independent Study

Syllabus

Where/When/How/URL

Meeting time and places to be arranged. Check the Web page for meeting times and other instructions.

Spring 2002

Check the Web page for registration instructions.

<http://www.ece.lsu.edu/v/>

Who

David M. Koppelman

Room 349 Electrical Engineering Building

578-5482, koppel@ece.lsu.edu, <http://www.ece.lsu.edu/koppel/koppel.html>

Tentative Office hours: Mon 15:00-16:00; Tue & Thr 14:00-15:30 Wed 9:30-10:30.

Prerequisite

Permission of instructor.

What

Drawing wires to connect logic gates may be fun (especially using a cool schematic capture program) when you're working with half a dozen gates but is tedious when working with a larger number of components, say 10^7 . Rather than using a schematic (graphical) representation, real systems are designed using *hardware description languages* (HDLs). Engineers design by writing HDL code, feeding the code to simulators to verify functionality, and feeding the code to synthesizers to complete the design.

The course will cover Verilog, one of two widely used HDLs. (The other is VHDL). Course work will include writing Verilog descriptions of circuits and testbench code, and verifying designs through simulation. The first half of the course will cover Verilog syntax, in the second half students will work on projects, some may be based on material covered in EE 4720.

The course is independent study. Some Verilog material for the first part of the course will be covered in EE 3755, students may want to audit that course. Readings (but not lectures) for more advanced material will also be assigned. The class will meet occasionally (perhaps every two weeks).

Topics

Structural and behavior modeling.

Delay modeling and simulation.

Synthesis and Synthesizable Designs

Projects

Text

Handouts, optional texts: "Modeling, synthesis, and rapid prototyping with the Verilog HDL," Michael D. Ciletti; "Verilog HDL," Samir Palnitkar. Lower-cost texts may be substituted.

Grading

Pass/Fail Grading will be based upon participation in projects and may also include assignments and quizzes.