

EE 7700-1: Computer Microarchitecture

Where/When/How/URL

3129 CEBA Building, Monday Wednesday Friday 12:40–13:30, **Spring 2007**
Call Number 1856, <http://www.ece.lsu.edu/tca/>

Who

David M. Koppelman, Room 349 Electrical Engineering Building
(225) 578-5482, koppel@ece.lsu.edu, <http://www.ece.lsu.edu/koppel>
Office hours: Monday–Friday: 9:00–10:00.

Prerequisites

By Course: Credit or registration in EE 4720 or equivalent.

By Topic: Computer architecture and digital logic must be thoroughly understood. Students must also have a familiarity machine language and C programming and the basics of operating systems.

Topics

- Limit Studies
- Computer Simulation, Instrumentation, and Visualization
- Machine Organizations for Explicit Parallelism (Brief Coverage)
 - Grid, distributed, cluster, multiprocessor (single-core chips), multiprocessor (multi-core chips), simultaneous multithreading (hyperthreading).
- Memory Latency Hiding Techniques
 - Dynamic Scheduling, Store/Load Dependence Prediction
 - Prefetching and address prediction.
 - Pre-Execution
- Critical Path Compression
 - Dynamic Re-compilation, Optimization Caches
 - Value Prediction, Computation Re-Use
 - Master/Slave Speculative Parallelization
- Non-Linear Fetch
 - Out-of-Order Fetch (Multiscalar, IMT, Skipper, etc.)
 - Eager Execution

Topics subject to change.

Text

Papers and other references. (No textbook.)

Grading

35% Midterm Exam • 35% Final Exam • 30% Homework and Projects

Final exam weight may be increased for a student who shows significant improvement on the final exam.

Late assignment penalty: 10% per day late deducted. Missed-midterm-exam policy: at instructor's discretion either a makeup exam, use final exam grade for midterm grade (*i.e.*, 70% final exam weight), or use of zero for midterm grade. Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class.