LSU EE 7700-1 **Homework 1** **Due: 7 March 2007**

In class Wall's limit study on instruction level parallelism and many techniques to exploit ILP were covered. For this assignment simulation results will be searched for examples of execution bottlenecks of various types with respect to Wall's limits and basic processor capabilities. The simulations are of SPECint2000 benchmarks running on dynamically scheduled machines of various types. Each simulation is of a particular machine (say, 8-way superscalar, 256-entry reorder buffer, 3-block per cycle prediction) running a particular benchmark (say, crafty); the simulation results are written to a *dataset file*. The dataset files can be viewed using a visualization tool called PSE.

PSE runs on ECE Linux and Sun machines, (Linux preferred). Follow the instructions for account setup on the course procedures page. The procedures page also has links to some PSE documentation (which might be a bit out of date).

The dataset files for this assignment are located in directory /home/faculty/koppel/pub/ds/2007/batch.sm.0098 which should be accessible from ECE Linux machines. The dataset files are named using *run ids*, view the web page `index.html` to see the benchmark and machine configuration. If your system is set up properly you can view the dataset by clicking the run id.

The simulated machines have the following characteristics:

- Dynamically scheduled. (Out of order execution.)
- Superscalar. Issue (fetch/decode/commit) width (IW) is either 2, 4, 8, or 16 instructions per cycle (depending on configuration).
- Reorder buffer (ROB) size is either 64, 128, 256, or 512 entries.
- Can predict either 1 or 3 blocks per cycle.
- Uses YAGS predictor with 8-branch GHR and 2^{16}-entry PHTs.

Problem 1: Using PSE find regions of execution which exhibit the characteristics described below. Choose any benchmark or configuration that provides an answer. For each region give:

- The benchmark, issue width, rob size, and blocks / cycle.
- The run ID. (For example, sm.98.017).
- The segment number (upper-left hand corner) and cycle number (bottom) in PSE.
- Briefly describe what led you to believe it exhibited the characteristic. Use a sketch of the region for your argument. Even if you take the trouble to print the segment plot, please provide your own sketch that includes only important features.

(*a*) Find a region that is fetch limited due to taken control transfers in a configuration (not benchmark) which has limited fetch capability. (Don't consider regions with mispredictions, that's a different problem.) Find another one in a configuration that has good fetch capability.

(*b*) Find two regions in which the IPC is close to that of the ideal ILP. In one region describe how a modified microarchitecture might allow execution to be faster, beyond the ILP limit. In the other region argue that it would be difficult to do so.