Advanced Superscalar Techniques

Outline
- Limits of Instruction-Level Parallelism
- Eager Execution
- Load/Store Dependency Prediction and Renaming
- Trace Processors
- References

Limits of Instruction-Level Parallelism

From Hennessey and Patterson Section 4.7

Goal: Find issue rate of an ideal processor.

Ideal Processor
- Unlimited number of reservation stations.
- Perfect branch prediction.
- Perfect jump prediction.
- Perfect memory address dependence prediction.

Results:

<table>
<thead>
<tr>
<th></th>
<th>gcc</th>
<th>espresso</th>
<th>liSPEC</th>
<th>fppp</th>
<th>doduc</th>
<th>tomcatv</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction issues</td>
<td>54.1</td>
<td></td>
<td>62.6</td>
<td>17.9</td>
<td>75.2</td>
<td>118.7</td>
</tr>
<tr>
<td>per cycle</td>
<td>100</td>
<td></td>
<td>120</td>
<td>80</td>
<td>140</td>
<td>160</td>
</tr>
</tbody>
</table>

FIGURE 4.38 ILP available in a perfect processor for six of the SPEC benchmarks.

Effect of Window Size

Use pretty-good-but-not-ideal processor:
- 2048-instruction window.
- 64-way superscalar.

Branch Predictors

Perfect: all branches predicted.

Selective History: McFarling's gshare/bimodal predictor, 2^13-entry tables for gshare, bimodal, and selector.

One-Level: 512-entry BHT.

Static: base predictions on a profile run.

None: No branch prediction.

FIGURE 4.40 The effect of window size shown by each application by plotting the average number of instruction issues per clock cycle.
### Number of Physical Registers

Vary physical registers. (Effect similar to varying reservation stations.)

![Figure 4.42: The effect of branch-prediction schemes sorted by application.](image)

![Figure 4.44: The reduction in available parallelism is significant when fewer than an unbounded number of renaming registers are available.](image)

### Memory Dependency Effects

![Figure 4.46: The effect of varying levels of alias analysis on individual programs.](image)

### Window Size for “Realizable” Processors

**Realizable Processor**
- 64-way superscalar.
- gshare/bimodal predictor with 1024-entry tables.
- Perfect load/store dependency analysis.
- Register renaming with 64 additional registers.
FIGURE 4.48 The amount of parallelism available versus the window size for a variety of integer and floating-point programs with up to 64 arbitrary instruction issues per clock.

References

Limits of Instruction-Level Parallelism

Material (and graphs) from text, section 4.7:


Source used for textbook.


(Selective) Eager Execution


References, Continued

Load/Store Dependence Prediction and Renaming

Store barrier cache: in load/store queue wait only for stores that had caused dependency violations.


Predicting load/store dependencies using store sets. Includes performance of systems that predict all pairs dependent and no pairs dependent.


Forwarding data from store to load if dependency predicted.


Trace Processors

Description of trace processor using several aggressive techniques, including value prediction. Includes comparison with a higher cost system: a superscalar processor with similar prediction capabilities and issue bandwidth.


Description of trace processor and comparison to a more limited superscalar processor.