

Title: Core Discovery in Internet Multicast Routing Protocol

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Abstract:

This paper presents modifications to the *Core Based Tree* (CBT) multicast routing protocol for selecting a set of optimal routers in a domain as core routers for a multicast group. Currently, there is no mechanism in CBT to locate core routers in an automatic fashion, adapting to network changes. Our proposed modifications help configure an optimal router as core based on three heuristics: *Center of Members* (CBT-CoM), *Center of Sources* (CBT-CoS), and *Center of Sources and Members* (CBT-CoSM). We next evaluate and compare the performance of these heuristics using network dynamics. For this, an implementation based on the simulation package NSv2 [8] and a topology generation package GT-ITM [9] is considered.

Title: Analysing Packetized Voice and Video Traffic in an ATM Multiplexer

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Abstract:

This paper considers packetized voice and video traffic incoming to an ATM multiplexer. Each voice and video source is approximated by a two-state Markov-modulated Poisson process (MMPP(2)). We propose a method based on the asymptotic results of a renewal process to obtain the equivalent MMPP(2) parameters. The integrated voice and video sources are modelled by the superposition of two MMPP(2) processes, denoted MMPP(4). The analysis of the superposed traffic in terms of buffer occupancy, cell loss probability and delay is performed with an MMPP(4)/ER(k)/1/B queuing model considering different buffer sizes and numbers of sources. Results of the proposed method are also compared with those of Heffes and *Lucantoni* (*IEEE J. Select. Areas Commun.*, SAC-4, 356-368 (1986)) and with a Poisson approximation.

Title: Comparison of genetic algorithms and simulated annealing for cost-minimization in a multisensor system

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Abstract:

Many sensor fusion systems combine redundant inputs to increase information reliability. In spite of this, few studies show how to choose redundant sensors for these systems. We find sensor configurations that minimize system cost while ensuring system dependability. Dependability is the generic term for system reliability and availability. Given many types of sensors, all fulfilling system operational requirements, but with

different dependability and per item cost, heuristic search methods are used to find minimum cost configurations. Our main contributions are deriving the optimization problem, showing the search can be limited to a multidimensional surface, deriving a fitness function, and providing an efficient algorithm for computing dependability bounds. Two heuristics, genetic algorithms and simulated annealing, are proposed as methods. Experimental results show cost savings of up to 20% compared to systems with only one component type.

Title: Comparison of video conference realization schemes

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Abstract:

In this paper, we investigate the issue of how *multiparty-to-multiparty communication should be realized*. In order to quantify the different techniques, we examine the network-layer (bandwidth and buffer) allocations of four models for realizing multiparty-to-multiparty communication. An example application considered in this paper, where such communication will be needed, is video conferencing based on MPEG video streams. Analytical comparisons are carried out based on actual data obtained from empirical measurements of the source characteristics of MPEG video (determined to be a 40 state Markov modulated fluid source). Our results show that in order to minimize bandwidth and buffer(network-layer resources) allocations, we must exploit the effect of statistical multiplexing by using shared buffers for such multiparty-to-multiparty communication. Using these results we identify the best technique for multiparty-to-multiparty communications.

Title: Hyperneural Network--An Efficient Model for Test Generation in Digital Circuits

Author(s):

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Abstract:

This paper considers the problem of applying neural network for logic circuit testing and proposes an efficient method based on *hyperneural network* (HNN). The HNN uses an energy function that not only considers binary relations but also captures all higher order relations among N neurons. We illustrate the hyperneural concept using two formulations. First, a constraint energy function is defined and the gate model is obtained. Second, the Hopfield network is reformulated to generate the gate level hyperneural model. The gate level HNNs are used to give a mathematical form to the digital circuit that, in turn, requires optimization techniques to solve the test generation problem. We have used ISCAS'85 benchmark circuits to illustrate the method. Results are compared with those obtained from PODEM, MODEM, and FAN.

Title: Evaluating FTRE's for Dependability Measures in Fault Tolerant Systems

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Abstract:

In order to analyze dependability measures in a fault tolerant system, we generally consider a nonstate space or a state space type model. A fault tree with repeated events (FTRE's) presents an important strategy for the nonstate space model. This paper deals with a conservative assessment to complex fault tree models, henceforth called as CRAFT, to obtain an approximate analysis of the FTRE's. It is noncutset, direct, bottom-up approach. It uses failure probability or failure rate as input and determines a bound on the probability of occurrence of the TOP event. CRAFT generalizes the concept of a cutting heuristic that obtains the signal probabilities for testability measurement in logic circuits. The method is efficient and solves coherent and noncoherent FTRE's having AND, OR, XOR, and NOT gates. In addition, CRAFT considers M/N, priority AND, and two types of functional dependency, namely OR and AND types. Examples such as the C_m^* architecture and a fault-tolerant software based on recovery block concept are used to illustrate the approach. The paper also provides a comparison with approaches such as SHARPE, HARP, and FTC.