Electrical & Computer Engineering

S E M I N A R

Louisiana State University

Software Tools for Modeling and Simulation of On-Chip Communication Architectures

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Abstract—Recent years have seen a proliferation of complex System-on-Chips (SoCs) that are composed of multiple processor cores and other Intellectual Property (IP) cores. These cores are connected by the on-chip communication architecture (OCA).

In this talk, I will introduce a retargetable simulation framework where SoC designs, including the OCAs, can be constructed easily and evaluated efficiently and faithfully. The modeling and simulation platform is based on an existing formal concurrency model, the Operation State Machine (OSM). The OCA models are constructed faithfully by explicitly modeling both the operation concurrency and the microarchitecture concurrency. Coupled with existing Processor Element (PE) models, this framework is capable of synthesizing a multiprocessor cycle-accurate SoC simulator from a system-level description. The case studies aim to examine and evaluate this framework. The targeted architectures include a router-based packet switching on-chip communication network and an industry-standard on-chip bus architecture. Experimental results show that this framework can significantly reduce the design turn around time and improve design reuse in the early stages of SoC design.

Xinping Zhu is currently a Ph.D. candidate in Electrical Engineering at Princeton University. He received his B.S.E. degree in Automation from Tsinghua University, Beijing, in 1999. His research focuses on developing modeling and simulation tools for advanced multiprocessing general purpose and embedded processors, with emphasis on the on-chip communication architectures.

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