Electrical & Computer Engineering

S E M I N A R

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Interactions Between Architecture Design and Lower Level Design

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Abstract—My research has explored the interactions between architecture design and lower level design in order to facilitate both design and verification processes. In the contemporary design process, a problem with the widely used flip-flop insertion method for interconnects is that it is not aware of the microarchitecture constraints. Therefore I have used a statistical method to quantify each interconnects impact on microarchitecture, which was later used as the constraints in the floor planning process. In this manner, I have achieved a design with optimal balance among architecture performance, interconnects latency, and the area of the layout. In the verification process, test vectors generated from the architecture/system verification have been used as inputs for RTL simulations for debugging. However the test vectors generated were not optimized and thus resulted in unreasonable simulation time. To optimize the test vectors generation, I have proposed both a single heuristic algorithm and a multiple simultaneous heuristics algorithm. Both algorithms have been proven to be efficient in discovering different types of bugs for Cray X1 and Stanford DASH cache coherence protocols. I have also proposed a novel memory structure with flexible sequential and random access modes for embedded systems, and conducted research in exploiting the prefetching effect of speculative execution in a multithreaded architecture.

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