Electrical & Computer Engineering

S E M I N A R

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A Highly Configurable Cache Architecture for Embedded Systems

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Abstract—Energy consumption is a major concern in many embedded computing systems. Several studies have shown that cache memories account for about 50% of the total energy consumed in these systems. The performance of a given cache architecture is determined, to a large degree, by the behavior of the application executing on the architecture. Desktop systems have to accommodate a very wide range of applications and therefore the cache architecture is usually set by the manufacturer as a best compromise given current applications, technology and cost. Unlike desktop systems, embedded systems are designed to run a small range of well-defined applications. In this context, a cache architecture that is tuned for that narrow range of applications can have both increased performance as well as lower energy consumption. I introduce a novel cache architecture intended for embedded microprocessor platforms. The cache has four software-configurable parameters that can be tuned to particular applications. First, the cache's associativity can be configured to be direct-mapped, two-way, or four-way set associative, using a novel technique we call way concatenation. Second, the cache's total size can be configured by shutting down ways. Third, the cache's line size can be configured to have 16, 32, or 64 bytes. Finally, a victim buffer can be turned on or off. A study of 23 programs drawn from Powerstone, MediaBench and Spec2000 benchmark suites shows that the configurable cache tuned to each program saved energy for every program compared to a conventional four-way set-associative cache as well as compared to a conventional direct mapped cache, with an average savings of energy related to memory access of over 40%.

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