Scaling High-Speed Shared-Memory Switch Fabric Buffers

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Shared-memory switch fabrics are a popular choice among commercial switch vendors and are used in many high-speed routers. They can easily emulate output-queued architectures achieving optimal delay-throughput performance. Furthermore, because of statistical sharing of the buffer space they make efficient use of memory and can be economically implemented on a single VLSI chip. However, due to this single-chip implementation, typically, the buffer size in these architectures is small. In cases of bursty or unbalanced traffic buffer overflow can occur resulting in head-of-line blocking and throughput loss. Due to this limitation input queuing together with complex scheduling algorithms to resolve output contention are needed in order to prevent buffer overflow.

In this talk we first present an overview of shared-memory switch fabrics and their application in high-speed routers. Next we present a novel approach to expanding the buffer size in a shared memory switch through external buffer space. Utilizing this two-tier buffering mechanism we present a two-level scheduling algorithm whose complexity is considerably lower than that of traditional input scheduling algorithms. Our approach easily provides differentiated qualities of service to different traffic classes while maintaining high throughput across the switch fabric.

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