MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

AUTOMATIC CONTROL TOPICS

A. Basic Tools

Laplace, Z transforms: basic properties, use in solving linear differential/difference equations, application to system analysis, transfer functions. Fourier transform, Fourier series: basic properties, application to signal analysis, frequency response, spectral energy density.

B. Basic Concepts

Linearity, time invariance, causality, difference and differential systems, linearization, signal-flow and block diagrams, BIBO and asymptotic stability.

C. Classical Control

Transient and steady state analysis and performance indicators, pole location, sensitivity; frequency domain analysis, phase and gain margins; Nyquist stability, Routh-Hourwitz criterion, root locus, lead and lag compensator design, PID control; pole placement with fractional controllers.

D. Sampled Data Systems

Basic A/D and D/A conversion, sampling theorem. Discretization of continuous time systems, deadbeat control.

E. State Space Control for Continuous and Discrete Time Systems

State and state equations, transition matrix, solution of state equation. Realization, controllability and stabilizability, observability and detectability, Lyapunov stability, state feedback and pole placement, asymptotic observers, state feedback with observers.

Representative References

1. C-T. Chen, *System and Signal Analysis*, Saunders College Publishing.
2. B.C. Kuo, *Automatic Control Systems*, Prentice Hall.
3. G.F. Franklin, J.D. Powell, A. Emami-Naeini, *Feedback Control of Linear Systems*, Addison Wesley.
4. G.F. Franklin, J.D. Powell, M.L. Workman, *Digital Control of Dynamic Systems,* Addison Wesley.
5. K. Ogata, *Discrete-time Control Systems*, Prentice Hall.
6. W.L. Brogan, *Modern Control Theory*, Quantum Publishers, Inc.
7. T. Kailath, *Linear Systems,* Prentice Hall.
8. K. Ogata, *Modern Control Engineering*, Prentice Hall.
9. C. T. Chen, *Linear system Theory and Design*, 3rd Ed., Oxford University Press, 1999.

M.S. Comprehensive /Ph.D. Qualifying Exam

Communication and Signal Processing Topics

Probability Theory and Random Processes
Basic concepts in probability theory; stationarity and wide sense stationarity of random processes, power spectral density, linear filtering of random processes, minimum mean squared error estimation, Gaussian and Poisson random processes.

Signals, Systems, and Digital Signal Processing
Continuous time and discrete time signals and systems: fundamental concepts, system properties (causality, stability, time invariance, etc.); time and frequency domain characterization of discrete and continuous time signals and systems; transform domain techniques; sampling and reconstruction; sampling rate conversion, frequency-domain analysis, aliasing and Nyquist rate concepts; discrete Fourier Transform and FFT algorithms; design and implementation of FIR and IIR filters.

Analog Communication
Amplitude modulation techniques; frequency and phase modulation techniques; sampling, quantization; pulse code modulation (PCM); effect of noise on continuous wave and PCM systems.

Digital Communication
Signal space representation; baseband representation of bandpass signals and systems; maximum likelihood (ML) detection and estimation; optimum receiver principles. performance of optimum receivers; differential, partially coherent and non-coherent detection of signals; bandwidth efficiency and power efficiency; receiver design and performance analysis of digital modulation schemes in fading channels; linear block codes and their decoding strategies, hard decision and soft decision decoding.

Representative References

1. Simon Haykin, *Communications Systems*, (Wiley).
2. J. G. Proakis and M. Salehi, *Communication Systems Engineering, 2nd Edition*, Prentice Hall.
3. J. G. Proakis, *Digital Communication*, 4th Edition, McGraw-Hill, 2000.
4. J. M. Wopzencraft and I. M. Jacobs, *Principles of Communication Engineering*, John Wiley & Sons, New York, 1965.
5. Henry Stark and John W. Woods, *Probability and Random Processes with Applications to Signal Processing, 3rd Edition.* Prentice-Hall.
6. *Probability, Random Variables, and Stochastic Processes*, A. Papoulis, 3rd edition, McGraw-Hill, 1991.
7. S. K. Mitra, *Digital Signal Processing*, 3rd edition, McGraw-Hill.
8. A. V. Oppenheim and R.W. Schafer, *Discrete-time Signal Processing*, Prentice-Hall.

MS COMPREHENSIVE / PHD QUALIFYING EXAM

COMPUTER ENGINEERING TOPICS

Appearing below is an outline of topics which computer-area questions will be based on. Most of the topics clearly fall into one of the three question areas, Hardware, Software, and Applications, but questions in one area can draw on topics from other areas. For example, the solution to an algorithm (software) question might require knowledge of cache organization (hardware).

Topics described with "Proficiency in" (or similar wording) must be understood very well, as though you were going to take a test in a course covering the topic. Topics described using "Competence with" (or similar wording) must be understood well enough to solve problems or answer substantive questions, however definitions or other background might be provided as part of the question. This information should help students that know the material make a quick start solving the problem. For topics listed under "Familiarity with" students should have a basic background in the area, including basic terminology, but need not know many specifics. For these problems a greater amount of background will be provided, enough so that a good student might be able to solve them without having taken any courses covering the topic.

Logic Design

Proficiency with combinational and sequential logic theory at EE 2720 and EE 2730 level, including Boolean algebra and basic minimization techniques. Proficiency in designing basic combinational and sequential circuits.

Computer Arithmetic

Proficiency with signed integer representations and with full adder and carry look-ahead adder designs. Competence with basic integer multiplication and division circuits. Competence with floating-point (FP) representations, including IEEE 754, and with FP arithmetic. Familiarity with modular and residue arithmetic.

Computer Instruction-Set Architecture (ISA) and Microarchitecture

Proficiency with 5-staged pipelined RISC (e.g., MIPS) implementations, including design rationale, direct and bypassed data paths, control signals, and relationship between implementation and instructions. Competence in assembly language programming, including RISC instruction sets. Competence with instruction set design issues, including memory addressing modes, and the variety of jumps & branch instructions. Familiarity with interrupts, traps, and exceptions. Familiarity with pipeline depth and superscalar width issues. Familiarity with caches and branch prediction techniques.

Computer Communication Networks

Competence with basic switching and multiplexing techniques. Familiarity with network layers and protocol stacks, ARQ protocols, error detection and correction. Familiarity with Internet addressing and routing standards and techniques. Familiarity with network reliability, availability, structural reliability terminology and techniques.

Algorithms and Data Structures

Proficiency with basic data structures (including arrays, stacks, linked lists, trees), basic algorithms (including binary search, merge sort, tree searches), memory content and layout of numbers, pointers, arrays, and structures complexity analysis of algorithms. Competence with advanced data structures (including hash tables, graph representations), algorithmic paradigms (including divide and-conquer, greedy, dynamic programming) and analysis techniques (including recurrence relations, amortized analysis). Familiarity with computational complexity and intractability randomized, online and approximation algorithms.

Parallel and Distributed Computing

Competence in major parallel system organization topics including hardware organizations (CPU & network), parallel program organizations (processes, tasks, or threads), communication models (message passing or shared memory). Competence with metrics for analysis of performance including speedup, efficiency, time complexity, and space complexity. Competence with use and implementation of basic synchronization primitives and constructs including compare & swap, atomic memory operations, semaphores, and barriers. Competence with basic parallel algorithms including reduction, sorting, leader election, graph algs, etc. Competence with common interconnects including bus, crossbar, mesh, hypercube networks.

Familiarity with other interconnects including Log n stage networks (e.g., omega), Clos and Benes networks.

Operating Systems and Compilers

Competence with coordination concepts, constructs, and issues, including multiple-process access to shared structures, mutual exclusion, and deadlock. (See also basic synchronization topics under Parallel and distributed computing.) Competence with basic memory management issues including virtual and physical addresses and their rationale virtual to physical address translation techniques, page swapping basics. Competence with program compilation techniques, including control-flow and data-flow program representations, dependencies and dependence testing, common optimizations, and common program transformations.

Computer Vision and Image Processing

Proficiency in geometric and radiometric image formation. Proficiency in image segmentation, enhancement and restoration techniques. Competence in image compression and morphological image processing. Familiarity with pattern recognition techniques.

Logic Testing and Reliability

Familiarity with fault models, including the stuck-at model.

MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

ELECTRONICS ENGINEERING TOPICS

A. Circuits

Circuit applications of diodes. Circuit applications of BJT, MOSFETs and JFETs in linear and digital circuits. Linear applications include amplifiers, oscillators, differential amplifiers and operational amplifiers. Applications of ideal operational amplifiers. Digital applications include internal operation of standard logic gates used as building blocks in logic families such as TTL, ECL, NMOS and CMOS.

B. Devices

Basics of carrier transport in semiconductor materials, physics of p-n junction diodes, bipolar and field effect transistors. Derivation of terminal current-voltage characteristics of discrete devices, large and small signal models. Basic physics of photonic devices. Basic integrated circuit technology.

C. Fields

Static fields, Maxwell's equations, propagation through istropic medium, reflections and basic antenna theory.

Representative References

1. M.N. Horenstein, *Microelectronic Circuit and Devices*, Prentice Hall.
2. Mitchell & Mitchell, *Introduction to Electronic Design*, 2nd Ed., Prentice Hall.
3. Gray & Mayer, *Analysis and Design of Analog Integrated Circuits*, 3rd Ed., John Wiley.
4. D. A. Hodges, H. G. Jackson and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits in Deep Submicron Technology*, 3rd Ed., McGraw-Hill.
5. B. Streetman, *Solid State Electronic Devices*, 3rd Ed., Prentice Hall.
6. J.P. McKelvey, *Solid State and Semiconductor Physics*, Harper & Row.
7. Shen, *Applied Electromagnetics*, 2nd Ed., Prindle-Weber-Schmidt.

COMPREHENSIVE MS/QUALIFYING PH.D. EXAM

POWER ENGINEERING TOPICS

A. Electric Machinery

Maxwell's equations; analysis of simple electromechanical devices using Maxwell's equations; synchronous machines, voltage behind reactance model, Park transformation, d,q equations; exact and approximate equivalent circuits of single-phase transformers, nonlinear effects; modeling and calculation of its parameters of transmission lines; modeling and analysis of direct current and induction machines.

B. Power Systems

Per-unit calculations; symmetrical components; sequence impedances of transformers, synchronous machines and induction motors, sequence impedances and capacitances of transmission lines; sequence networks for fault analysis; shunt faults (3-phase, LG, LLG, LL faults); series faults (1LO, 2LO); power flow equations, (Decoupled) Newton-Raphson, Gauss/Gauss-Seidel methods; optimal dispatch with/without line losses; transient stability, swing equation, equal area criterion, effect of clearing time; low-frequency oscillations, supplementary excitation/governor control; linear optimal stabilization.

C. Power Electronics

Fourier series of nonsinusoidal voltages and currents; analysis of circuits with nonsinusoidal voltage and current waveforms, nonsinusoidal active and apparent powers; single-phase and three-phase rectifiers, controlled AC/DC converters, DC/DC converters, inverters.

Representative References

1. R.D. Schultz & R.A. Smith, *Introduction to Electric Power Engineering,* John Wiley, 1988.
2. V. DelToro, *Electric Power Systems*, Prentice Hall, 1992.
3. P.M. Andersen, *Analysis of Faulted Power Systems*, The Iowa State Univ. Press, 1983.
4. Y.N. Yu, *Electric Power System Dynamics*, Academic Press, 1983.
5. M.H. Rashid, *Power Electronics*, Prentice Hall, 1988.
6. N. Mohan, T.M. Undeland, W.P. Robbins, *Power Electronics*, John Wiley, 1989.

LOUISIANA STATE UNIVERSITY
Division of Electrical & Computer Engineering

Exam ID: **Sp-215-00**

Duration: 4 Hours

MS COMPREHENSIVE / PhD QUALIFYING EXAM — Spring 2015

- The exam consists of 40 QUESTIONS divided in eight groups of five questions:

COMPUTER	ELECTRONICS	POWER	SYSTEMS
Hardware	Circuits and Systems		Automatic Control
Software	Physical Electronics		Communications & Signal Processing
Applications			

- Each student must answer **SIX (6) QUESTIONS**:

  PhD: **5 questions** from any of the groups in **THEIR DECLARED MAJOR AREA**. The **(6th) sixth question** can be from any group.

  MS: **ANY** six (6) questions.

- During the Exam:

1. Turn your cell phone off or on vibrate mode.
2. **Cell phone use is NOT PERMITTED** during the exam, **including the calculator.**
3. You are permitted to use an **ECE provided calculator only.**
4. You can use a pen or pencil for the exam.
5. **DO NOT write your name or LSU ID on any test materials**. You have been given an Exam ID. If you use your name or LSU ID on any test materials, IT WILL NOT BE GRADED.
6. Extra answer sheets and scratch paper are provided by the exam proctor.
7. DO NOT write on the question booklet or the folder.
8. DO NOT un-staple the exam.
9. Use a SINGLE SIDE of the paper for your answers.
10. Start each new problem on a NEW answer sheet.
11. Write the problem number ON EACH ANSWER SHEET (hardware 1, power 3, etc.)
12. Number multiple page answers in sequence (Power 3: pg 1 of 4, Power 3: pg 2 of 4, etc.)
13. The **test proctor cannot answer any questions** about the content of the exam. If you believe that the problem is not clear or is in error, write the assumptions or corrections; then work the problem completely.

- After The Exam:

1. Put completed **answer sheets that you wish to be graded IN THE MANILA ENVELOPE** provided, and clasp it.
2. **NOTHING OUTSIDE OF THE ENVELOPE WILL BE GRADED**, no exceptions.
3. Put the test booklet and ALL other un-used, scribbled on or otherwise un-gradable answer sheets in the test folder.

****IMPORTANT** CIRCLE THE SIX (6) PROBLEMS THAT YOU WISH TO BE GRADED!!**

Computer - *Hardware*	1	2	3	4	5
Computer - *Software*	1	2	3	4	5
Computer - *Applications*	1	2	3	4	5
Electronics - *Circuit & Systems*	1	2	3	4	5
Electronics - *Physical Electronics*	1	2	3	4	5
Power	1	2	3	4	5
Systems - *Automatic Control*	1	2	3	4	5
Systems - *Communications & Signal Processing*	1	2	3	4	5

Because they represent unsigned integers in binary, conventional processors can quickly perform operations like $r2^i$ and $\lfloor r2^{-i} \rfloor$, where r is the contents of a register and i is a small value. Suppose it were necessary to quickly perform operations such as $r3^i$ and $\lfloor r3^{-i} \rfloor$. Conventional processors would have to resort to time-consuming multiply and divide instructions. These operations could be quickly performed if the underlying integer representation was in radix 3 (ternary) rather than in radix 2 (binary). Consider a CPU that keeps integers in a binary-coded ternary (BCT) representation. The representation is stored in conventional two-state logic but each ternary digit is encoded using two bits.

(*a*) Design an n-ternary-digit adder for such integers (which are represented using $2n$ bits) using basic logic gates and binary full- and half-adders. The design should be in the form of a ripple adder adapted to BCT so that it takes $O(n)$ time and uses $O(n)$ hardware.

(*b*) Design propagate and generate circuits for the BCT adder that can be used to construct a carry lookahead BCT adder.

Let $S = \{s_1, s_2, \cdots, s_z\}$ be a set of binary strings of maximum length n. For any string s_i of length $\ell \leq n$ and any integer $1 \leq \alpha \leq \ell$, its α-prefix is the string consisting of the first α bits of s_i. If $\alpha > \ell$, then the ℓ-bit string does not have an α-prefix.

For $1 \leq \alpha \leq n$, let $k = k_1 k_2 \cdots k_\alpha$ be an α-bit binary string called the *key*. (Note that α should not be considered fixed as it could be different for different instances of the problem.) This question involves finding the longest string(s) in S whose α-prefix equals the key. In this problem we will call these string(s), the *longest string(s) of the key*. There could be 0, 1 or multiple longest strings for a given key.

Answer the following questions. All answers must be justified.

(a) Let $S = \{0, 11, 110, 1101, 1111\}$. Find all longest string(s) of S with the following key k as prefix.

(i) $k = 110$

(ii) $k = 01$

(iii) $k = 11$.

(b) For this part assume that for any given key the longest string, if it exists, is unique. Design a hardware module to find the longest string in S for any given k.

Assume that the key is input through a $O(n)$-bit register and that the set S is stored in a bank of $O(n)$-bit registers. The output is a $O(n)$-bit longest string or an indication that no such string exists. You can also assume that the gates used in your design allow unbounded fan-in and fan-out.

Speed should be the main objective of your design. For two equally fast solutions choose one with less hardware cost. Find the order of time needed for your solution.

(c) How would you approach the problem if there could be multiple longest strings for a given key. Assume here that the lexicographically earliest string is output in case of multiple matches.

Computer Hardware 1 **Fall 2013**

This question is regarding to cache design.

(a) For the same cache size, is it possible for a direct-mapped cache having a better hit rate than a fully associative cache? If so, give an example for the access pattern or the program using the caches; if not, justify the reason.

(b) For the same cache with different replacement policies, is it possible for the cache with the least-recently-used (LRU) policy having a better hit rate than the optimal (OPT) replacement policy? If so, give an example for the access pattern; otherwise, explain why not?

(c) For a dual-core processor, there is a shared last level cache between the two cores. Two threads (T1 and T2) can run either individually or simultaneously. When the threads running individually, the last level cache hit ratio for the two threads (T1 and T2) are H1 and H2 respectively. When the threads running simultaneously, the last level cache hit ratio for the two threads (T1 and T2) is H1' and H2' respectively. Is it possible for H1' > H1 and H2' > H2? If yes, list an example for the access patterns or write the programs; otherwise, justify your answer.

Usually, we have two policies for memory disambiguation in an out-of-order executed processor: (1) a conservative solution is stalling a load instruction and its dependent instructions until the early store's address generation; (2) another alternative is predicting the memory dependence between loads and earlier outstanding stores. Memory dependence prediction allows loads to bypass earlier stores if no dependence is predicted. Otherwise, if dependence is predicted, load values can be forwarded from the latest earlier stores without cache access. At the commit stage of stores, the processor check correctness of predictions, if not, loads and their dependent instructions would be re-executed.

Now consider a two-issue, out-of-order execution pipeline with following stages: Instruction Fetch (IF), Decode (ID), Issue (IS), Execution / Address Generation (EX), Write Result (WR), Commit (CT). There are two integer ALU units, two load/store units and one MUL unit.

For the following code section, the EX stage for MUL instructions requires 10 cycles. All other instructions' EX stages have only 1 cycle. Please note that SW instructions only write cache in CT stage.

```
1. MUL    R2, R11, R12
2. SW     R1, 0(R2)
3. LW     R3, 20(R4)
4. ADD    R5, R3, R6
5. LW     R7, 100(R8)
6. SUB    R9, R7, R8
7. ADDI   R10, R5, 20
```

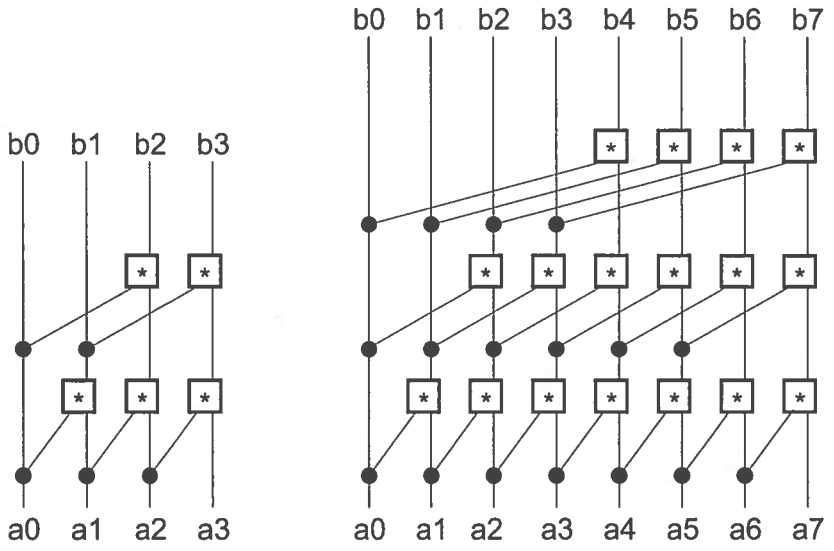
(a) If this pipeline employs the policy (1) mentioned above for memory dependence, show execution steps with timing for the above code section.

(b) If this pipeline employs the policy (2) mentioned above for memory dependence, the memory dependence predictor predicts that there is no dependence for both loads. Two loads (inst. 3 and 5) are executed without stalls. However, after the store address generation, instruction 3 has a true dependence with instruction 2 but instruction 5 doesn't have, show execution steps with timing for the above code section.

(c) Design a memory dependence predictor. The predictor would provide two predictions: dependence, no dependence. Draw a diagram for your design and specify the circumstances for each prediction.

Computer Hardware 4 **Fall 2013**

Let $*$ be any associative binary operation. The *prefix computation* (with respect to $*$) on an array $A = \langle a_0, a_1, \cdots, a_{n-1} \rangle$ produces a second array $B = \langle b_0, b_1, \cdots, b_{n-1} \rangle$, where $b_i = a_0 * a_1 * \cdots * a_i$, for any $0 \leq i < n$. The figure below shows prefix computation circuits for $n = 4$ and 8. In these figures, each box represents hardware for applying $*$ to its two inputs.



(a) Draw a similar prefix computing circuit for 16 inputs.

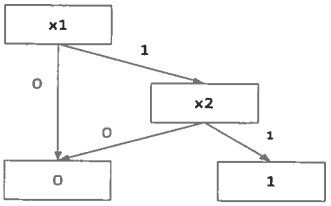
(b) Adapt the given circuit for 8 inputs to work for 5 inputs.

(c) Describe the circuit for the general case of $n = 2^k$ inputs, and prove that it correctly performs the prefix computation.

(d) Observe that adding 1 to an n-bit number amounts to complementing all lower order bits up to the first 0. For example, $10110\ 0111111 + 1 = \overbrace{10110}^{\text{unchanged}}\ \underbrace{1000000}_{\text{complemented}}$.

An n-bit binary counter counts up from 0 to $2^n - 1$ and then back to 0. Describe how a fast prefix computing circuit can help build a fast counter.

(a) "In the field of computer science, a binary decision diagram (**BDD**) or a propositional directed acyclic graph (PDAG) is a data structure that is used to represent a Boolean function The data structure is created using the *Shannon expansion* where a switching function is split into two sub-functions (cofactors) by assigning one variable (cf. *if-then-else normal form*). [Wikipedia]." For example, the BDD for an AND gate with inputs x1 and x2 is as follows:



BDD for a 2-input AND gate

Using this concept, show the BDD for a (i) 2-input OR gate with inputs x1 and x2 and (ii) 1-bit Full Adder with inputs A_i, B_i, and C_{in} and outputs S_i and C_{out}.

(b) In the figure shown above (BDD for a 2-input AND gate), if each event (x_i as 1 or 0) is equally likely, find the probability of (a) output being 1 and (b) output being 0. What will happen to (b) if the probability of x_i being 1 changes to ¾ ?

We want to run a multi-task application on a square mesh of cores, where the mesh has size $m \times m$, the application with $n \leq m^2$ tasks, and we can map at most one task to each core. For an application with multiple tasks, let a task graph for that application contain a vertex v_i for each task t_i and an edge (v_i, v_j) for each pair of communicating tasks t_i and t_j. Edge (v_i, v_j) has weight $w(v_i, v_j)$ equal to the number of bits communicated between tasks t_i and t_j. If core c_x handles task t_i and core c_y handles task t_j, then the communication energy for this pair of tasks is $w(v_i, v_j)$ times η (a bit-energy constant) times the Manhattan distance between c_x and c_y. (The Manhattan distance is the magnitude of the difference of the row indices plus the magnitude of the difference of the column indices.) Given a two-dimensional mesh of cores and a task graph, the *task mapping problem* is to map each task to a core (at most one task to a core) in a way that minimizes communication energy.

Describe two heuristics to approximately solve the task mapping problem. Identify the strengths and weaknesses of both. Specify which of the two heuristics you expect to perform better and explain why.

Let $G = (V, E)$ denote an undirected graph in which each edge $e_i \in E$ has bandwidth $b(e_i)$. The *bottleneck rate* $b(P)$ of a path P between two vertices u, v is the minimum bandwidth of any edge in P. The *best achievable bottleneck rate* for pair u, v is the maximum over all paths P between u and v of the value $b(P)$.

Prove that a spanning tree T exists in G such that, for every pair of vertices u, v, the bottleneck rate of unique path in T between u and v is equal to the best achievable bottleneck rate for u, v. Give an efficient algorithm to construct such a spanning tree. Derive the time complexity of your algorithm.

Computer Software 3 **Spring 2015**

Consider a system in which a counter needs to be incremented using bit level operations. It is well-known that to increment a binary number, all you need to do is complement all the bits from the right up to the rightmost 0. For example incrementing 1010 1011 0111 1111 gives $\underbrace{1010\ 1011}_{\texttt{unchanged}}\ \underbrace{1000\ 0000}_{\texttt{complemented}}$. For this problem the cost of the incrementing equals the number of bits complemented.

Answer the following parts. All answers must be justified.

(a) Determine the cost of increment the following binary numbers.

(i) 000

(ii) 010

(iii) 111

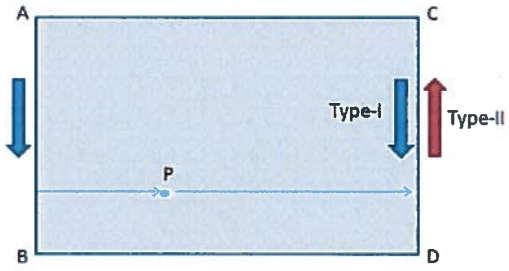
(b) What is the worst case cost of incrementing an n-bit counter?

(c) If the n-bit counter is incremented from 0 to $2^n - 1$, then prove that the amortized cost per increment (that is, the average cost per increment) is $O(1)$ (upper bounded by a constant).

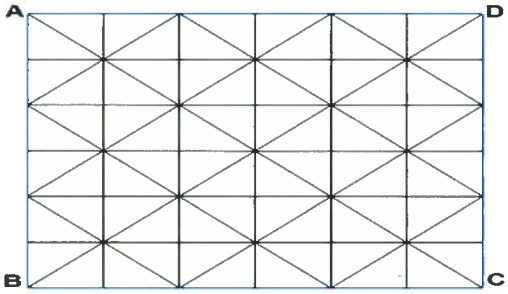
For this part, you can use the fact that $\sum_{i=1}^{n} \frac{i}{2^i} = 2 - \frac{n+2}{2^n}$.

(d) To prove part (c), is it necessary for the counter to start at 0?

Computer Software Q4 **Spring 2015**



(1)



(2)

Given a rectangle patch $ABCD$ (Figure (1)). If you glue AB with CD, following the direction indicated by the Type-I arrow, you will get a *cylinder*. But if you glue AB with DC instead, i.e. A glued to D, B glued to C, following the direction indicated by Type-II arrow, you will get a *Möbius strip*. Suppose there is a 2D robot living in a giant planet that is either a *cylinder* or *Möbius strip*, can you develop algorithms to help the robot identify whether the planet is a *cylinder* or a *Möbius* strip?

(a) Suppose the robot can move freely on this surface, but it can only examine and mark a very small neighboring region on the surface to detect whether a point is on the boundary and label it when needed. Describe an algorithm for the robot to differentiate the cylinder and Möbius strip.

(b) This is another method. Suppose the robot has a way to tessellate the planet to F triangles, E edges, and V vertices, as shown in Figure (2). And the robot can mark arrows along edges inside faces, then use the consistency of the directions of arrows from neighboring faces to differentiate the cylinder and Möbius strip. Develop an algorithm based on this idea, and analyze its time complexity.

Consider a long, quiet country road with houses scattered very sparsely along it. (Picture this road as a long line segment, with an eastern endpoint and a western endpoint.) Further suppose that the residents of all these houses are demanding cell phone users. You want to place cell phone base stations at certain points along the road so that each house is within four kilometers of one of the base stations.

Describe an efficient algorithm that achieves this goal, using as few base stations as possible. Explain the correctness of your algorithm, and derive its time complexity in terms of the length of the road and the number of houses along it.

For each of the following two statements, decide whether it is true or false. If true, then explain why. If false, then give a counterexample.

(a) Let $G = (V, E)$ be an undirected, weighted graph with weight $w(u, v)$ on edge (u, v). Edge weights are all positive and distinct. Let T be a minimum spanning tree for G. Suppose we replace each edge weight $w(u, v) = c$ in G by its square c^2, creating a new instance G'. True or false: T must still be a minimum spanning tree for G'.

(b) Let $G = (V, E)$ be a directed, weighted graph with weight $w(u, v)$ on edge (u, v). Edge weights are all positive and distinct. Let P be a minimum-weight path from $s \in V$ to $t \in V$. Suppose we replace each edge weight $w(u, v) = c$ in G by its square c^2, creating a new instance G'. True or false: P must still be a minimum-weight path from s to t for G'.

Computer Software Q3 **Fall 2014**

Given two strings, the longest common substring (LCS) is a longest sequence of characters exists in both strings. For example, given string $S_1 = babcdefggg$ and string $S_2 = befabcdgfeeg$, their longest common substring is $abcd$.

a) Develop your most most efficient algorithm to compute the longest common substring between two given strings. Analyze your algorithm's space and time complexity.

b) Consider a slightly modified definition on LCS. Suppose now the common substring is allowed to have some different characters, as long as the different characters in the common string are not consecutive and are not at the beginning or ending position of the string. For example, the new LCS between S_1 and S_2 now becomes $abcdef$ of S_1, which matches with $abcdgf$ from S_2. Modify your algorithm to solve this problem. Make it efficient and analyze its space and time complexity.

Given two points $\mathbf{v}_1 = (x_1, y_1)$ and $\mathbf{v}_2 = (x_2, y_2)$, any point p located on line segment $[\mathbf{v}_1, \mathbf{v}_2]$ can be represented by:

$$p = (1 - \lambda)\mathbf{v}_1 + \lambda\mathbf{v}_2, \tag{1}$$

where $0 \leq \lambda \leq 1$ is called p's barycentric coordinate. The barycentric coordinate for any point between $\mathbf{v}_1$ and $\mathbf{v}_2$ is between 0 and 1, and it is linear with respect to $\mathbf{v}_1$ and $\mathbf{v}_2$.

(1) Now consider three non-collinear points $\mathbf{v}_1, \mathbf{v}_2, \mathbf{v}_3$, which forms a triangle $[\mathbf{v}_1, \mathbf{v}_2, \mathbf{v}_3]$. Any point p inside triangle $[\mathbf{v}_1, \mathbf{v}_2, \mathbf{v}_3]$ can also be represented using barycentric coordinates linearly that interpolates these three points. Derive the barycentric coordinates for a point inside the triangle. Note that coordinates should have each of its components ranging inside $[0, 1]$.

(2) Further generalize this barycentric coordinates to $n, (n > 3)$ points in n-dimensional space.

Computer Application 3 **Fall 2014**

An image whose profile is given across an edge in Fig 1 is deteriorated with a white Gaussian noise.

i. Propose an operator (single operator or composition of operators) that processes the image with a kernel-based function to reduce effect of the noise and to detect the edge.
ii. What is the purpose of using this kernel-based function proposed; what type of a filter can it be?
iii. How does your operator detect the edge pixel?
iv. Illustrate your answers over the image profile.
v. How can you increase computation performance of your operator for multiple images?

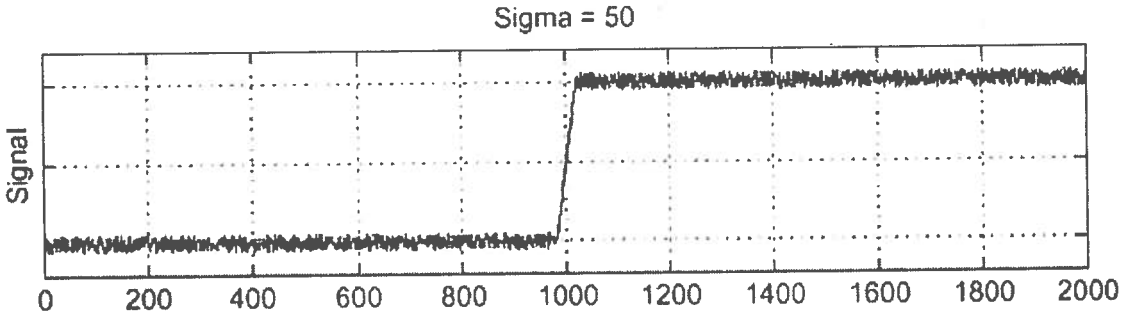


Fig 1 Image profile across an edge

Computer Application 4 **Fall 2014**

Assume that an image is represented by its average image index *AvIndx* defined in equation (1). As an engineer you propose a similarity index, called normalized average image difference *NAID* defined in equation (2), between two images based on their *AvIndx*. You are asked to compare two images I_1 and I_2 whose elements are non-negative.

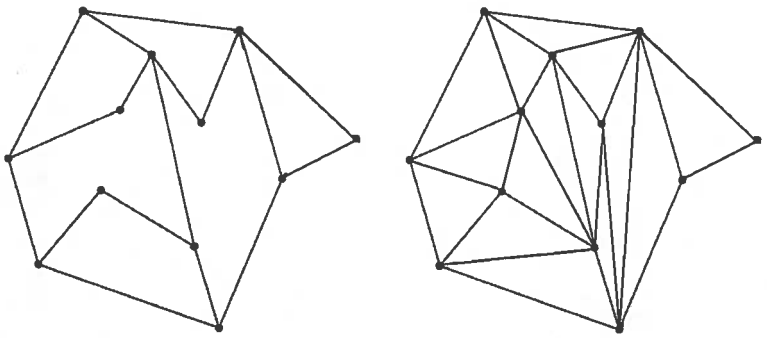
a. How would you test whether this method is 'robust' to a noise in the images compared?
b. What would be the relation between the *NAID* and a threshold *T* such that the proposed similarity measure is 'robust'? Explain your answer formally. State all assumptions you consider.

The proposed similarity measure: Two images are said to be dissimilar if their normalized average image difference *NAID* is greater than a threshold *T*. Hint: Signal = Original Signal + Noise.

$$AvIndx(I) = \frac{\sum_{x,y} I(x,y)}{N} \quad (1)$$

$$NAID(I_1, I_2) = \frac{|AvIndx(I_1) - AvIndx(I_2)|}{\sum_{x,y} I_1(x,y) + I_2(x,y)} \quad (2)$$

Let $P = \{p_1, p_2, \ldots, p_n\}$ be a set of points in the plane. A *planar subdivision* of P is a graph $G = \{V, E\}$ embedded in the plane, where $V = P$ and each edge $e = (p_i, p_j) \in E, p_i, p_j \in P$ is a straight line segment. A *maximal planar subdivision* S of P is a planar subdivision such that no new edge connecting two vertices can be added to S without destroying its planarity, i.e., any edge that is not in S intersects one of the existing edges. A *triangulation* of P is a planar subdivision of P where each bounded facet is a triangle. The left figure is a planar subdivision, and the right figure is a triangulation.



a) Prove that a maximal planar subdivision of P is a triangulation.

b) Is a triangulation always a maximal planar subdivision? If so, prove it; if not, give a counter example.

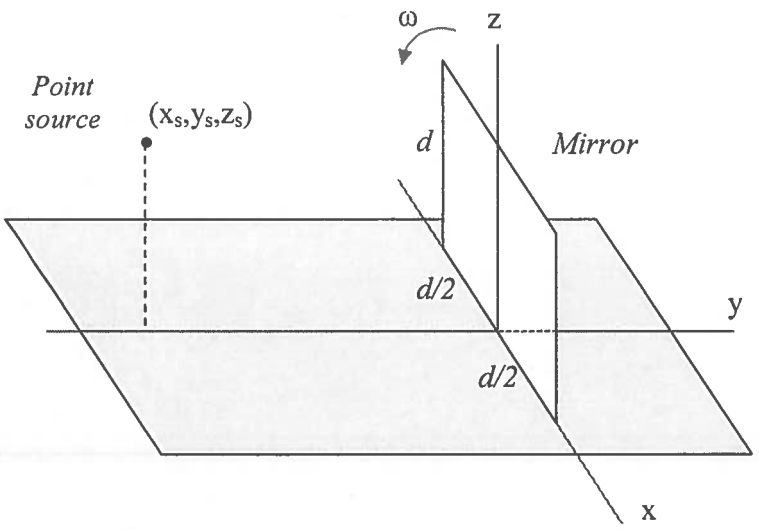
c) Consider a convex polygon with n vertices on its boundary, without introducing new interior point, one can construct a triangulation of this polygon. Does each triangulation scheme have the same number of triangles? If so, how many? If not, explain why.

d) Suppose an arbitrarily given polygon has n vertices on the boundary and m points inside the polygon; a triangulation that taking all these $n+m$ points as vertices can be constructed. Does each triangulation scheme have the same number of triangles? If so, how many? If not, explain and derive the number.

Computer Applications 3 Fall 2013

We have a setup consisting of (i) a point light source with radiance intensity I, located at (x_s,y_s,z_s), (ii) a mirror with size d-by-d, located in the xz-plane, and (iii) a planar surface of infinite size, located in the xy-plane.

Note that $x_s = 0$ and $z_s < d$.



(a) What is the irradiance right below the point source?

(b) What is the irradiance at an arbitrary point on the surface?

(c) Suppose that the mirror starts to rotate along the x axis with an angular velocity of ω in the direction shown in the figure. Derive the irradiance right below the point source and plot it as a function of time.

(State any assumptions you make in your solutions.)

Computer Applications 5 **Fall 2013**

Quadric patches are 3D surfaces that can be represented implicitly as

$$S(x, y, z) = ax^2 + by^2 + cz^2 + dxy + eyz + fxz + gx + hy + jz + k = 0. \quad (1)$$

a) Many simple geometric primitives are in the family of quadric surfaces. Describe the coefficients of spheres, ellipsoids, cylinders, and planes.

b) Any quadric surface patch can be formulated using a matrix representation,

$$P^T Q P = 0,$$

where P is a 4×1 vector and Q is a 4×4 symmetric matrix. Derive P and Q from equation (1).

c) Given a 3D surface patch S, to compute its following geometric properties:

(i) the normal of point $\mathbf{p}(x, y, z) \in S$ on the surface,

(ii) whether a point $\mathbf{q}(x, y, z)$ is on S or not,

(iii) hidden surface determination through z-buffering, namely, given the x and y coordinates of a point $\mathbf{p} \in M$ on the surface M, to check $\mathbf{p}$'s depth coordinate z,

which representation scheme, triangle mesh or implicit quadric representation described above, is more efficient? You should elaborate your comparison on each of these three computations.

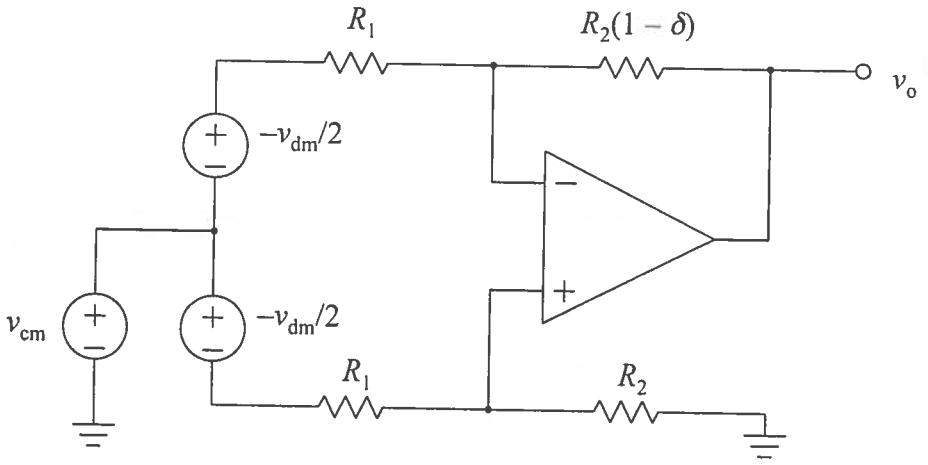
Circuits and Systems
Problem 5

Consider the op-amp circuit shown below. Given $0 < \delta < 1$. Assume an ideal op-amp and answer the following questions.

(a) Find a general expression for the output voltage, v_o.

(b) Find an expression for common mode rejection ratio (CMRR).

(c) When $R_1 = 10\ \text{k}\Omega$ and $R_2 = 100\ \text{k}\Omega$, estimate the resistance tolerance, δ, required for a guaranteed CMRR of 80 dB.



Circuits and Systems **Fall 2014**
Problem 1

In the circuit below, all the diodes are identical, and conduct 1 mA with a forward voltage of 0.7 Volts. Initially there are 40 diodes in series.

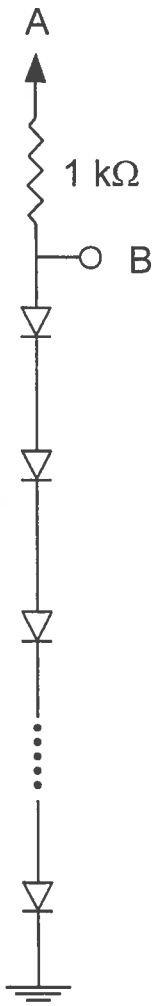
1) If the voltage at B is 28 Volts, what is the voltage at A?

2) What is the impedance at B?

3) If there are only 39 diodes and the voltage at B is 28 Volts, what is the voltage at A?

4) What is the impedance at B?

5) If the voltage at B is 28 Volts and the voltage at A is 32 Volts, how many diodes are there?



Fall 2014

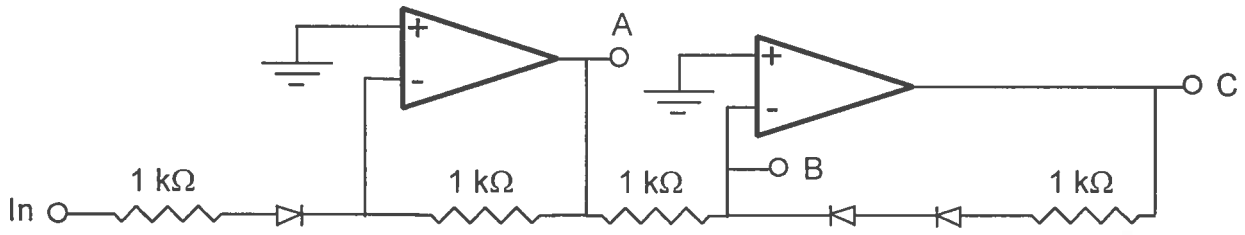
Circuits and Systems
Problem 2

In the circuit below the op-amps are ideal, and the diodes are identical with 0.7 Volt forward voltage.

a) If the input is at 0 Volts, find the voltages at A, B, and C.

b) If the input is at 1 Volt, find the voltages at A, B, and C.

c) Find the large signal gains for both positive and negative inputs.



Circuits and Systems **Fall 2014**

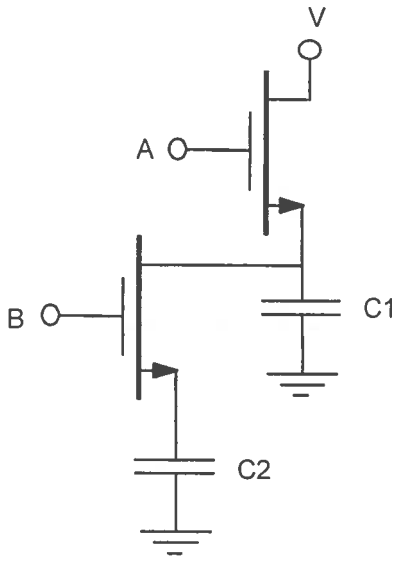
Problem 3

a) In the circuit below point A is initially positive and B is negative. The capacitor C1 is therefore charged to the voltage V. A is then held negative and B is made positive. What is the ratio between C1 and C2 so that C2 is charged to 0.001V?

b) The voltages on A and B are repetitively cycled, charging C1 to V and then discharging it into C2. How many charge-discharge cycles are required for the voltage on the larger capacitor to reach (1-1/e)V?

c) Choose a charge-discharge frequency so that the time for the voltage on the larger capacitor to reach (1-1/e)V is 1 sec.

d) What is the equivalent resistance charging the larger capacitor?



Fall 2014

Circuits and Systems
Problem 5

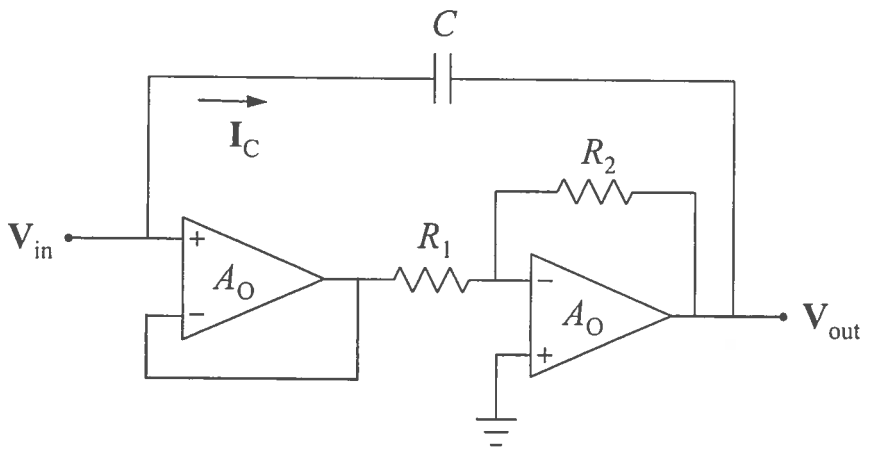
Consider the op-amp circuit shown below. Given, $\mathbf{V}_{in} = V_0 \sin(\omega t)$ and open loop gain, $A_O = 10^5$. Assume ideal op-amps and answer the following questions.

(a) When the capacitor (C) is not connected, find an expression for the output voltage to the input voltage, $\mathbf{V}_{out}/\mathbf{V}_{in}$.

(b) Now consider the capacitor (C) is connected as shown in the circuit below. Find an expression for the current, $\mathbf{I}_C$, in terms of $\mathbf{V}_{in}$ and $\mathbf{V}_{out}$.

(c) Find an expression for $\mathbf{I}_C$ in terms of R_1 and R_2.

(d) Is it possible to determine effective impedance seen from the $\mathbf{V}_{in}$ terminal? If so, find the effective impedance. If not, explain why it is not possible to determine effective impedance.

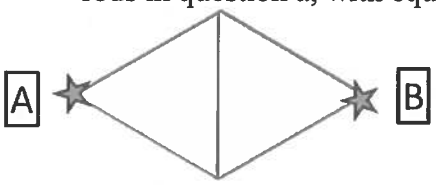


Circuits and Systems
Problem 3

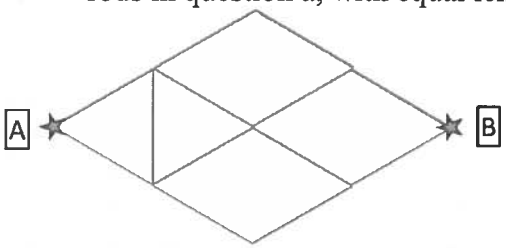
Calculate the resistance of the following structures.

a. Calculate the resistance of a rod with a diameter of 100 um and a length of 1 mm. The resistivity is ρ=0.5 ohm·cm (You can assume that π is equal to 3.)

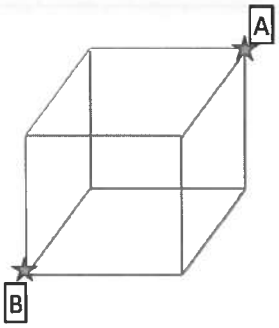
b. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).



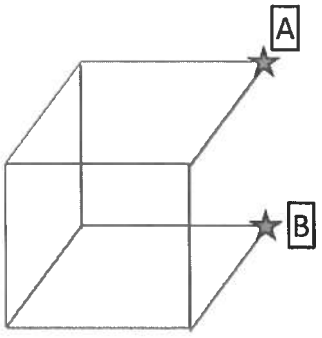
c. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).



d. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).



e. Calculate the resistance between A & B of the following network made from the rods in question a, with equal length (1mm).

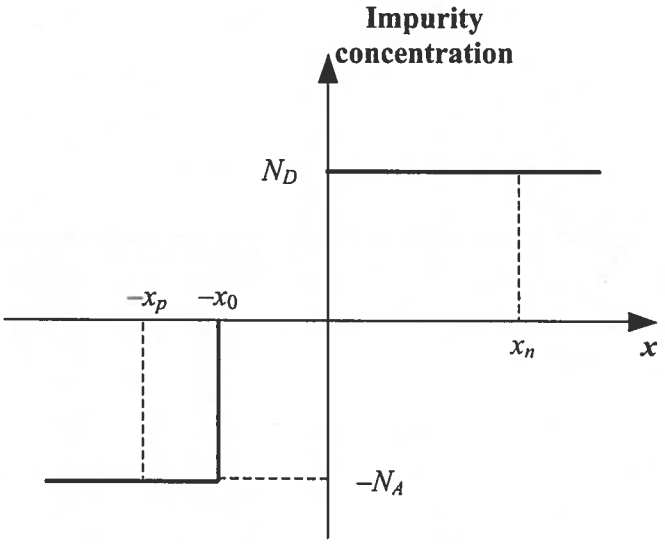


Physical Electronics
Problem 1

A silicon diode has the doping profile as shown in the figure below. N_D and N_A are donor concentration and acceptor concentration, respectively. Given,

$$p_0 = n_i \exp\left(\frac{E_i - E_F}{kT}\right) \quad \text{and} \quad n_0 = n_i \exp\left(\frac{E_F - E_i}{kT}\right)$$

where n_i is the intrinsic carrier concentration, E_i is the intrinsic Fermi level, E_F is the Fermi level, k is the Boltzmann constant and T is the temperature. n_0 and p_0 are electron and hole concentrations in equilibrium. x_n and x_p are n-side and p-side widths of the depletion region. Assume that $-x_p < -x_0$ for all applied biases of interest.



Given, $n_i = 1.45 \times 10^{10}$ cm^{-3}, $k = 1.38 \times 10^{-23}$ J/K, $T = 300$ K, $N_D = 5 \times 10^{15}$ cm^{-3}, $N_A = 1 \times 10^{16}$ cm^{-3}, and $x_0 = 0.5$ μm.

(a) Assuming impurities are 100% ionized, derive the expression for the built-in potential at thermal equilibrium. Justify your answer and show detailed steps.

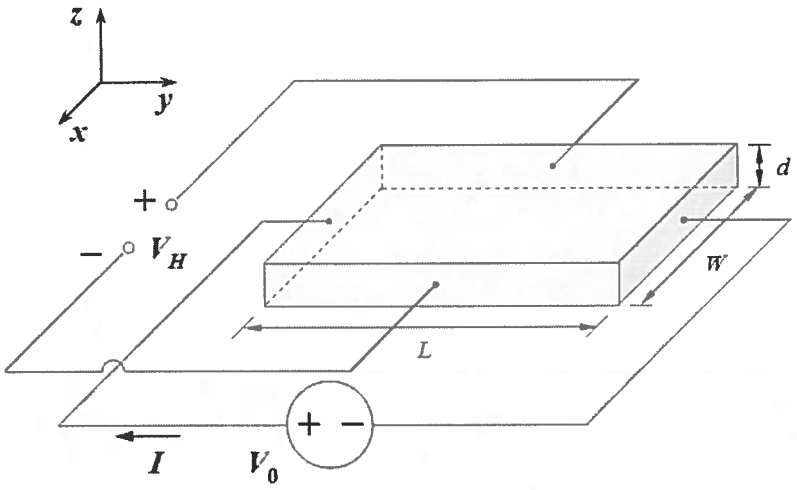
(b) Calculate the built-in voltage (V_{bi}), x_n, and x_p.

(c) Draw an equilibrium band diagram.

(d) When a forward bias of 0.45 V is applied, repeat (b).

Physical Electronics
Problem 3

The figure below illustrates a semiconductor block for measuring the Hall effect. A current (I) is applied in $+y$ direction and a magnetic field (B) is applied in $+z$ direction. Answer the following questions.



(a) Explain how the Hall effect can be used to distinguish the doping type of a semiconductor.

(b) Derive an expression of the Hall voltage V_H for a p-type semiconductor. Define parameters if necessary.

(c) Consider that the silicon Hall sensor whose geometry is L = 1 mm, W = 50 μm, and d = 5 μm in the figure shown above is placed in the known magnetic field (B). When B = 50 mT (or 0.05 Wb/m^2), I = 1 mA, and V_0 = 5 V, the measured Hall voltage (V_H) is 5 mV. Determine the type, concentration, and mobility of the majority carrier.

(d) Will the Hall voltage have temperature dependence? Present your view on this.

Fall 2014

Physical Electronics

Problem 1

a) The following equation describes the relationship between the carrier concentration and the dopant concentration at room temperature, based on charge neutrality. Will the same equation be valid at extremely low temperature? Please justify your answer.

$$p - n + N_d - N_a = 0$$

b) Will the above equation be valid at high temperature (T=400K)? Please justify your answer.

c) A silicon is doped with Boron at a concentration of 10^{15} #/cm^3. What is the concentration of free electron and holes at 300K? Intrinsic carrier concentration $n_i = (9.15*10^{19})*(T/300)^2 * e^{-0.5928\,kT}$ and you can assume non-degeneracy. (you can assume $np=n_i^2$)

d) For the same silicon, what will be the concentration of free electron and holes at T=470K?

*. p, n, n_i, N_d, and N_a are hole concentration, free electron concentration, intrinsic carrier concentration, donor concentration, and acceptor concentration(#/cm^3) in a silicon. k is Boltzman constant and is $8.6*10^{-5}$ eV/K.

Physical Electronics
Problem 2

Fall 2014

A silicon *pn* junction diode has the doping concentrations of $N_A = 2 \times 10^{16}$ cm^{-3} and $N_D = 5 \times 10^{15}$ cm^{-3}, respectively. Given, the intrinsic carrier concentration (n_i) is 1.45×10^{10} cm^{-3}, the Boltzmann constant (k) is 1.38×10^{-23} J/K, and the temperature (T) is 300 K. x_n and x_p are n-side and p-side widths of the depletion region.

(a) Draw an equilibrium band diagram.

(b) Assuming impurities are 100% ionized, derive the expression for the built-in potential at thermal equilibrium. Simply writing down the equation will not earn any credit.

(c) Calculate the built-in voltage (V_{bi}), the depletion region widths (x_n and x_p), and the maximum electric field (E_{max}).

(d) In (b), what would happen if the impurities are not 100% ionized? Would the resulting built-in potential be higher or lower, and why?

(e) When a reverse bias of 0.5 V is applied, repeat (c). In addition, calculate the junction capacitance. Assume the dielectric constant of silicon (ε_s) is 11.7.

Physical Electronics
Problem 3

Fall 2014

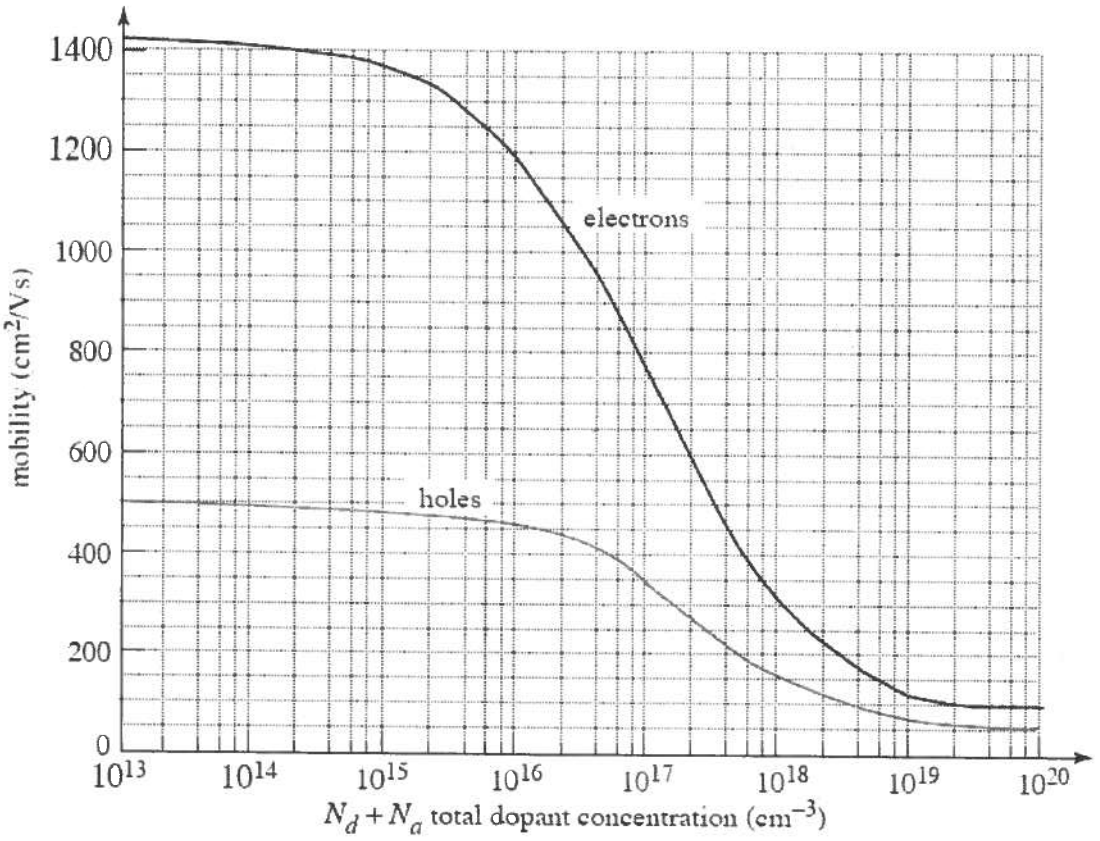
Given a sample of silicon with n-type doping concentration, $N_D=10^{17}$ cm^{-3}. Assume an electric field, E, of magnitude 1 x 10^3 V/cm is applied along the sample in the +x direction. Use the figure below, as necessary. **Circle final answers**.

a) Calculate the drift velocity for electrons. Indicate both magnitude and sign.

b) If an electron drifts a distance of 1 micron along this silicon sample, how long will it take, on average, to drift this distance? (Show your calculation(s).)

c) Find the number of collisions that will occur over a distance of 1 micron. (Assume a collision time of $\tau = 0.07$ picoseconds.)

d) Repeat part c) over a distance four (4) times the mean free path of electrons. Is your answer valid? Explain—use no more than ½ page for your discussion.



Fall 2014

Physical Electronics

Problem 4

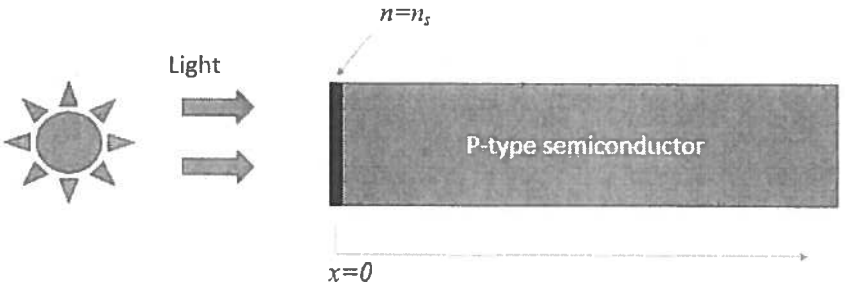
The following is a minority carrier diffusion equation for p-type semiconductor.

$$\frac{\partial \Delta n_p}{\partial t} = D_N \frac{\partial^2 \Delta n_p}{\partial x^2} - \frac{\Delta n_p}{\tau_n} + G_L$$

a) A piece of p-type silicon is uniformly illuminated with G_L. What is the steady-state concentration of the minority carrier?

b) A piece of silicon is uniformly illuminated with G_L until it reaches the stead-state condition. Then, the illumination is turned off at $t=0$. Derive the concentration of the minority carrier over time, $\Delta n_p(t)$.

c) Light is illuminated on one end of silicon bar as below, which is uniformly doped with $N_A=10^{15}$ #/cm^3. The light cannot penetrate into the silicon and affects only the surface(x=0). The concentration of the free electron at the illuminated side is measured to be n_s. Derive $n(x)$, the free electron concentration, along the length of the silicon bar in a steady-state condition.



*. Δn_p is an excessive minority carrier concentration, defined as n - n_0, where n, n_0 are the free electron concentration, and the equilibrium electron concentration. D_n is the minority carrier diffusivity; τ is minority carrier lifetime.

Physical Electronics
Problem 5

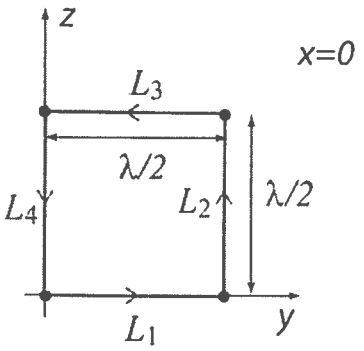
Fall 2014

The magnetic field phasor of a uniform plane wave propagating in free space is given by

$$\mathbf{H}(z) = H_0 e^{-jk_0 z}\hat{\mathbf{y}}.$$

(a) Calculate the left side of Ampere's law $\oint \mathbf{H} \cdot d\mathbf{L} = \int_S \mathbf{J}_d \cdot d\mathbf{S}$ for the surface $x = 0,\ 0 \le y \le \frac{\lambda}{2},\ 0 \le z \le \frac{\lambda}{2}$ (shown in the figure below), where $\lambda = \frac{2\pi}{k_0}$ is the wavelength, and $\mathbf{J}_d = j\omega\mathbf{D}$ is the displacement current density.

(b) Calculate the electric flux density $\mathbf{D}$, and use it to calculate the right side of Ampere's law.

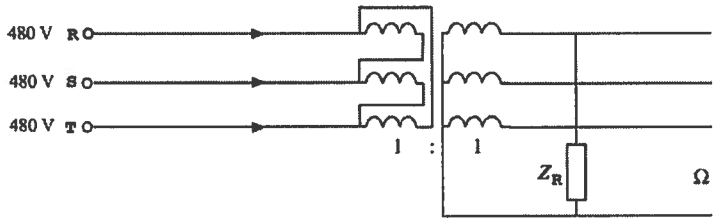


POWER 1 **SPRING 2014**

A. Develop power equation of the three-phase unbalanced linear-time invariant (LTI) load specified in terms of line-to-line admittances for harmonics $\boldsymbol{Y}_{RS}$, $\boldsymbol{Y}_{ST}$, $\boldsymbol{Y}_{TR}$, assuming that the supply voltage is sinusoidal, but symmetrical and of the positive sequence.

B. Specify phenomena that affect the power factor of such loads.

C. Calculate the rms values of the active, reactive and unbalanced currents in the circuit shown in Figure and the power factor, λ, of the supply, assuming that $\boldsymbol{Z}_R = 2+j3\ \Omega$.



POWER 2 **SPRING 2014**

A Buck-Boost DC/DC converter supplied with voltage U = 200 V is used for the control of the output voltage on the resistance R_0 = 15 Ω from U_1 = 100 V to U_2 = 300 V. Draw the structure of the converter, the waveforms of the inductor and capacitor currents. Calculate inductance L and capacitance C of the converter if the switching frequency is equal to f = 15 kHz and output voltage ripples cannot be higher than 5 % of the output voltage.

POWER 3 **SPRING 2014**

1. Draw the equivalent circuit of a single-phase transformer. What kind of measurements have to be done to determine the parameters of this circuit?
2. Draw the phasor diagrams of currents and voltages, one for the inductive and one for pure resistive load. Show when the voltage regulation is greater.
3. A single phase transformer built (in Europe) for the rated frequency of 50 Hz is going to be connected to the power line (in US) of rated voltage and 60 Hz frequency. Will the power losses in the transformer increase or decrease with respect to those at 50 Hz frequency (assuming the transformer is loaded by the rated current in both circumstances). Explain what kind of power losses and why.
4. 3 single-phase transformers of the turn ratio 10:5 are connected to the 3 phase line of 220 V line voltage. Their primary and secondary windings are connected, first both in Δ and next both in Y.
    - Draw the circuit diagrams for both cases
    - What are the secondary phase voltage and the line voltage in each of the two connections?

POWER 4 **SPRING 2014**

1. Draw the equivalent circuit of the very long high voltage transmission lines. Draw its simplified equivalent circuit with a resistance, inductance, and capacitance.
2. Is there any limit of power transmitted by the line? Which of the line, resistive or inductive can transmit more maximum power?
3. How to minimize the voltage regulation (caused by the voltage drop along the transmission line) of the receiver? Is it possible to minimize it to zero? Explain how.
4. Draw the equivalent circuit of the inductive transmission line linking two systems. Using the voltage phasor diagram explain when the power can be transmitted from one system to another if the magnitudes of the voltages of both systems are equal.

POWER 5 **SPRING 2014**

Design a micro grid of PV rated at 200KW of power and at 230 V AC using a PV module with the following voltage and current characteristics. Determine the following:

a. Number of modules in a string for PV type 1
b. Number of strings in an array for PV type 1
c. Number of arrays
d. Inverter specifications
e. One-line diagram of the system

TABLE 5.47 Photovoltaic Module Data.

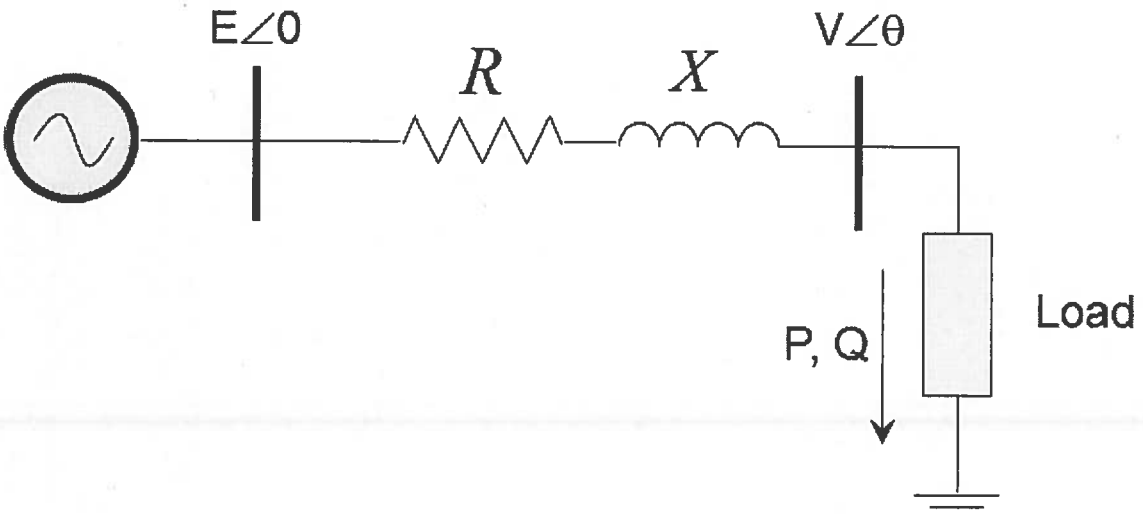
Panel	Type 1	Type 2	Type 3	Type 4
Power (Max). W	190	200	170	87
Voltage at max. power point (MPP), V	54.8	26.3	28.7	17.4
Current at MPP, A	3.47	7.6	5.93	5.02
V_{oc} (open-circuit voltage), V	67.5	32.9	35.8	21.7
I_{sc} (short-circuit current, A	3.75	8.1	6.62	5.34
Efficiency	16.40%	13.10%	16.80%	>16%
Cost	$870.00	$695.00	$550.00	$397.00
Width	34.6″	38.6″	38.3″	25.7″
Length	51.9″	58.5″	63.8″	39.6″
Thickness	1.8″	1.4″	1.56″	2.3″
Weight	33.07 lbs	39 lbs	40.7 lbs	18.3 lbs

POWER 3 **FALL 2013**

1- What is the maximum power transferable to the load? (Assume a constant power factor – i.e. P/Q=constant and neglect R)

2- Draw a typical graph of load voltage vs. active power

3- Explain at least one method to overcome the voltage drop in case of high active power drop.



AUTOMATIC CONTROL 1 **Spring 2015**

Consider a unity negative feedback control system with the loop transfer function given by

$$KG(s) = \frac{K(s+2)^2}{s^3}$$

1. Show that there exsts $K_c > 0$ such that the feedback system is stable for all $K \in (0,\ K_c)$, and use the Routh-Hurwitz method to find the largest value of such K_c.
2. Sketch the Nyquist plot and determine the critical value of $K_c > 0$. Is it the same as that in 1., and why?
3. Find the phase margins when $K = \frac{K_c}{3}$ and when $K = \frac{2K_c}{3}$. Discuss the step response performance such as the percentage overshot and rise time when $K \in (0,\ K_c)$ increases and decreases.

AUTOMATIC CONTROL 2 **Spring 2015**

Let (A, B, C, D) be a realization of order n, and A be a Schur stability matrix. Let P and Q be the observability and reachability gramians, respectively. That is,

$$P = A^T P A + C^T C, \quad Q = AQA^T + BB^T.$$

1. Let $P = U\Sigma_o U^*$ be singular value decomposition where U is unitary, and Σ_o is diagonal and of rank $r_o < n$. Show that similarity transform $S = U^T$ yields observability Kalman decomposition.
2. Let $Q = V\Sigma_c V^T$ be singular value decomposition where V is unitary, and Σ_c is diagonal and of rank $r_c < n$. Show that similarity transform $S = V^T$ yields reachability Kalman decomposition.
3. Suppose that A is not a Schur stability matrix but satisfying $\lambda_i(A)\lambda_k(A) \neq 1$ for all (i, k). In this case the two Lyapunov equations still have unique solutions P and Q. Can you use the same method as 1. and 2. for finding the Kalman decompositions? Why or why not?

AUTOMATIC CONTROL 3 **Spring 2015**

Consider a linear system with the following state space realizaiton

$$\begin{aligned} \dot{x} &= \begin{bmatrix} -1 & 0 \\ 0 & 2 \end{bmatrix} x + \begin{bmatrix} 0 \\ a \end{bmatrix} u \\ y &= \begin{bmatrix} b & 1 \end{bmatrix} x \end{aligned}$$

1. Determine the condition for the controllability and the stabilizability of the system.
2. Determine the condiiton for the observability and detectability of the system.
3. Let $a = 1$. Find a state feedback $u = Fx$ if possible so that the closed eigenvalues are at -1 and -10. Find another state feedback if possible so that the closed eigenvalues are at -10 and -10.
4. Let $a = 1$ and $b = 0$. Find a state estimator (or observer) so that the states can be asymptotically estimated.

AUTOMATIC CONTROL 4 **Spring 2015**

Let a transfer matrix be given by

$$G(s) = \begin{bmatrix} \dfrac{1}{s+1} & \dfrac{10(s+5)}{s(s+1)} \\ \dfrac{1}{s+2} & \dfrac{20}{s} \end{bmatrix}$$

1. Find a minimal (controllable and observable) realization for G.
2. Find a Smith-McMillian form for the transfer matrix G.
3. Find the transmission zeros of the system.
4. Suppose z is a zero. Then find a vector $u = \begin{bmatrix} 1 \\ a \end{bmatrix}$ so that $G(z)u = 0$.

AUTOMATIC CONTROL 5 **Spring 2015**

Consider a unity feedback system with open loop transfer function

$$G(s) = \frac{K(s-1)}{s(s-2)(s+10)}$$

1. Draw root locuses for $K > 0$ and $K < 0$ respectively.
2. Show that the feedback system cannot be stabilized by any stable controller.
3. Suppose $C(s)$ is a controller that stabilizes the feedback system. Discuss the possible controller poles and zeros locations.

AUTOMATIC CONTROL 1 **FALL 2014**

Consider a unity negative feedback system with a plant model given by

$$P(s) = \frac{10(s-5)}{s(s^2+s+4)}$$

and a controller given by

$$C(s) = \frac{K(s+b)}{s+a}$$

for some $K > 0$ and some real b and a.

1. Use root locus method to determine the signs of b and a so that the closed-loop system is stable for all $K \in (0, K_u)$ for some $K_u > 0$.
2. Sketch the possible forms of root locus in terms of the pole and zero location of $C(s)$.

Consider the following discrete-time linear and time-invariant (LTI) system

$$y[n] + y[n-1] - 12y[n-2] = x[n],$$

where $x[n]$ and $y[n]$ are, respectively, the input and output sequences.

1. Determine the frequency response of the above LTI system.
2. Determine the total solution for $n \geq 0$ of the above LTI system for an input $x[n] = 5\,\mu[n]$ and with the initial conditions $y[-1] = -1$ and $y[-2] = 1$. Here, $\mu[n] = 1$ for $n \geq 0$ and 0 for $n < 0$.

COMMUNICATIONS AND SIGNAL PROCESSING 1 **FALL 2014**

Consider the continuous-time signal waveform

$$s(t) = \sum_{k=0}^{n-1} c_k\, p(t - kT_c),$$

where $T_c > 0$ and $p(t) = \begin{cases} 1, & \text{if } 0 \le t < T_c \\ 0, & \text{otherwise} \end{cases}$.

1. If $\{c_0, c_1, \ldots, c_{n-1}\}$ is a given (deterministic) sequence, determine the signal spectrum $S(j\,\Omega) = \mathcal{F}\{s(t)\} = \int_{-\infty}^{\infty} s(t)\, \exp(-j\,\Omega t)\, dt$ in terms of c_k, T_c, and Ω, where $j = \sqrt{-1}$.
2. If the symbol period is $T_b = nT_c$, what is the frequency response for the matched filter, i.e., $S_{\text{match}}(j\,\Omega) = \mathcal{F}\{s(T_b - t)\}$ in terms of c_k, T_c, and Ω?
3. According to Part 2, determine the value of the output of the matched filter at the instant $t = nT_c$ in terms of c_k, T_c, and n.

The unit-step input signal $u(n)$ is defined as 1 for $n \geq 0$ and 0 for $n < 0$. Consider a causal, linear and time-invariant (LTI) system whose input signal is given by $x(n) = u(n)$ and whose output signal is given by

$$y(n) = 2^n u(-n-1) - (0.5)^n u(n).$$

1. Determine the impulse response $h(n)$ of this LTI system.
2. Find the transfer function $H(z)$.
3. Determine whether the LTI system is stable or not, in a bounded-input bounded-output (BIBO) sense.
4. If the LTI system has the input signal $x(n) = 2^n u(n) + u(-n)$, determine the corresponding output signal $y(n)$.

Let $\{X_t; -\infty < t < \infty\}$ be a Gaussian random process with $E\{X_t\} = 0$ for all t and

$$E\{X_t\, X_s\} = \frac{1}{2}\,(|t| + |s| - |t - s|).$$

1. Write the probability density function (PDF) of the random variable X_t for $t = 1$, and $t = -1$.
2. Write the joint PDF of X_t and X_{-s} for $t > 0$ and $s > 0$.
3. What conclusion can you draw for the segments $\{X_t; t \geq 0\}$ and $\{X_t; t < 0\}$ of the process.
4. The process $\{X(t)\}$ is used to modulate a carrier signal at frequency f_0 to get

$$Y(t) = X(t)\cos(2\pi f_0 t + \Theta)$$

where f_0 is constant and Θ is independent of $\{X(t)\}$ and is uniformly distributed over the interval $[0, 2\pi)$. Find the mean and autocorrelation functions of the process $\{Y(t)\}$.

Signals $x(t)$ and $y(t)$ are both periodic with period T. Let $\{x_n\}$ and $\{y_n\}$ denote the Fourier series for $x(t)$ and $y(t)$, respectively.

1. Write the Fourier series pair of equations relating $x(t)$ and $\{x_n\}$.
2. Prove the equality
$$\int_{-T/2}^{T/2} x(t)y^*(t)dt = \sum_{n=-\infty}^{\infty} x_n y_n^* \tag{0.1}$$
3. Using (0.1) prove the Parseval's theorem and interpret it.
4. $g(t)$ is a function of duration T_0 over the interval $[-T_0/2, T_0/2]$. Let $f_0 = 1/T_0$. Prove the following identity referred to as *Poisson's sum formula.*
$$\sum_{m=-\infty}^{\infty} g(t - mT_0) = f_0 \sum_{n=-\infty}^{\infty} G(nf_0)e^{j2\pi nf_0 t} \tag{0.2}$$
where $G(f)$ is the Fourier transform of $g(t)$.

Consider a sequence of K identically and independently distributed Bernoulli random variables $\{X_n, n = 0, 1, \cdots, K-1\}$ with $\mathrm{P}(X_n = 1) = 1 - P(X_n = 0) = \alpha \in (0, 1)$ for all n. Let $S_K = \sum_{n=0}^{K-1} X_n$ denote the weight of the sequence, namely, total number of 1's observed in the sequence. Answer the following questions:

1. Compute $\mathrm{P}\{X_0 = x_0, X_1 = x_1, \cdots, X_{K-1} = x_{K-1}\}$, the probability of any sequence of K binary variables, with $x_j \in \{0, 1\}$ for all j, and express it as a function of its total weight S_K.
2. Find the probability mass function (PMF) of S_K, i.e. $\mathrm{P}(S_K = j)$ for all possible j's.
3. Given $S_K = L \leq K$, find the conditional probability mass function of the sequence $\{X_n\}$, i.e. $\mathrm{P}\{X_0 = x_0, X_1 = x_1, \cdots, X_{K-1} = x_{K-1} | S_K = L\}$. Does this conditional probability depend on the parameter α?
4. Assume $\alpha = 0.3$, and we divide all possible binary sequences of K binary symbols into different classes in terms of S_K, i.e. all sequences whose total weight is $S_K = L \leq K$ are put into the L-th class. Among all these classes, which class has the largest probability for large K? (Justify your answer)