

MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

COMPUTER ENGINEERING TOPICS

Logic Design

Combinational logic theory and design
Sequential circuits and their implementation

Processor Design

System organization
Memory systems
 Memory hierarchy
 Memory addressing modes
 Caches
Implementation techniques
 Hardwired and microprogrammed controllers
 Pipelined and superscalar datapaths
Instruction set design
Computer arithmetic
 Basic concepts and implementation

Algorithms and Data Structures

Stacks, queues, linked lists, trees
Computational complexity, running time analysis, recurrence relations
Basic sequential algorithms: quicksort, merge sort, searching, etc.

Operating Systems

Coordination constructs, processes,
Memory management, virtual memory, deadlocks

Parallel Computing

Fundamental concepts: speedup, efficiency, complexity analysis,
 interconnection topologies, Flynn's taxonomy
Fundamental knowledge of mesh, hypercube, and similar networks
Basic parallel algorithms: broadcast, prefix sums

Computer Networks

Fundamental concepts in networks: switching and multiplexing

Other Applications

Neural network models, Image processing, logic testing

Note: The student is required to understand the above topics thoroughly. Any additional concepts required to solve a problem will be provided with the question itself.

MS COMPREHENSIVE / PH.D. QUALIFYING EXAM
ELECTRONICS ENGINEERING TOPICS

A. Circuits

Circuit applications of diodes. Circuit applications of BJT, MOSFETs and JFETs in linear and digital circuits. Linear applications include amplifiers, oscillators, differential amplifiers and operational amplifiers. Applications of ideal operational amplifiers. Digital applications include internal operation of standard logic gates used as building blocks in logic families such as TTL, ECL, NMOS and CMOS.

B. Devices

Basics of carrier transport in semiconductor materials, physics of p-n junction diodes, bipolar and field effect transistors. Derivation of terminal current-voltage characteristics of discrete devices, large and small signal models. Basic physics of photonic devices. Basic integrated circuit technology.

C. Fields

Static fields, Maxwell's equations, propagation through isotropic medium, reflections and basic antenna theory.

Representative References

1. M.N. Horenstein, *Microelectronic Circuit and Devices*, Prentice Hall.
2. Mitchell & Mitchell, *Introduction to Electronic Design*, 2nd Ed., Prentice Hall.
3. Gray & Mayer, *Analysis and Design of Analog Integrated Circuits*, 3rd Ed., John Wiley.
4. Hodges & Jackson, *Analysis and Design of Digital Integrated Circuits*, 2nd Ed., McGraw Hill.
5. B. Streetman, *Solid State Electronic Devices*, 3rd Ed., Prentice Hall.
6. J.P. McKelvey, *Solid State and Semiconductor Physics*, Harper & Row.
7. Shen, *Applied Electromagnetics*, 2nd Ed., Prindle-Weber-Schmidt.

M.S. Comprehensive /Ph.D. Qualifying Exam

Communication and Signal Processing Topics

Probability Theory and Random Processes

Basic concepts in probability theory; stationarity and wide sense stationarity of random processes, power spectral density, linear filtering of random processes, minimum mean squared error estimation, Gaussian and Poisson random processes.

Signals, Systems, and Digital Signal Processing

Continuous time and discrete time signals and systems: fundamental concepts, system properties (causality, stability, time invariance, etc.); time and frequency domain characterization of discrete and continuous time signals and systems; transform domain techniques; sampling and reconstruction; sampling rate conversion, frequency-domain analysis, aliasing and Nyquist rate concepts; discrete Fourier Transform and FFT algorithms; design and implementation of FIR and IIR filters.

Analog Communication

Amplitude modulation techniques; frequency and phase modulation techniques; sampling, quantization; pulse code modulation (PCM); effect of noise on continuous wave and PCM systems.

Digital Communication

Signal space representation; baseband representation of bandpass signals and systems; maximum likelihood (ML) detection and estimation; optimum receiver principles. performance of optimum receivers; differential, partially coherent and non-coherent detection of signals; bandwidth efficiency and power efficiency; receiver design and performance analysis of digital modulation schemes in fading channels; linear block codes and their decoding strategies, hard decision and soft decision decoding.

Representative References

1. Simon Haykin, *Communications Systems*, (Wiley).
2. J. G. Proakis and M. Salehi, *Communication Systems Engineering, 2nd Edition*, Prentice Hall.
3. J. G. Proakis, *Digital Communication*, 4th Edition, McGraw-Hill, 2000.
4. J. M. Wopzencraft and I. M. Jacobs, *Principles of Communication Engineering*, John Wiley & Sons, New York, 1965.
5. Henry Stark and John W. Woods, *Probability and Random Processes with Applications to Signal Processing, 3rd Edition*. Prentice-Hall.
6. *Probability, Random Variables, and Stochastic Processes*, A. Papoulis, 3rd edition, McGraw-Hill, 1991.
7. S. K. Mitra, *Digital Signal Processing*, 3rd edition, McGraw-Hill.
8. A. V. Oppenheim and R.W. Schaffer, *Discrete-time Signal Processing*, Prentice-Hall.

MS COMPREHENSIVE / PH.D. QUALIFYING EXAM

AUTOMATIC CONTROL TOPICS

A. Basic Tools

Laplace, Z transforms: basic properties, use in solving linear differential/difference equations, application to system analysis, transfer functions. Fourier transform, Fourier series: basic properties, application to signal analysis, frequency response, spectral energy density.

B. Basic Concepts

Linearity, time invariance, causality, difference and differential systems, linearization, signal-flow and block diagrams, BIBO and asymptotic stability.

C. Classical Control

Transient and steady state analysis and performance indicators, pole location, sensitivity; frequency domain analysis, phase and gain margins; Nyquist stability, Routh-Hourwitz criterion, root locus, lead and lag compensator design, PID control; pole placement with fractional controllers.

D. Sampled Data Systems

Basic A/D and D/A conversion, sampling theorem. Discretization of continuous time systems, deadbeat control.

E. State Space Control for Continuous and Discrete Time Systems

State and state equations, transition matrix, solution of state equation. Realization, controllability and stabilizability, observability and detectability, Lyapunov stability, state feedback and pole placement, asymptotic observers, state feedback with observers.

Representative References

1. C-T. Chen, *System and Signal Analysis*, Saunders College Publishing.
2. B.C. Kuo, *Automatic Control Systems*, Prentice Hall.
3. G.F. Franklin, J.D. Powell, A. Emami-Naeini, *Feedback Control of Linear Systems*, Addison Wesley.
4. G.F. Franklin, J.D. Powell, M.L. Workman, *Digital Control of Dynamic Systems*, Addison Wesley.
5. K. Ogata, *Discrete-time Control Systems*, Prentice Hall.
6. W.L. Brogan, *Modern Control Theory*, Quantum Publishers, Inc.
7. T. Kailath, *Linear Systems*, Prentice Hall.
8. K. Ogata, *Modern Control Engineering*, Prentice Hall.
9. C. T. Chen, *Linear system Theory and Design*, 3rd Ed., Oxford University Press, 1999.

COMPREHENSIVE MS/QUALIFYING PH.D. EXAM

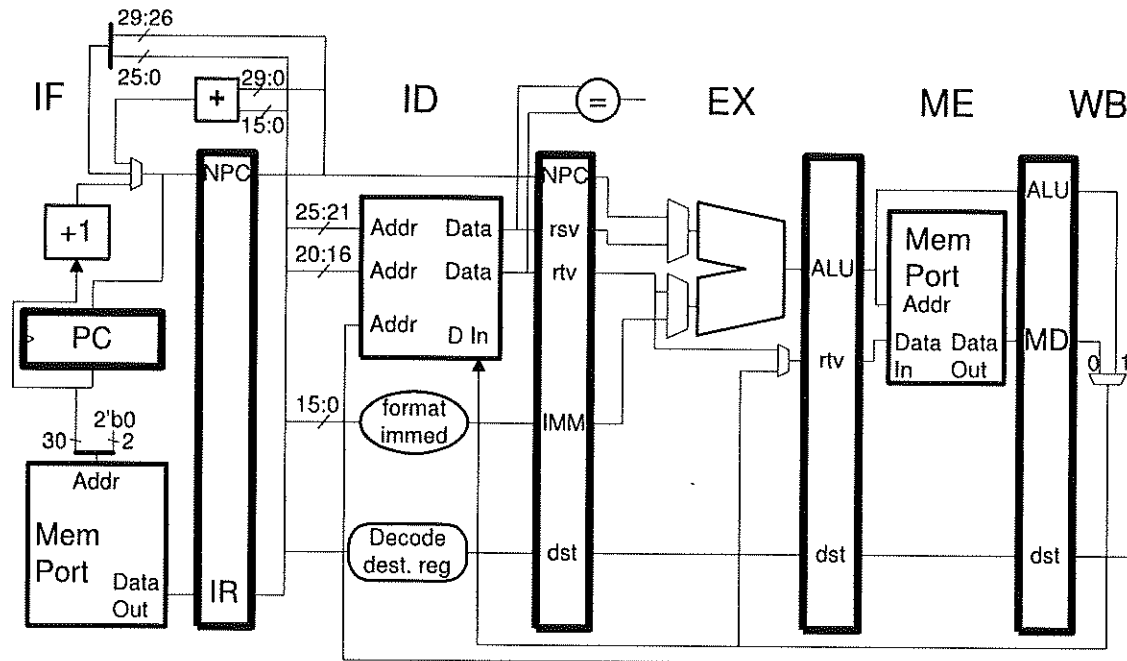
POWER ENGINEERING TOPICS

- A. Electric Machinery
Maxwell's equations; analysis of simple electromechanical devices using Maxwell's equations; synchronous machines, voltage behind reactance model, Park transformation, d,q equations; exact and approximate equivalent circuits of single-phase transformers, nonlinear effects; modeling and calculation of its parameters of transmission lines; modeling and analysis of direct current and induction machines.
- B. Power Systems
Per-unit calculations; symmetrical components; sequence impedances of transformers, synchronous machines and induction motors, sequence impedances and capacitances of transmission lines; sequence networks for fault analysis; shunt faults (3-phase, LG, LLG, LL faults); series faults (1LO, 2LO); power flow equations, (Decoupled) Newton-Raphson, Gauss/Gauss-Seidel methods; optimal dispatch with/without line losses; transient stability, swing equation, equal area criterion, effect of clearing time; low-frequency oscillations, supplementary excitation/governor control; linear optimal stabilization.
- C. Power Electronics
Fourier series of nonsinusoidal voltages and currents; analysis of circuits with nonsinusoidal voltage and current waveforms, nonsinusoidal active and apparent powers; single-phase and three-phase rectifiers, controlled AC/DC converters, DC/DC converters, inverters.

Representative References

1. R.D. Schultz & R.A. Smith, *Introduction to Electric Power Engineering*, John Wiley, 1988.
2. V. DelToro, *Electric Power Systems*, Prentice Hall, 1992.
3. P.M. Andersen, *Analysis of Faulted Power Systems*, The Iowa State Univ. Press, 1983.
4. Y.N. Yu, *Electric Power System Dynamics*, Academic Press, 1983.
5. M.H. Rashid, *Power Electronics*, Prentice Hall, 1988.
6. N. Mohan, T.M. Undeland, W.P. Robbins, *Power Electronics*, John Wiley, 1989.

Illustrated below is a MIPS implementation in which the branch is resolved in ID, but which lacks bypass paths into the EX stage. The register file, in ID, is designed so that a read of a register that is also being written will return the value being written.



(a) Show a pipeline execution diagram for the MIPS code below assuming that the branch is taken. Pay close attention to bypass paths (or their absence) and be sure that the number of stall cycles in your solution is correct.

```
beq r20, r21, TARG
add r1, r2, r3
andi r14, r14, 0xff
and r12, r1, r13
TARG:
sub r4, r1, r5
```

(b) Show a pipeline execution diagram for the MIPS code above assuming that the branch is not taken.

For the parts below consider a variant of MIPS called *MIPS Exposed!!* (*MIPSe!!*), in which the behavior of an instruction is defined to be whatever the illustrated pipeline would do if it didn't stall.

(c) The code below is identical to the code above, but it is written for MIPSe!. Re-write the code for MIPS.

```
beq r20, r21, TARG
add r1, r2, r3
andi r14, r14, 0xff
and r12, r1, r13
TARG:
sub r4, r1, r5
```

Call the outcome of a branch either taken (T) or not taken (N), the *local history* of a branch is a sequence of its outcomes. For example, a branch with local history TTN has three outcomes, the most recent not taken.

A *local history predictor* predicts a branch by using its local history as an index (an address) into a *pattern history table (PHT)* in which 2-bit counter values are stored. The branch is predicted not taken if the count is 0 or 1, otherwise it is predicted taken. If the branch is ultimately taken the counter is incremented otherwise it is decremented. Let m denote the number of bits in the PHT index (address).

Call pattern TTNTTNTN... a 3-iteration loop pattern, generated by a 3-iteration loop branch; define an i -iteration loop pattern and branch similarly.

(a) Consider the local history predictor described above in which m bits of a branch's local history is used to index the PHT. **Ignoring interference** from other branches, what is the longest i -iteration loop branch (largest i) that can be predicted with 100% accuracy on this predictor. Use an example to justify your answer.

(b) Explain why the answer to the question above would be different if one did not ignore interference from other branches. Consider common branch behaviors, and illustrate your answer with an example.

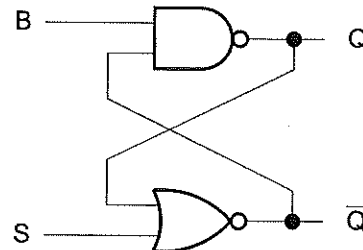
For the next parts consider two methods to reduce interference between branches: *LH xor PC indexing* and *LH cat PC indexing*. In LH xor PC indexing the m -bit PHT index is the m -bit local history exclusive orred with m bits of the PC (address) of the branch being predicted. In LH cat PC indexing the m -bit PHT index is the $\frac{m}{2}$ -bit local history concatenated with $\frac{m}{2}$ bits of the branch PC.

(c) Which of the two methods would be better for the loop branches described above? Explain.

(d) Suppose a program had a frequently executing branch that could be modeled as a Bernoulli random variable, with probability of being taken switching from $p = .2$ to $p = .8$ every million executions of the branch. Which of the two methods would be better for this random branch? Explain, and also explain the impact on short perfect loop branches.

This problem involves the utility of some fictitious hardware elements defined below. Answer the following questions. All answers must be justified.

- (a) Consider the BS-latch represented by the circuit to the right.
Trace the response of the BS latch for the four possible logic values of the inputs.

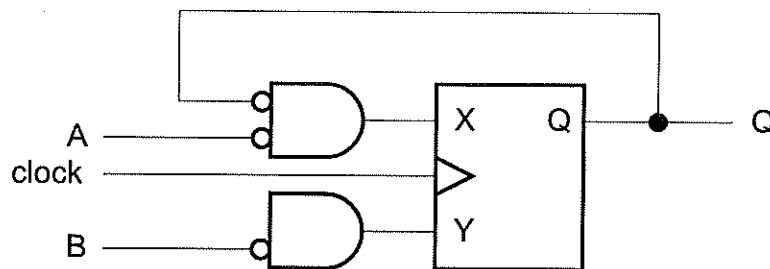


- (b) Is the BS latch useful for designing sequential logic? Justify your answer.

- (c) The function table to the right describes a fictitious XY flip-flop. Variables Q and Q^* refer to the present and next state, respectively, of the flip-flop.

X	Y	Q^*
0	0	1
0	1	Q
1	0	\overline{Q}
1	1	1

Determine the state diagram of the circuit shown below, that employs the XY flip-flop.



- (d) Prove that every sequential circuit can be constructed using only XY flip-flops and combinational logic.

Consider an undirected graph $G = (V, E)$. We define an edge of G to be a *cycle-enabling* edge if its removal renders the graph acyclic. Design an efficient sequential algorithm to determine the set of all *cycle-enabling* edges of an undirected graph. Provide an analysis of its running time. Explain why your algorithm is correct. You will get no points if the complexity of your algorithm equals or exceeds $O(|V||E|)$.

An $N \times N$ mesh topology is an N -row n -column arrangement of nodes with edges between a node and its neighbors to the north, south east and west. For $0 \leq i, j < N$, the node at row i and column j has a two-dimensional index (i, j) . The *neighbors* of node (i, j) are nodes $(i - 1, j)$, $(i + 1, j)$, $(i, j - 1)$ and $(i, j + 1)$ (if they exist).

There are several possible one-dimensional numberings for an $N \times N$ mesh. The figures below shows two; *row-major* on the left and *diagonal* on the right.



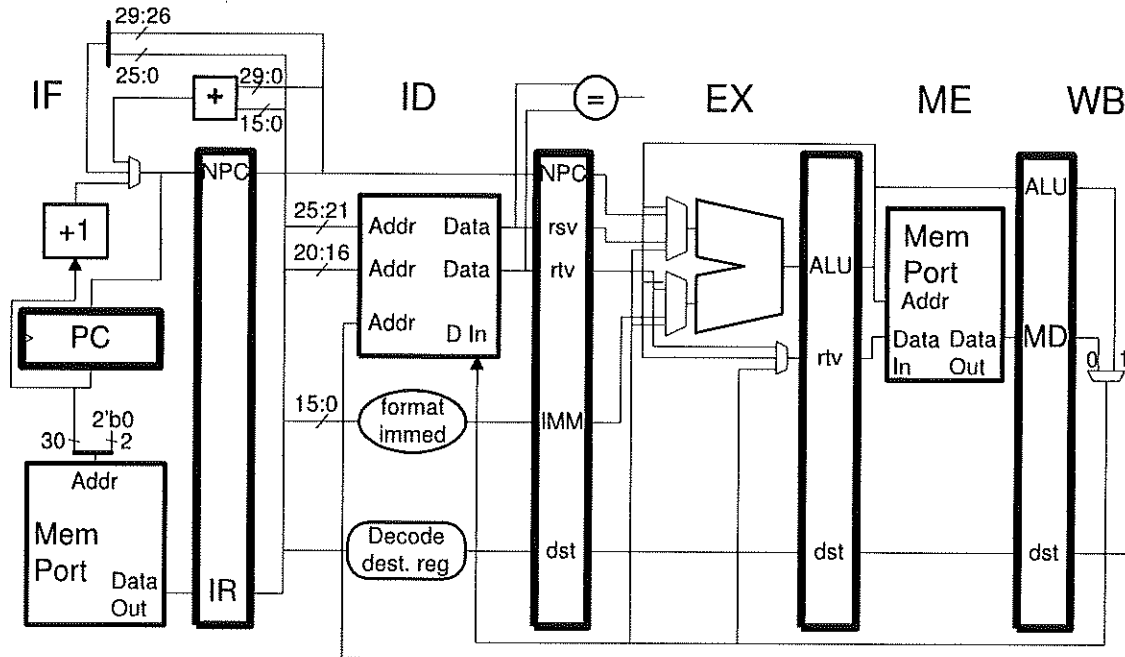
For any node (i, j) of an $N \times N$ mesh, let $f(i, j)$ be a 1-dimensional number of the node. For any neighbor (i', j') of (i, j) , the *distance* between (i, j) and (i', j') is defined to be $|f(i, j) - f(i', j')|$, the absolute value of the difference of their indices. The *average distance* of node (i, j) is the average of its distances from all its neighbors.

Some geometric problems benefit from a 1-dimensional numbering that tends to keep the numbering of neighboring nodes close to each other. That is, they prefer 1-dimensional numberings for which nodes have a small average distance.

Answer the following questions. All answers must be justified.

- For a 4×4 R-Mesh, determine the average distance of node $(2, 2)$ under the two numberings (row major and diagonal) shown above.
- For any $N \geq 1$, and any $0 \leq i, j < N$, determine the average distance of node (i, j) of an $N \times N$ Mesh under the row major and diagonal numberings.
- Can you think of a way of numbering nodes that could have a smaller average distance for most nodes than in row major or diagonal numbering?

The MIPS code below executes on the illustrated implementation. It includes a prefetch instruction that will bring data to the cache for later use (to avoid a cache miss or at least reduce cache miss time seen by the load).



LOOP:

```
lw r1, 0(r2)      # Load data at address 0+r2 into register r1.
add r3, r3, r1
add r2, r2, 4
bneq r2, r4 LOOP  # Branch if r2 is not equal to r4
prefetch 0x400(r2) # Delay slot, executed whether or not branch taken. This
                  # instruction loads data at address 0x400+r2 into the cache.
```

A loop is said to be *unrolled by degree d* if the loop body is duplicated d times; if the loop executed I iterations before unrolling it would execute $\lfloor \frac{I}{d} \rfloor$ iterations after unrolling, for convenience assume that I is a multiple of d . Degree 1 indicates no unrolling at all.

(a) Show the code when the loop is unrolled by degree 2. Take care to apply appropriate optimizations. A goal is to reduce the instruction count and the number of stalls.

(b) Compare the performance of the unrolled and original loop. Use an appropriate performance measure. Assume that the load never misses the cache.

(c) Consider a processor similar to the one above except that load instructions never stall in ME due to a cache miss, instead they proceed through WB normally. If a load does miss then an instruction that tries to use the loaded value before it arrives will stall until the data arrives.

Suppose that the prefetch in the original code eliminates cache misses for the `lw`. To what degree would the code need to be unrolled to make the prefetch instruction unnecessary with no-stall loads? (Assume an unlimited number of registers.)

One approach to combat cheating in multiplayer computer games is to select multiple “referees” to monitor game play. Define the *average player-to-referees delay* for a player p_i as the average of the delays from p_i to each referee. Two criteria exist for selecting this set of referees:

1. minimize the sum over all players of the average player-to-referees delay, and
2. minimize the difference between the maximum average player-to-referees delay and the minimum average player-to-referees delay, where the maximum and minimum are taken over all players.

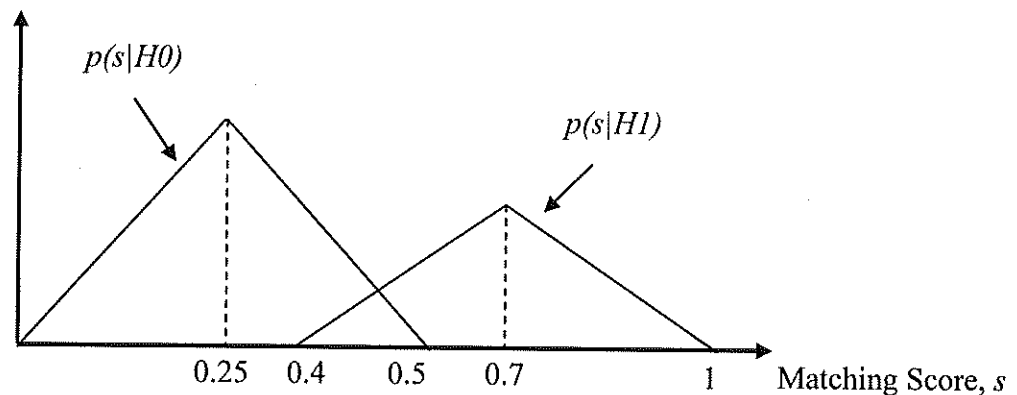
Design an algorithm to select r referees from a pool of z potential referees for a set of n players. You are given a table of the delays from each player to each potential referee. Your algorithm should be efficient and should try to satisfy both criteria as much as possible (but it might not be optimal for either criterion). What is the time complexity of your algorithm? Does it favor Criterion 1 over Criterion 2 or vice versa or does it address both equally?

Design a data structure to be used with a task scheduler as follows. Each task has a key, which is an arbitrary integer.

- When a new task arrives, insert the task into the data structure.
- When the task scheduler requests a task, then return the task with smallest key value and remove that task from the structure.

The structure is to execute these operations as efficiently as possible.

Describe in detail your data structure, the INSERT procedure, and the REMOVE-MINIMUM procedure. If the structure contains n tasks, then how much memory does it use? What is the time complexity of the INSERT procedure as a function of n ? What is the time complexity of the REMOVE-MINIMUM procedure as a function of n ?



A fingerprint verification system produces matching scores with distributions (probability density functions) as shown in the figure above, where

$H0$ is when the person is an imposter, that is, he is not who he claims he is;

$H1$ is when the person is genuine, that is, he is who claims he is.

The system verifies an identity if the matching score, s , is larger than a threshold T .

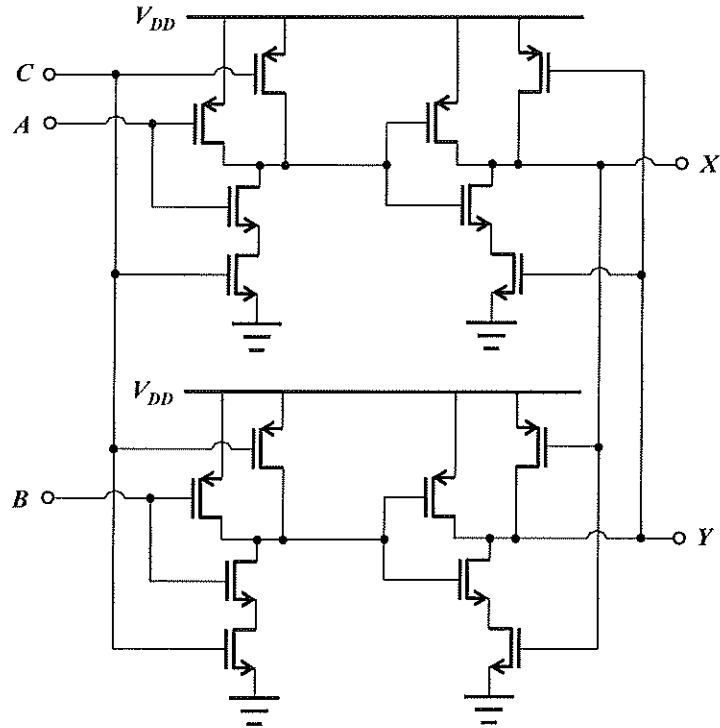
There is a risk (a scalar weight) associated with each misclassification. The risk of classifying an imposter as genuine is $R0$; and the risk of classifying a genuine person as an imposter is $R1$.

- (a) Formulate the total risk as a weighted probability of error.
- (b) Determine the optimal threshold value (that minimizes the total risk) when $R0=R1$.
- (c) Determine the optimal threshold value when the risk of verifying an imposter is double the risk of declining a genuine person.

Spring 2011

Circuits and Systems Problem 2

For a CMOS digital circuit given below, answer the following questions.



- (a) Draw the gate-level diagram.
- (b) Complete the truth table given below.
- (c) Explain the function of the circuit.

Inputs			Outputs	
A	B	C	X	Y
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Let a dynamical system be described by the following set of differential equations:

$$\ddot{x}_1 + 3\dot{x}_1 + 2x_1 = 2\dot{u} + 8u$$

$$\dot{x}_2 + ax_2 = x_1$$

$$y = x_1 + x_2$$

1. Find a state space realization of the system;
2. Discuss the controllability and observability of the system with respect to the parameter a .

Let a second order dynamical system be described by

$$\dot{x} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 2 & 1 \\ 0 & 0 & -4 \end{bmatrix} x + \begin{bmatrix} 0 \\ 1 \\ 0 \end{bmatrix} u$$

$$y = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix} x$$

1. Determine if the system is controllable, stabilizable, observable and detectable.
2. If possible, find a state feedback control so that the closed-loop poles are at $\{-4, -4, -4\}$.
If not possible, explain why.
3. If possible, find a state feedback control so that the closed-loop poles are at $\{-5, -5, -5\}$.
If not possible, explain why.
4. if possible, design a state estimator so that the observer poles are at $\{-10, -10, -10\}$. If not, explain why.

AUTOMATIC CONTROL 3**SPRING 2011**

Consider a negative unity feedback system with plant model

$$P(s) = \frac{1}{(s+1)(s+p)}$$

- (a). In the case $p = 6$, design a PI controller so that the steady state error with respect to the unit ramp input is no more than 0.25 and the overshoot is no more than 10%.
- (b) For the design in (a), find the crossover frequency ω_c , the phase margin, and the maximum possible steady state error when the reference input is $r(t) = \sin(\omega_c t)$?
- (c) For the design in (a), sketch its Nyquist plot.
- (d) For the design in (a) with $p \neq 6$, analyze the phase margin for $2 \leq p \leq 5$.

AUTOMATIC CONTROL 4**SPRING 2011**

(a) Suppose that $P_n(s) = p_0 s^n + p_1 s^{n-1} + \dots + p_n$ is Hurwitz and $p_0 > 0$. Use arguments from root locus to show that $P_{n+1}(s) = \delta s^{n+1} + P_n(s)$ is also Hurwitz, provided that $\delta > 0$ is sufficiently small.

(b) Let $G(s) = B(s)/A(s)$, with $B(s)$ Hurwitz, be the plant model and $C(s) = K/s$ be an integrator feedback compensator. Without loss of generality $b_0 > 0$. Show that

$$1 + K \frac{B(s)}{A(s)} = 1 + K \frac{b_0 s^n + b_1 s^{n-1} + \dots + b_n}{s(s^n + a_1 s^{n-1} + \dots + a_n)} \neq 0$$

for all s on the closed right half plane provided that $K > 0$ is sufficiently large.

(c) Suppose that $B(s) = (s+1)^2 + 1$ and $A(s) = s^2(s^2 - 4)$. Sketch the root locus in (b) for $K > 0$ without computing the breaking point and $j\omega$ -axis crossing.

(d) Suppose in (b) that $b_0 = 0$, $b_1 \neq 0$, and $B(s)$ is Hurwitz. Find the existence condition of the stabilizing gain K in terms of poles and zeros of $G(s)$.

AUTOMATIC CONTROL 5**SPRING 2011**

Consider state-space system: $\dot{x}(t) = Ax(t) + Bu(t)$, $x(0) = x_0$, where $x(t) \in \mathbb{R}^n$ and $u(t) \in \mathbb{R}^m$.

(a) Find the solution $x(t)$ for $t \geq 0$.

(b) Show that the system, i.e., (A, B) , is controllable, if and only if the controllability Gramian

$$G_c(T_f) = \int_0^{T_f} e^{At} B B^T e^{A^T t} dt > 0,$$

for any $T_f > 0$. That is, $G_c(T_f)$ is positive definite.

(c) Suppose that (A, B) is controllable and $x_0 = 0$. For a given $x_f \in \mathbb{R}^n$, find control input such that $x(T_f) = x_f$ where $T_f > 0$. Discuss what will happen for your control input in the case of $T_f \rightarrow \infty$.

The transfer function for a causal digital filter is given by $H(z) = \frac{z-b}{z-a} = \sum_{n=0}^{\infty} h_n z^{-n}$, where $|a| < 1$ and $a \neq b$. Both a and b are real numbers.

- (a) Use the long division to determine h_n in terms of a and b , $\forall n$.
 (b) Use the inverse z -transform by partial fraction expansion to determine h_n in terms of a and b , $\forall n$.

- (c) Assume $F_L(z) = \sum_{n=0}^L h_n z^{-n}$, where L is a positive integer. Define $\rho = \frac{\sum_{n=0}^L |h_n|^2}{\sum_{n=0}^{\infty} |h_n|^2}$. Find the algebraic expression for L , in terms of ρ , a , and b .

- (d) According to (c), determine the *normalized approximation error* as given by

$$\frac{\int_{-\pi}^{\pi} |F_L(e^{j\omega}) - H(e^{j\omega})|^2 d\omega}{\int_{-\pi}^{\pi} |H(e^{j\omega})|^2 d\omega},$$

in terms of ρ , where $j = \sqrt{-1}$, $F_L(e^{j\omega}) = \sum_{n=0}^L h_n e^{-j\omega n}$, and $H(e^{j\omega}) = \frac{e^{j\omega} - b}{e^{j\omega} - a}$.

White noise with power spectral density $S_X(f) = N_0/2$ is applied to a filter with impulse response $h(t) = 1$ for $0 < t < 1$ and 0 otherwise.

1. Find the cross power spectral density $S_{XY}(f)$.
2. Find the cross-correlation $R_{XY}(\tau)$.
3. Find the output power spectral density $S_Y(f)$.
4. Find the output auto-correlation $R_Y(\tau)$.
5. Find the output power P_Y .

Assume that the Fourier transform of the continuous-time signal $x(t)$ for $t \in (-\infty, +\infty)$ is given by $X(j\omega) = e^{-j\omega}$ for $\omega \in [-1, 1]$ and 0 otherwise.

Let the signal $y(t) = \frac{d^2x(t)}{dt^2}$, the second-order derivative of $x(t)$.

1. Find the Fourier transform of the signal $y(t)$, namely, $Y(j\omega)$.
2. Find the total energy of the signal $y(t)$, namely,

$$\int_{-\infty}^{+\infty} |y(t)|^2 dt.$$

3. Find a signal $z(t)$ such that its Fourier transform is $Z(j\omega) = j\omega Y(j\omega)$.
4. Given the linear system defined by

$$r(t) = \int_0^t x(\tau) d\tau,$$

find the Fourier transform of the output signal $r(t)$, namely, $R(j\omega)$.

Given a deterministic low-pass signal $x(t)$ generated at point A whose Fourier transform is $X(f)$, where $X(f) = 0$ for $|f| > B_w$, and the peak amplitude of $x(t)$ is $X_{max} < \infty$. Consider a remote point C which is interested in restoring $x(t)$.

- Assume the received signal at C is $r(t) = s(t) + w(t)$, where $w(t)$ is an additive white Gaussian noise (AWGN) with power spectral density $N_0/2$ and $s(t)$ is the digitally modulated signal transmitted from A .
- Consider a scalar uniform mid-rise quantizer at A with $L = 2^R$ levels to quantize $x(t)$, where R is the number of bits used to represent each level. (Note: a mid-rise quantizer maps an input to R bits by dividing the entire range of each $x(t)$ uniformly into L (even) levels, and each representing point is the mid point of each quantization cell.)
- Assume an uncoded BPSK modulation with transmission energy E_s and basis function $\phi(t), t \in [0, T]$ is used to transmit digitized information from $x(t)$ through the AWGN channel, where T is the symbol period.

Answer the following questions:

- (a) Provide a system block diagram including all processing units at both A and C in order to achieve your goal of recovering $x(t)$ at C .
- (b) Can we have $x(t)$ perfectly restored at C ? Justify your answer. If not, further remark on the sources of uncertainty, as well as how they contribute to making the restored signal $\hat{x}(t)$ not equal to $x(t)$.

A binary communication system with two equiprobable messages uses the following signals:

$$s_1(t) = \begin{cases} 1 & 0 \leq t < 1 \\ 2 & 1 \leq t < 2 \\ 0 & \text{otherwise} \end{cases}$$

$$s_2(t) = \begin{cases} 1 & 0 \leq t < 1 \\ -2 & 1 \leq t < 2 \\ 0 & \text{otherwise} \end{cases}$$

1. Find the energy of each of the transmitted signals.
2. Assuming that the channel is additive white Gaussian noise with power spectral density of $N_0/2$ watts/Hz, find the error probability of the optimal receiver (the one that minimizes the probability of error) and express it in terms of N_0 .
3. Assume that we have a two-path channel and the two received signals are given by

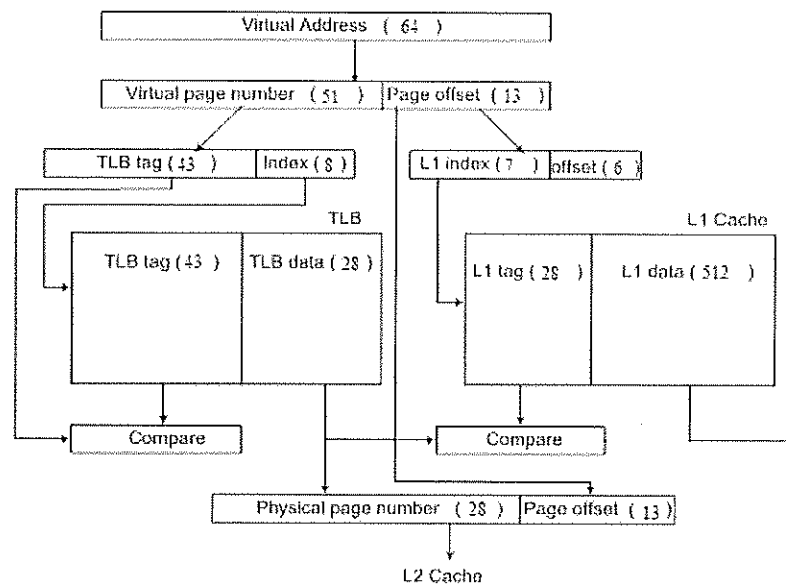
$$r_1(t) = s(t) + N_1(t), \quad r_2(t) = s(t) + N_2(t),$$

where $s(t)$ is the transmitted signal and where $N_1(t)$ and $N_2(t)$ are independent white Gaussian noise processes with power spectral density of $N_0/2$ and they are independent of the transmitted message. The receiver makes its decision based on the two received signals $r_1(t)$ and $r_2(t)$. Determine the structure of the optimum receiver and find its probability of error.

4. Now suppose that

$$r_1(t) = As(t) + N_1(t), \quad r_2(t) = s(t) + N_2(t),$$

where A is a constant known to the receiver. In this case what is the receiver's optimal decision rule?



The overall picture of a hypothetical memory hierarchy going from virtual address to L2 cache access is shown above. The page size is 8KB. The TLB is direct mapped with 256 entries. The L1 cache size is 32KB with 4-way set-associative design with 64-byte blocks. The virtual address is 64 bits and the physical address is 41 bits. The number of bits for each item is denoted. For example, virtual address (64) means the virtual address has 64 bits.

- A. Describe the procedure of a L1 data cache access illustrated by the above figure in details.
- B. In the above cache accessing procedure, can the TLB and the L1 cache be searched in parallel? You must justify your answer in details.
- C. Suppose the L1 cache size increases from 32KB to 128KB and other parameters remain unchanged. Can the TLB and the L1 cache be searched in parallel? If yes, answer the reason clearly; if not, state your reason and propose a solution to make this parallel search possible.

Computer Hardware 4

Fall 2011

The *test-and-set* spin lock is the simplest synchronization mechanism possible on most commercial shared-memory machines. This spin lock relies on the exchange primitive to atomically load the old value and store a new value. The lock routine performs the exchange operation repeatedly until it finds the lock unlocked (i.e., the returned value is 0).

```
tas:      ADDI      R2, R0, #1
lockit:   EXCH      R2, 0(R1)    //Atomic exchange value of R2 and memory 0(R1)
          BNEZ      R2, lockit
```

Unlocking a spin lock simply requires a store of the value 0.

```
unlock:   SW        R0, 0(R1)
```

The more optimized *test-and-test-and-set* lock uses a load to check the lock, allowing it to spin with a shared variable in the cache.

```
tatas:    LD         R2, 0(R1)
          BNEZ      R2, tatas
          ADDI      R2, R0, #1
          EXCH      R2, 0(R1)
          BNEZ      R2, tatas
```

Now consider a bus-based, symmetric shared memory system with 4 processors. Each processor has its own cache. Assume that processors P0, P1, and P2 are all trying to acquire a lock at address 0x100 (i.e., register R1 holds the value 0x100). The stall cycles resulting from processor operations are listed in the following table.

Operation	Stall Cycles
CPU read/write misses if satisfied by the memory.	100
CPU read/write misses if satisfied by a remote cache.	50
CPU write hits and generate an invalidation.	15

In the following questions, we have these assumptions: (1) the critical sections are 1000 cycles long; (2) the processors acquire the lock in the order of P0, P1 and P2; (3) the cache block containing the address 0x100 only has a valid copy in memory initially.

- Using the *test-and-set* spin lock, determine how many memory stall cycles each processor incurs before acquiring the lock.
- Using the *test-and-test-and-set* spin lock, determine how many memory stall cycles each processor incurs before acquiring the lock.
- How many bus transactions occur for each lock respectively?

Computer Hardware 5

Fall 2011

Considering the following MIPS-like code:

1. LW R1, 100(R2) // $R1 \leftarrow [100+R2]$
2. ADD R3, R1, R8 // $R3 \leftarrow R1+R8$
3. LW R5, 10(R3) // $R5 \leftarrow [10+R3]$
4. AND R8, R3, R6 // $R8 \leftarrow R3 \&\& R6$
5. SUB R4, R5, R7 // $R4 \leftarrow R5 - R7$
6. XOR R3, R1, R9 // $R3 \leftarrow R1 \oplus R9$

(a) Consider a processor with a single issue, in-order seven stage pipeline: instruction fetch (F), instruction decode / register read (D), execution / effective address generation (X), memory access stage 1, 2 and 3 (M1, M2 and M3), write-back (W). Assume that there are three forwarding paths to each of the ALU input: (1) the ALU output at the beginning of the M1 stage, (2) the ALU output at the beginning of the W stage and (3) the memory output at the beginning of the W stage. Complete the pipeline diagram showing the execution of the code on the processor. You answer should be in the format of the following table. Denote pipeline stalls with a “-”.

Instruction	1	2	3	4	5	6	7	8
1. LW R1, 100(R2)	F	D	X	M1	M2	M3	W				
2. ADD R3, R1, R8											
3. LW R5, 10(R3)											
4. AND R8, R3, R6											
5. SUB R4, R5, R7											
6. XOR R3, R1, R9											

(b) Assume the processor from part (a) is enhanced with load value prediction hardware. With this scheme, load instructions can speculatively obtain their values after the instruction fetch (F) stage. Therefore the load dependent instructions can execute with the speculative value smoothly and the pipeline doesn't stall. At the beginning of the load's WB stage, the processor will check between the true data value fetched from memory and the speculative value. For the above code, if the first load instruction (instruction 1) gets the *wrong* value from the prediction hardware and the second load instruction (instruction 3) gets the *correct* value, complete the pipeline diagram showing the execution of the code. Please devise a reasonable recovery method and show its operation in the diagram. You need pay attention to avoid the structural hazard. You also must use the format in part (a).

- a) Let a, b, m be positive integers where $m \neq 1$. Prove that $(a + b) \bmod m = (a \bmod m + b \bmod m) \bmod m$.
- b) Let c, m be positive integers where $m \neq 1$. The multiplicative inverse $\bmod m$ of the number c , denoted as $c^{-1} \bmod m$, is an integer e such that $(c \times e) \bmod m = 1$.

Let (c, m) denote the greatest common divisor of c and m .

Prove that if $(c, m) = d \neq 1$, then $c^{-1} \bmod m$ does not exist.

Hint: Provide a proof by contradiction in this part b).

Consider a directed acyclic graph $G = (V, E)$ that represents dependencies among a set of tasks. Each vertex in G corresponds to a task, and each edge $(u, v) \in E$ indicates that task u must complete before v can start. The graph is represented in an adjacency list form.

- (a) Assume that the execution time (or, delay) of the tasks is one unit of time. Derive an efficient sequential algorithm that computes all the pairs of nodes that can never be executing at the same time. Explain why your algorithm is correct. What is the time complexity of your algorithm, in terms of the number of edges and number of vertices? Show all the steps in your derivation of the time complexity.
- (b) For this part, assume that the execution time (or, delay) each task i is t_i where t_i is an integer and $t_i \geq 1$. Derive an efficient sequential algorithm that computes all the pairs of nodes that can never be executing at the same time. Explain why your algorithm is correct. What is the time complexity of your algorithm, in terms of the number of edges and number of vertices? Show all the steps in your derivation of the time complexity.

There is a flight of stairs with n steps. You can climb 1, 2 or 3 steps in one stride. Let t_n denote the number of different ways in which you can climb the n -step flight of stairs.

For example, $t_3 = 4$ with the four different methods of climbing the stairs being $\langle 3 \rangle$, $\langle 1, 2 \rangle$, $\langle 2, 1 \rangle$, $\langle 1, 1, 1 \rangle$; here $\langle 1, 2 \rangle$ represents climbing the first step separately, and the last two steps in one stride. In $\langle 1, 1, 1 \rangle$, each step is climbed separately.

Your answers to all the questions below must be justified.

- (a) Determine t_1 , t_2 and t_4 ; it is given that $t_3 = 4$.
- (b) Construct a recurrence relation for t_n , for any $n \geq 1$.
- (c) Consider a string of symbols. These symbols are represented in binary and have variable length. They are drawn from the set $\{0, 10, 110, 111\}$. Thus each string of x symbols has a length ℓ (in bits) that satisfies $x \leq \ell \leq 3x$. Derive a recurrence relation for T_n , the number of distinct n -bit strings.
- (d) Given an n -bit string, outline an efficient algorithm to identify the symbols in the string.
- (e) What are the difficulties posed in constructing an algorithm as in part (d), if the symbols are drawn from the set $\{0, 1, 10, 110, 111\}$?

A *perfect shuffle* of a list of $2n$ quantities $x_0, x_1, \dots, x_{2n-1}$ is the permutation

$$x_0, x_n, x_1, x_{n+1}, x_2, x_{n+2}, \dots, x_{n-1}, x_{2n-1}$$

We will use this definition later in this problem.

For integers $n \geq 0$ and let $\alpha \geq 0$ be a multiple of 2^{2n} . Let $A(n)$ be a $2^n \times 2^n$ array of points, numbered from α to $\alpha + 2^{2n} - 1$. A renumbering of $\{\alpha, \alpha + 1, \alpha + 2, \dots, \alpha + 2^{2n} - 1\}$ is defined to be a *2-D filling function* for $A(n)$ as follows. Divide $A(n)$ into four quadrants $A_0(n-1)$, $A_1(n-1)$, $A_2(n-1)$ and $A_3(n-1)$, each a $2^{n-1} \times 2^{n-1}$ sub-array of A . For a 2-D filling function

- the (new 2-D filling function) numbers of $A(n)$ must be distinct,
- the new numbers within any of the $A_i(n-1)$'s (for $0 \leq i < 4$) must be from an interval of $2^{2(n-1)}$ contiguous integers, and
- each of the $A_i(n-1)$'s must be (recursively) numbered by a 2-D filling function.

- (a) What is the perfect shuffle of a, b, c, d, e, f, g, h ?
- (b) Which of the following numberings of a 4×4 array is a 2-D filling function? Justify your answer.

0	1	2	3
4	5	6	7
8	9	10	11
12	13	14	15

(i)

0	1	2	3
7	6	5	4
8	9	10	11
15	14	13	12

(ii)

0	1	4	5
2	3	6	7
8	9	12	13
10	11	14	15

(iii)

- (c) Consider $A(n)$, a $2^n \times 2^n$ array of points where the element in row i and column j is indexed $i2^n + j$; here $0 \leq i, j < 2^n$. This is called the row-major indexing of (i, j) . Define the *shuffled row-major* index of (i, j) to be the number obtained by a perfect shuffle of the $2n$ -bit binary representation of the row-major index of (i, j) . Specifically, if the binary representation of the row major index of (i, j) is $x_0x_1 \dots x_{2n-1}$, then the binary representation of the shuffled row major index is.

$$x_0x_nx_1x_{n+1}x_2x_{n+2} \dots x_{n-1}x_{2n-1}$$

Construct the shuffled row-major indexing for a 4×4 array.

- (d) Prove that the shuffled row-major indexing for a $2^n \times 2^n$ array is a 2-D filling function.

Suppose we use a triangle mesh to represent a 3D object (see Figure 1), then we can discretely measure the shape on the mesh. Suppose we have stored the mesh in a graph: each vertex is a node, associated with its (x, y, z) coordinates, and each edge corresponds a path connecting nodes.

For example, given two vertices $\mathbf{p}_1, \mathbf{p}_2$,

$$\mathbf{p}_1 = \begin{pmatrix} x_1 \\ y_1 \\ z_1 \end{pmatrix}, \mathbf{p}_2 = \begin{pmatrix} x_2 \\ y_2 \\ z_2 \end{pmatrix},$$

the Euclidean distance between them is simply $|\mathbf{p}_1 \mathbf{p}_2| = |\mathbf{p}_2 - \mathbf{p}_1|$.

- (a) We usually want to compute the *geodesic curve* between two points, i.e., the path with the shortest length that traverses over the surface. This path can be discretely approximated on the mesh (graph) as $\{\mathbf{p}_1, \mathbf{p}_2, \mathbf{p}_3, \dots, \mathbf{p}_n\}$, composed of consecutive edges $[\mathbf{p}_i, \mathbf{p}_{i+1}]$, $i = 1, \dots, n - 1$, (each \mathbf{p}_i is a vertex). Given two vertices, describe your algorithm to find this approximate path and compute its curve length.
- (b) What is the area of a triangle $[\mathbf{p}_i, \mathbf{p}_j, \mathbf{p}_k]$? What is the approximate area of the model's surface?
- (c) How to compute the volume of a tetrahedron $[\mathbf{p}_i, \mathbf{p}_j, \mathbf{p}_k, \mathbf{p}_l]$?
- (d) Suppose a given surface ∂M is the boundary of a solid object M . You have the discrete triangle mesh representation of ∂M , can you compute the volume of M ? Please discuss the generality of your algorithm, and show whether it works for all kinds of geometry. Try to develop a robust and general algorithm.

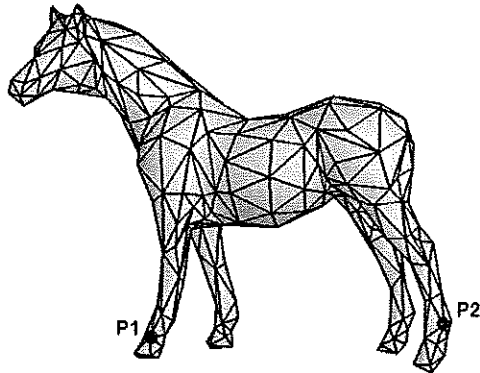


Figure 1: A triangle mesh.

- (a) Given two points $\mathbf{p}_1, \mathbf{p}_2$ on the E^2 plane, the *cross product* $\mathbf{p}_1 \times \mathbf{p}_2$ can be used to detect that with respect to the origin $\mathbf{q}(0, 0)$, whether $\mathbf{qp}_1 = (x_1, y_1)$ is at the clockwise (CW) or counterclockwise (CCW) side (about the origin) from $\mathbf{qp}_2 = (x_2, y_2)$. Illustrate the geometric interpretation of the cross product, and explain how to tell this by looking at $\mathbf{p}_1 \times \mathbf{p}_2$.
- (b) Based on the routine of (a), can you detect whether two line segments $[\mathbf{p}_1, \mathbf{p}_2]$ and $[\mathbf{p}_3, \mathbf{p}_4]$ are intersected? Write your intersection detection pseudo-code algorithm:
bool Check($\mathbf{p}_1, \mathbf{p}_2, \mathbf{p}_3, \mathbf{p}_4$),
which takes 2D coordinates $(x_i, y_i), i = 1, 2, 3, 4$ of these points as the input, and returns whether $[\mathbf{p}_1, \mathbf{p}_2]$ intersects $[\mathbf{p}_3, \mathbf{p}_4]$ or not.
Note: (1) assume $[\mathbf{p}_1, \mathbf{p}_2]$ and $[\mathbf{p}_3, \mathbf{p}_4]$ are not collinear; and (2) here you shall only use the routine in (a), i.e. cross product, for this detection.
- (c) With *Check()* operator developed in (b), given a set of n line segments $[\mathbf{p}_i, \mathbf{q}_i], i = 1, \dots, n$, how to detect whether or not any intersection exists? Can you do it in $O(n^2)$ time? Can you do it in $O(n \log n)$ time?
Hint: you can assume the line segments and their endpoints $(\mathbf{p}_i, \mathbf{q}_i)$ are sparsely located and are not degenerated: (1) no three endpoints are collinear; (2) no two endpoints locate in the same position; and (3) no three or more segments intersect at a same point.

Computer Application 5

Fall 2011

Wavelet transforms are used in image processing to filter the noise or compress the information. Let $X = (c_{n,0}, c_{n,1}, \dots, c_{n,2^j-1})$ be the image data. A simple wavelet transform, called Haar transform, obtains scaling coefficients $c_{j,k}$ and wavelet coefficients $d_{j,k}$ using following equations:

$$\left. \begin{aligned} c_{j,k} &= \frac{c_{j+1,2k} + c_{j+1,2k+1}}{2} \\ d_{j,k} &= \frac{c_{j+1,2k} - c_{j+1,2k+1}}{2} \end{aligned} \right\} \quad (1)$$

Here j and k identify the k^{th} element at j^{th} level, where $j = n, n-1, \dots, 0$ and $k = 0, 1, \dots, 2^j-1$ for data of size 2^n . For $j = n$, $X = (c_{j,k})$.

- Using (1), obtain Haar transform for data $X = (3, 1, 0, 4, 8, 6, 9, 9)$.
- Write equations similar to (1) that will generate X from the result obtained in (a)
- Generalize (b) to recreate X from $c_{j,k}$ and $d_{j,k}$ for $j < n$.
- Write an efficient algorithm for forward (1) and inverse (c) Haar transforms.

**Circuits & Systems
Problem #1**

Fall 2011

A BiCMOS amplifier is shown below. Calculate the small-signal voltage gain v_o/v_i . Assume $I_S = 10^{-16}$ A, $\beta_F = 100$, $r_b = 0$, $V_A \rightarrow \infty$, $\mu_n C_{ox} = 200 \mu\text{A/V}^2$, $V_t = 0.6\text{V}$ and $\lambda = 0$.

I_S : Reverse saturation current of the p-n junction

β_F : BJT current gain in forward active mode of operation

r_b : Base resistance of the BJT

V_A : Early voltage in BJT

$\mu_n C_{ox}$: Process transconductance parameter of MOSFET where μ_n is the mobility of electrons in the channel region and C_{ox} is the gate oxide capacitance per unit area.

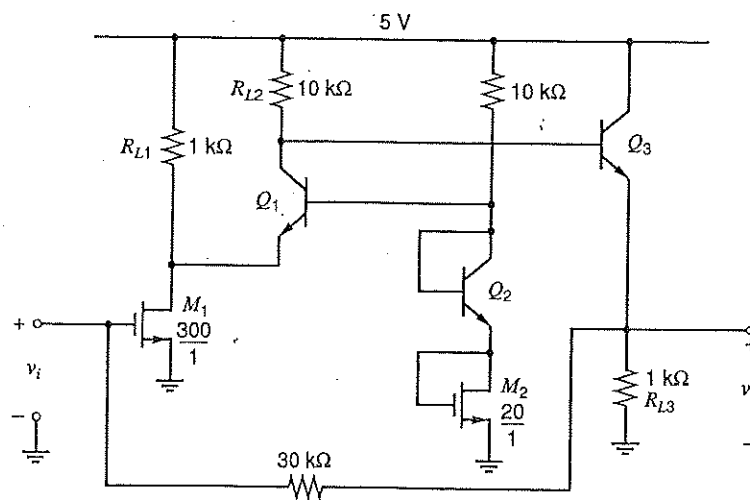
V_t : MOSFET threshold voltage

λ : MOSFET channel length modulation parameter

Note: $V_{BE} = 0.7\text{V}$.

Assume that the dc input is adjusted so that $I_{C1} = I_{C2}$. I_{C1} and I_{C2} are collector currents of transistors Q_1 and Q_2 , respectively.

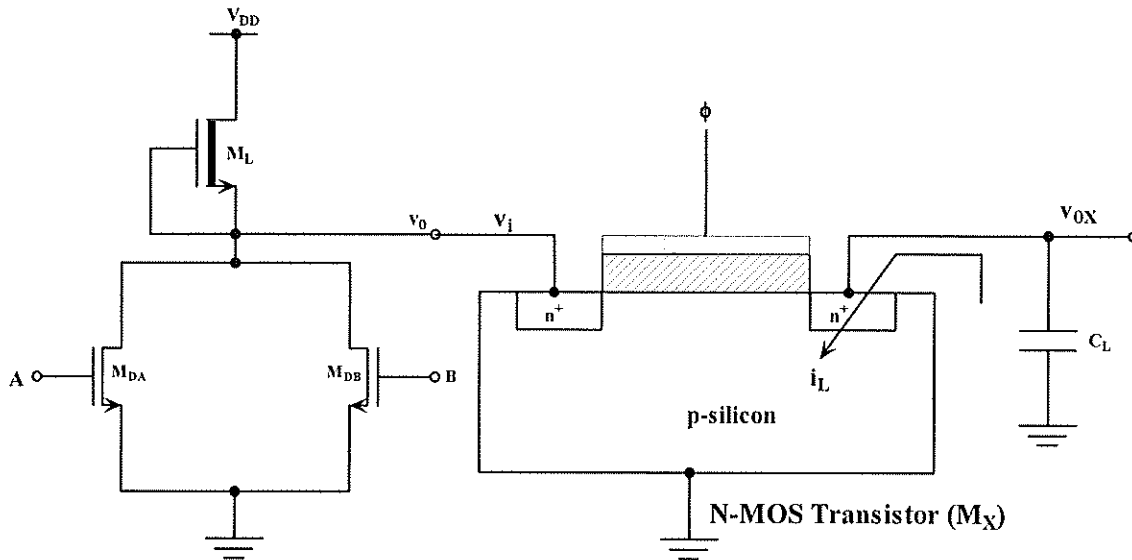
Use MOSFET I-V equation for the saturation region of operation.



Circuits & Systems
Problem #2

Fall 2011

- a) The following circuit is biased at $V_{DD} = 5V$. Assume that $K_N = 35 \mu A/V^2$. Also assume the width-to-length ratios of the load and driver transistors are $(W/L)_L = 1$ and $(W/L)_D = 4$, respectively. Let $V_{thD} = 0.8 V$ and $V_{thL} = -2 V$. Neglect the body effect and consider n-MOS transistor (M_X) is off. Determine the low output voltage of the circuit when $A = \text{logic 1}$ (5 V) and $B = \text{Logic 0}$ (0 V), and when both inputs are high (5 V). $K_N = \mu_n C_{ox}$ is the process transconductance parameter. V_{thD} and V_{thL} are threshold voltages of driver and load transistors, respectively.

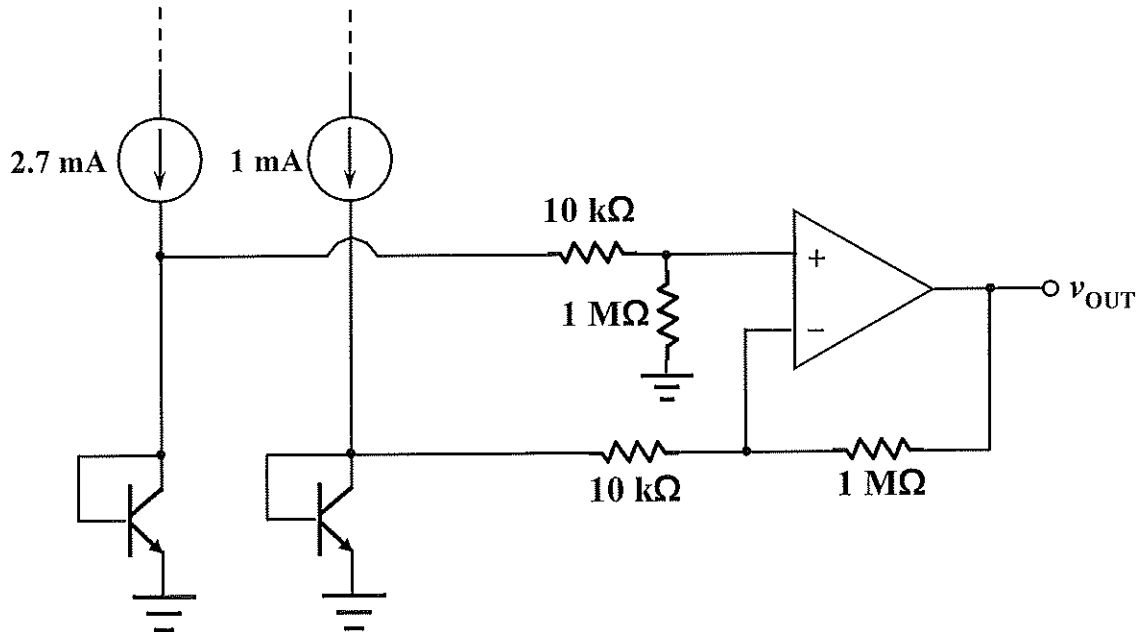


- b) Estimate the rate at which the output voltage, V_{0X} decreases with time. Assume the capacitor is initially charged to $V_{0X} = 4.2 V$. Let $C_L = 1 pF$ and assume the reverse-biased p-n junction leakage current is constant at $i_L = 1 nA$.

Circuits and Systems
Problem 3

Fall 2011

For an electronic thermometer circuit given below, answer the following questions.



- (a) Express v_{OUT} in terms of the ambient temperature T . Assume that the two transistors in the circuit are identical.
- (b) Discuss about the limit of the circuit.

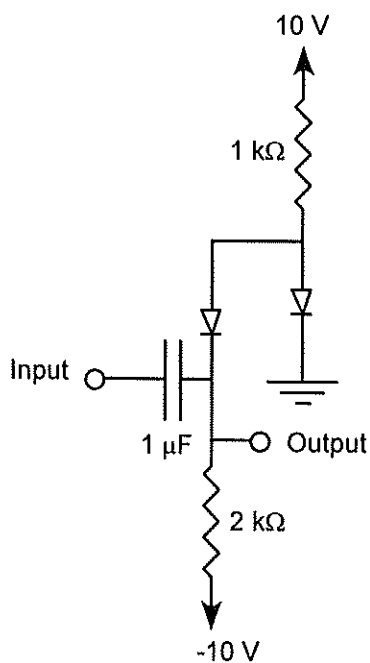
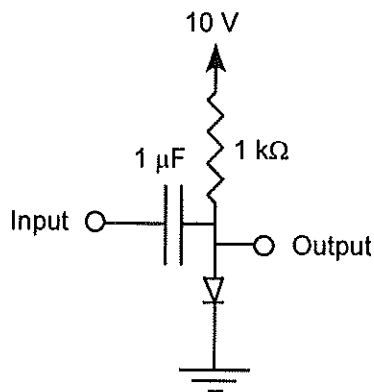
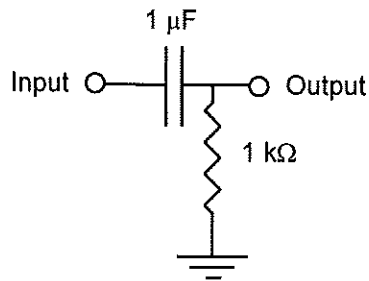
Circuits and Systems

Problem 4

Fall 2011

A 10 Volt p-p square wave at a frequency of 100 Hz is applied to the inputs of each circuit below.

Sketch the output waveforms, clearly indicating times and amplitudes.

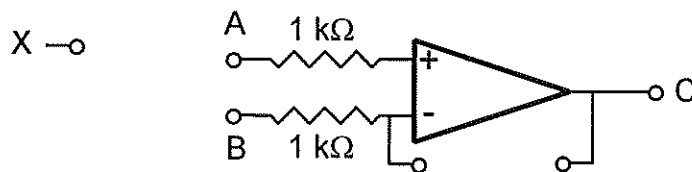


Circuits and Systems
Problem 5

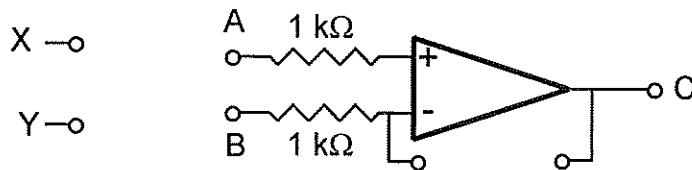
Fall 2011

You have two signals, X and Y, both varying between 0 and 1 Volt.

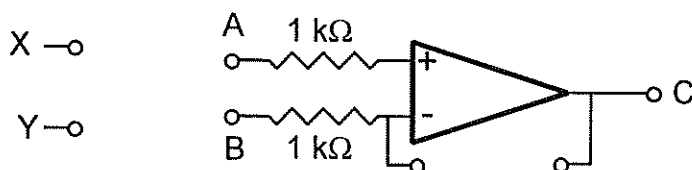
- a) Add components to the circuit below so that the output at point C is proportional to the signal at X. Estimate the maximum and minimum values at C.



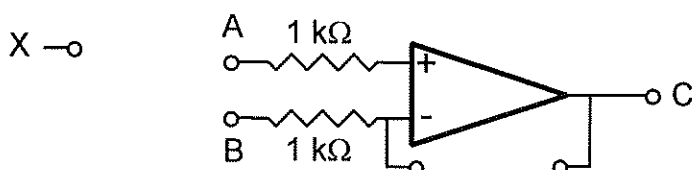
- b) Add components to the circuit below so that the output at point C is proportional to the sum of the signals at X and Y. Estimate the maximum and minimum values at C.



- c) Add components to the circuit below so that the output at point C is proportional to the difference of the signals at X and Y. Estimate the maximum and minimum values at C.



- d) Add components to the circuit below so that the output at point C is proportional to the logarithm of the signal at X. Estimate the maximum and minimum values at C.



Physical Electronics
Problem 3

Fall 2011

1. A p-n junction diode current can be looked upon as net recombination or generation of electron-hole pairs per unit time somewhere inside the diode. Explain the validity of this statement.
2. A forward biased light emitting diode (LED) made from a direct band gap material (band gap = 2.3 eV) draws 4.5 kA/cm^2 current when connected to an external terminal battery voltage of 2.6 V. The diode cross-section area is $90 \text{ } \mu\text{m}^2$. In this semiconductor, 92% of recombinations are known to be radiative. The diode packaging permits 85% of emitted photons to exit from the package, the remaining being absorbed by the packaging material. The LED is made of a p⁺-n junction i.e. the p-side is much more heavily doped than the n-side.

For this case, determine:

- a) Number of photons coming out of the LED/sec.
- b) Heat dissipated inside the diode material (in Watts).
- c) Efficiency of the LED to convert electric energy from a battery to externally observable light energy.
- d) Where is most of light generated inside the diode? Explain giving reasons.

State any assumptions made. Magnitude of an electron charge $q = 1.6 \times 10^{-19} \text{ C}$.

Physical Electronics
Problem 4

Fall 2011

Consider a p-type semiconductor bar of length L in equilibrium with an acceptor impurity density distribution $N_A(x)$, where $0 \leq x \leq L$ is distance along the bar. Assume 100% impurity ionization. $N_A(x) \gg n_i$, the intrinsic carrier density for all values of x .

- a) If $N_A(x)$ is known to be uniform i.e. constant with distance x along the bar, find the value of equilibrium electric field $E_o(x)$. Show intermediary steps.
- b) Repeat part a) above if $N_A(x)$ is now a linear function of x i.e. $N_A(x) = C + D x$, where C and D are constants and $D > 0$.
- c) Determine $N_A(x)$ if $E_o(x)$ in the material is known to be constant i.e. $E_o(x) = E$, where E is a constant < 0 .
- d) For part c) above, qualitatively plot equilibrium energy band diagram showing all pertinent energy levels. Label your diagram carefully. Also plot $E_o(x)$ and equilibrium electrostatic potential $V_o(x)$ as a function of x for $0 < x < L$.
- e) For part c) above, is the material neutral i.e. is the space charge zero at position x ? Explain clearly. Where are the charges that produce the field located?

Physical Electronics
Problem 5

Fall 2011

An n-channel MOSFET with channel width $W = 20 \mu\text{m}$ and channel length $L = 1 \mu\text{m}$, oxide thickness $t_{ox} = 5 \text{ nm}$ and uniform substrate doping $N_A = 10^{15} \text{ cm}^{-3}$, is used as a voltage controlled resistor. Neglect body effect. For this device, the current voltage relationship is given by:

$$I_D = \frac{W}{L} \mu_n C_{ox} \left[(V_{GS} - V_{Tn}) V_{DS} - \frac{V_{DS}^2}{2} \right] \text{ where } I_D \text{ is the drain current, } \mu_n = 550 \text{ cm}^2/\text{V.s} \text{ is channel electron}$$

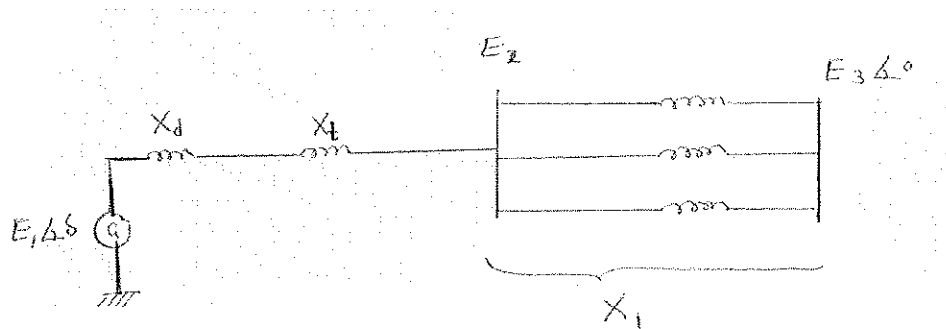
mobility, C_{ox} is oxide capacitance per unit area, V_{GS} is gate to source voltage, V_{Tn} is threshold voltage, V_{DS} is drain to source voltage. $kT/q = 26 \text{ mV}$ where k is Boltzmann constant and T is absolute temperature, $q = 1.6 \times 10^{-19} \text{ C}$ is magnitude of electron charge and intrinsic carrier density $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$. Relative permittivity of oxide $\epsilon_{ox} = 3.9$ and permittivity of free space $\epsilon_0 = 8.854 \times 10^{-14} \text{ F/cm}$.

Depletion width $d = \sqrt{\frac{2\epsilon_{rs}\epsilon_0\phi_s}{qN_A}}$ where relative permittivity of silicon $\epsilon_{rs} = 11.8$ and ϕ_s is silicon surface potential.

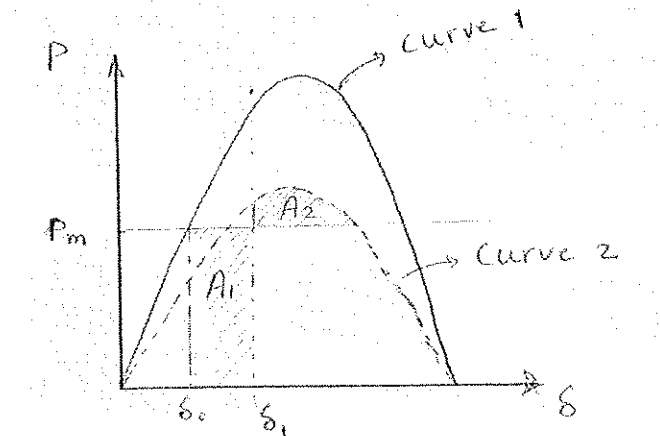
For this device, determine the following stating any assumptions made:

- Calculate the inversion layer charge density (in C/cm^2) required for the MOSFET to act as a $2.5 \text{ k}\Omega$ resistor between the source and the drain terminals at very low values of V_{DS} . What is the corresponding number density of charge carriers (number/ cm^2)? Show all the intermediary steps.
- Calculate the value of V_{GS} in excess of V_{Tn} required to obtain the inversion charge density in part a) above.
- Compute the depletion charge density at on-set of strong inversion in this device and compare it to the inversion charge density in part a) above.
- From the results of part c) above, can you justify neglecting the inversion charge density while calculating the value of threshold voltage V_{Tn} ? A qualitative explanation is required.

The synchronous generator shown in the following figure is connected to infinite bus E_3 through the generator stator reactance X_d , transformer reactance X_t , and transmission line impedance X_1 . The generator is modeled using the classical model (with constant internal voltage E_1 .) The generator is delivering active power P_0 under the internal voltage $E_1 \angle \delta_0$ where $\delta_0 = 30^\circ$. At time $t=0$ a symmetric three-phase fault with zero impedance occurs at bus 2 between the generator bus and the infinite bus.



- 1- What changes occur to the delivered power by the generator to the grid immediately after the fault?
- 2- Suppose that the fault lasts for t_1 seconds. What changes occur to the generator angular speed ω ?
- 3- Suppose that curve 1 in the graph shown below represents the variation of active power as a function of δ before the fault has occurred where P_m is the input mechanical power from turbine and δ_0 is the generator internal voltage angle prior to the fault. When the fault is removed at t_1 resulting in the generator's angle δ_1 , one of the parallel transmission lines are dropped resulting in the variation of after-fault active power P_2 as a function of δ shown in curve 2. Neglecting the stator and transformer reactances, find the maximum available power $P_{2\max}$ as a function of P_m .



- 4- In Part 3, assume that $P_{2\max}$ is greater than P_m , what can be said about the areas A1 and A2 if the generator is stable after the fault removal.

Figure 1. shows PWM inverter applied as a compensator.

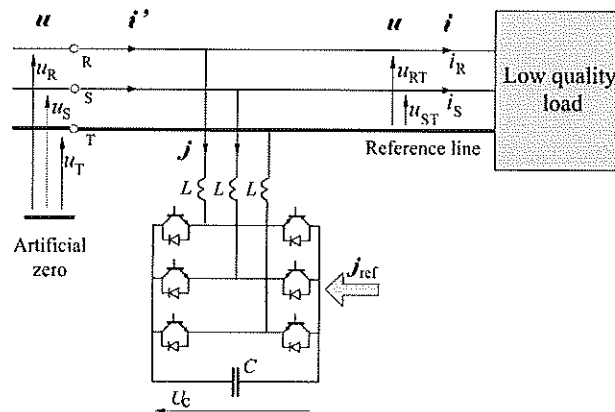


Fig.1

Develop formula for the reference signal j_{ref} if the compensator is to reduce:

- A. The load reactive current,
- B. The load unbalanced current,
- C. The load current harmonics.

- A. Explain how commutation notches and spikes, as shown in Fig. 2, occur in three-phase AC/DC converters.

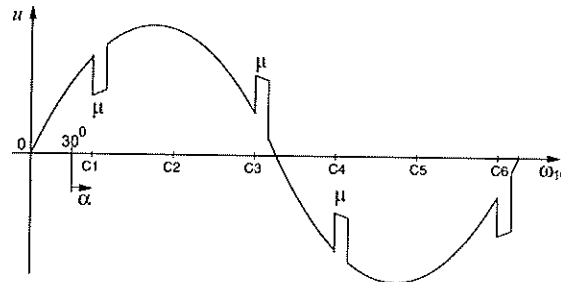


Fig. 2

- B. Develop formula for calculating commutation angle μ .
- C. Develop formula for calculating the voltage harmonics caused by commutation.

- 1) Draw the equivalent circuit of a single-phase transformer. What kind of measurements have to be done to determine the parameters of this circuit?
- 2) Draw the phasor diagrams of currents and voltages, one for the inductive and one for pure resistive load. Show when the voltage regulation is greater.
- 3) A single phase transformer built (in Europe) for the rated frequency of 50 Hz is going to be connected to the power line (in US) of rated voltage and 60 Hz frequency. Will the power losses in the transformer increase or decrease with respect to those at 50 Hz frequency (assuming the transformer is loaded by the rated current in both circumstances). Explain what kind of power losses and why.
- 4) 3 single-phase transformers of the turn ratio 10:5 are connected to the 3 phase line of 220 V line voltage. Their primary and secondary windings are connected, first both in Δ and next both in Y.
 - Draw the circuit diagrams for both cases
 - What are the secondary phase voltage and the line voltage in each of the two connections?

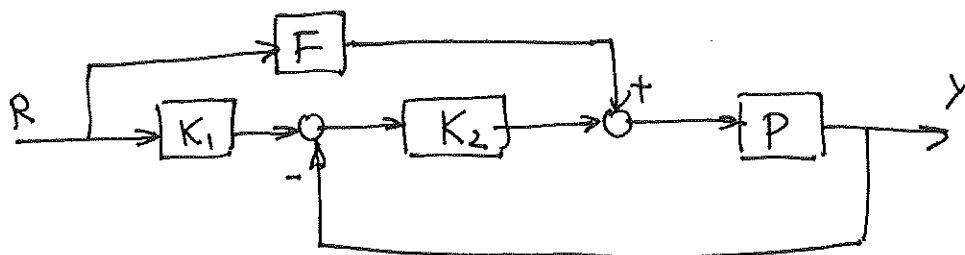
- 1) What are the differences in a design between 3-phase induction slip-ring motor and squirrel cage motor? Which one of these two motors would you recommend to drive the fan and which to drive a long fully loaded belt conveyer? Explain why.
- 2) Draw the equivalent circuit of induction motor without core losses parameter and show where the mechanical power and stator and rotor winding losses dissipate. What is the mechanical output power at zero speed and at synchronous speed?
- 3) What are the similarities in the operation of induction motor and transformer? In which of these two machines the no-load current is greater (related to their rated currents)? Explain why.
- 4) If you could vary the supply parameters (voltage and frequency) what would you do to change the speed of induction motor to keep the constant electromagnetic torque? Use torque-speed characteristic to explain.

Let a unity feedback system with a plant model be given by

$$G(s) = \frac{K(\tau s + 1)}{s(s + 1)(Ts + 1)}.$$

1. Sketch Nyquist diagrams for $\tau > T > 0$ and $T > \tau > 0$ respectively.
2. Using Nyquist stability criterion, find the stability condition of the system.
3. Using Nyquist stability criterion, find the relationship between τ and T so that the system is stable for every $K > 0$.

Let a feedback control system be shown below



1. Find the transfer function from R to Y .

2. Let

$$P(s) = \frac{10}{s(s+1)}, \quad K_2(s) = \frac{2(s+1)}{s+2}$$

find constants F and K_1 so that the steady state error with respect to a ramp $R(t) = t$ is zero.

3. Can you find constants F and K_1 so that the steady state error with respect to $R(t) = \sin t$ is zero?

AUTOMATIC CONTROL 4**FALL 2011**

Consider a unity negative feedback system with loop transfer function

$$GH(s) = \frac{K(s+1)(\alpha s + \beta)}{s^2(s-1)}.$$

- (a) Sketch its Nyquist plot for the case $\alpha = 0$ and $\beta = 1$.
- (b) Suppose that $\alpha > 0$ $\beta > 0$. Use Routh-Hurwitz method to determine the stability range of K as a function of α and β .
- (c) What is the Nyquist plot for the case $\alpha = 1$ and $\beta = 10$?

A causal linear and time-invariant (LTI) system has the frequency response

$$H(j\omega) = \frac{4 + j\omega}{6 + 5j\omega - \omega^2},$$

where $j = \sqrt{-1}$.

1. Determine a differential equation relating the input $x(t)$ and output $y(t)$ of the above LTI system.
2. Find the output $y(t)$ of the above LTI system when the input is

$$x(t) = te^{-t}u(t),$$

where $u(t)$ is the unit-step signal defined as 1 for $t > 0$ and 0 otherwise.

3. Let $Y(j\omega)$ be the Fourier transform of the signal $y(t)$. Find a signal $z(t)$ such that its Fourier transform is $Z(j\omega) = j\omega Y(j\omega)$.

A causal linear-time-invariant system with *initial rest* ($y[n] = 0$, for $n < 0$) is described by a difference equation:

$$y[n] = a_0x[n] + a_1x[n-1] + b_1y[n-1] + b_2y[n-2],$$

where a_0 , a_1 , b_1 , and b_2 are all real numbers. The z -transforms for $x[n]$, $y[n]$ are denoted by $X(z)$, $Y(z)$, respectively.

1. Determine the transfer function $H(z) = \frac{Y(z)}{X(z)}$ and the associated region of convergence (ROC) in terms of b_1 and b_2 .
2. Specify the condition in terms of b_1 and b_2 for the discrete-time Fourier transform (DTFT) $H(e^{j\omega})$ to exist, where $j = \sqrt{-1}$. Then, determine $H(e^{j\omega})$ directly from the result in Part 1.
3. Given $x[n] = \begin{cases} 1, & n = 0, \\ 0, & \text{otherwise} \end{cases}$, $y[4] = 1$, and $y[5] = 2$, find the relationship among a_0 , a_1 , b_1 , and b_2 . Then, determine the algebraic formula of $y[n]$, for $n > 5$, in terms of n , a_0 , a_1 , b_1 , and b_2 .
4. Determine the z -transform $Y(z)$ for the result in Part 3. Based on $Y(z)$, write the condition for $y[n]$ to be a *sinusoidal* signal as $n \rightarrow \infty$.

Consider two real jointly wide sense stationary (WSS) random processes $a(t)$ and $b(t)$ with zero mean and auto-correlation function $R_{aa}(\tau) = E[a(t + \tau)a(t)]$ and $R_{bb}(\tau) = E[b(t + \tau)b(t)]$, respectively, and cross-correlation function $R_{ab}(\tau) = E[a(t + \tau)b(t)]$.

1. For a process $x(t) = a(t) \cos(\omega_0 t) - b(t) \sin(\omega_0 t)$, compute its mean $E(x(t))$ and auto-correlation function $E[x(t + \tau)x(t)]$, where $\omega_0 > 0$ is a given deterministic frequency.
2. Is $x(t)$ a WSS random process? If Not, provide conditions on $R_{aa}(\tau)$, $R_{bb}(\tau)$ and $R_{ab}(\tau)$ under which $x(t)$ is a WSS process.
3. Under the same conditions as obtained in (2) compute the auto-correlation function of $y(t) = a(t) \sin(\omega_0 t) + b(t) \cos(\omega_0 t)$, as well as the cross-correlation function of $R_{xy}(t + \tau, t) = E[x(t + \tau)y(t)]$.
4. We form two complex random processes: $w(t) = a(t) + jb(t)$ and $z(t) = x(t) + jy(t)$, where $j = \sqrt{-1}$. Show that $S_z(f) = S_w(f + f_0)$, where $S_z(f)$ and $S_w(f)$ are power spectral density functions of $w(t)$ and $z(t)$, respectively, and $f_0 = \frac{\omega_0}{2\pi}$.

Consider a binary communication system between node A and node B, where the received signal at B is $Y = W_0$ when node A sends bit 0, and $Y = S + W_1$ when node A sends bit 1 to B. Here, W_j denotes the received noise at B when bit $j \in \{0, 1\}$ is transmitted, whose probability distribution function (PDF) is given by $P_{W_j}(w)$, and $S > 0$ is a positive random variable with PDF $P_S(x)$ and independent of W_j . Let $\pi_j = \Pr(j)$ denote the prior probability of bit $j \in \{0, 1\}$.

1. To minimize the average probability of error $P_e = \Pr(j \neq \hat{j})$, where $\hat{j} \in \{0, 1\}$ denotes the detected bit at B given Y , what is the corresponding decision rule (in terms of a function of Y)?
2. If W_j is Gaussian distributed with zero mean and σ_j^2 variance, and $S > 0$ is a deterministic variable, simplify your decision rule.
3. Under the decision rule in (2), is it possible to have $\alpha + \beta = 1$, where $\alpha = \Pr(\hat{j} = 1|j = 0)$ and $\beta = \Pr(\hat{j} = 0|j = 1)$, justify your answer.

An equally likely binary message is transmitted across an additive white Gaussian noise (AWGN) channel with power spectral density of $N_0/2$ Watts/Hz using the following signal set.

$$\begin{cases} s_0(t) = 0 & 0 \leq t < T \\ s_1(t) = \sqrt{\frac{E}{T}} & 0 \leq t < T \end{cases}$$

1. Find the probability of error for the optimal receiver (that which minimizes the probability of error).
2. The following demodulator is used in the receiver.

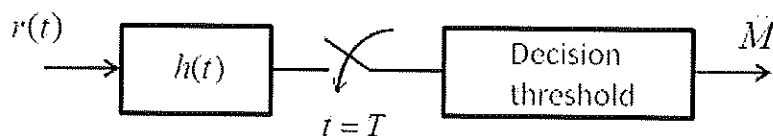


Figure 1: Demodulator

where

$$h(t) = \begin{cases} e^{-At} & 0 \leq t < T \\ 0 & \text{otherwise.} \end{cases}$$

- (a) Find the threshold in the decision threshold block that minimizes the probability of error.
- (b) Find the probability of error for this demodulator.
- (c) Evaluate the increase of transmitted energy required so that this receiver achieves the same error probability as the optimal receiver.

Duration: 4 Hours

MS COMPREHENSIVE / PhD QUALIFYING EXAM

Exam ID: Sp-212-00

- The exam consists of 40 questions divided in eight groups of five questions:

COMPUTERHardware
Software
ApplicationsELECTRONICSCircuits and Systems
Physical ElectronicsPOWERSYSTEMSAutomatic Control
Communications & Signal Processing

- Each student must answer **Six (6) questions**:

MS: Students taking the test only as MS-Comprehensive exam can answer **ANY six (6) questions**.

PhD: Students taking the test as part of the Qualifying Review **MUST** answer a **TOTAL of (6) questions**:
5 questions from any of the groups **in their declared major area**. The sixth question can be from any group.

NOTE: All the problems have been made as clear and error free as possible. The person proctoring the test cannot answer any questions about the content of the problems. If you believe that the problem is not clear or is in error, write the assumptions or corrections that you feel are appropriate; then work the problem completely.

- During the Exam:

1. **Do not use your name or lsu id on any test materials.** If you do, it will not be graded.
2. Do not write on the question booklet or the folder.
3. Do not un-staple the exam.
4. For your answers use a single side of the paper.
5. Number the problem (hardware 1, automatic control 3, etc.) And number the pages (1, 2, 3, etc.)
6. Start each problem on a new page.
7. Extra answer sheets are provided by the exam proctor.
8. You will be permitted to use an **ECE provided calculator only**.

- After The Exam:

1. Put your question book and completed answer sheets in the envelope provided, and seal it.
2. Put all other un-used, scribbled on or otherwise ungradable answer sheets in the folder.
3. **Nothing outside of the envelope will be graded, no exceptions.**

CIRCLE THE SIX (6) PROBLEMS THAT YOU WISH GRADED:

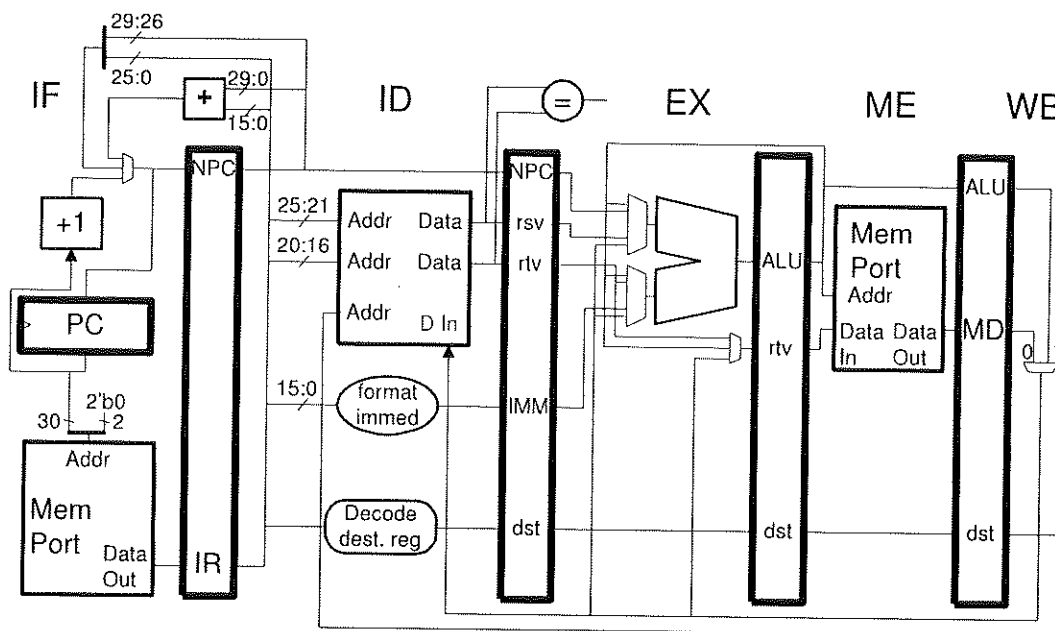
Computer - Hardware	1	2	3	4	5
Computer - Software	1	2	3	4	5
Computer - Applications	1	2	3	4	5
Electronics - Circuit & Systems	1	2	3	4	5
Electronics - Physical Electronics	1	2	3	4	5
Power	1	2	3	4	5
Systems - Automatic Control	1	2	3	4	5
Systems - Communications & Signal Processing	1	2	3	4	5

In the MIPS ISA, as in other RISC ISAs, an instruction either does arithmetic or accesses memory, but not both. Shown below are two hypothetical new MIPS instructions which break this rule. The first adds the contents of two registers and writes the sum to memory. The second adds a register to an immediate and writes the sum to memory.

```
add (r1), r2, r3    # Mem[r1] = r2 + r3
addi (r1), r2, 3    # Mem[r1] = r2 + 3
```

(a) Modify the illustrated implementation so that it can execute these instructions. (Sketch the changes, and adjacent unchanged components.) The first priority is speed, the second is cost. Assume that the memory port is on critical path.

The modified implementation should still implement the original MIPS instructions, including loads and stores.



(b) Suppose that the cost of implementing these new instructions would be offset by removing some capability from the illustrated implementation **without changing the ISA**. Describe a capability to be removed and provide an argument, including sample code, that performance would be faster with the new instructions.

The sample code should be in part slowed by the removed capability but sped by the new instructions. (Show the corresponding code without the special instructions.)

A program needs to compute an integer expression of the form $a_1k_{1j} + a_2k_{2j} + a_3k_{3j} + \dots$ where the $k_{ij} \in [1,31]$ are small integer constants and the range of i and j are of moderate size. There will be a large number of different integer values for the a_i .

Two methods of performing this computation appear below. Method 1 is a straightforward technique that stores the values of k in memory. In Method 2 the values of k appear as constants, with j selecting the correct set.

```
// Method 1
x = a1 * k1[j] + a2 * k2[j] + a3 * k3[j] ... ;

// Method 2
switch ( j ) {
  case 0: x = a1 * 3 + a2 * 7 + a3 * 2 + ... ; break;
  case 1: x = a1 * 2 + a2 * 12 + a3 * 6 + ... ; break;
  ...
}
```

(a) Consider a system with a perfect instruction and data cache. The overhead of the `switch` statement is 4 instructions. The system does **not** have an integer multiply instruction that takes an immediate operand. Given typical instruction latencies, why might Method 2 be faster in this system?

Why would it not make a difference if there were integer multiply instructions that took an immediate operand?

(b) Next, consider a system with a normal instruction and data cache. Provide an estimate of the relative size of the instruction cache and data cache needed for each method. Use the ISA of your choice, and state any assumptions about the ISA (such as the size of instructions). State any assumptions about the characteristics of the system.

In an out-of-order execution processor, a load instruction may obtain its address and value before a preceding (in program order) store instruction's address generation. In this case, if the processor executed the load instruction without any consideration about the earlier store instruction, program correctness would be violated if both instructions had true data dependence. Usually, we have two policies: (A) a conservative solution is stalling the load and its dependent instructions until the early store's address generation; (B) another alternative is predicting the memory dependence between loads and preceding stores. Memory dependence prediction allows some loads to bypass early stores if no dependence predicted. Otherwise, if dependence predicted, load values can be forwarded from the latest early stores without cache access. At the commit stage of stores, the processor checks correctness of predictions, if not, loads and their dependent instructions would be re-executed.

Now consider a two-issue, out-of-order execution pipeline with following stages: Instruction Fetch (IF), Decode (ID), Issue (IS), Execution / Address Generation (EX), Write Result (WR), Commit (CT). There are two integer ALU units, two load/store units and one MUL unit.

For the following code section, the EX stage for MUL instructions requires 10 cycles. All other instructions' EX stages have only 1 cycle. Please note that SW instructions only write cache in CT stage.

1. MUL	R2, R11, R12
2. SW	R1, 0(R2)
3. LW	R3, 20(R4)
4. ADD	R5, R3, R6
5. LW	R7, 100(R8)
6. SUB	R9, R7, R8
7. ADDI	R10, R5, 20

1. If this pipeline employs the policy (A) mentioned above for memory dependence, show execution steps with timing for the above code section.
2. If this pipeline employs the policy (B) mentioned above for memory dependence, the memory dependence predictor predicts that there is no dependence for both loads. Two loads (inst. 3 and 5) are executed without stalls. However, after the store address generation, instruction 3 has a true dependence with instruction 2 but instruction 5 doesn't have, show execution steps with timing for the above code section.
3. Design a memory dependence predictor. The predictor would provide three predictions: dependence, no dependence, maybe. If the prediction were maybe the load would wait. Draw a diagram for your design and specify the circumstances for each prediction.

Assume a symmetric shared-memory multiprocessor system that takes 100 cycles for a memory access and 300 cycles for a cache-to-cache transfer. A program running on this machine spends 60% of its time stalled on memory accesses and 20% of its time stalled on synchronization. A special prefetching, producer-initiated communication, can improve the system performance as follows:

- Of these memory stalls, 20% are due to producer-consumer data access patterns where the writer of data can identify the processor that will read the value next. In these cases, producer-initiated communication can directly transfer data to the cache of the next processor needing the data. This will reduce the latency of these memory accesses from 300 cycles for a cache-to-cache transfer to 1 cycle for a cache hit.
- Another 30% of the memory stalls are due to migratory data patterns where data move from one processor to another, but the migration path is unclear to the source processor. In this case, a producer-initiated communication can reduce the memory access latency from 300 cycles to 100 cycles by flushing the data back to memory.
- With a certain kind of optimizations, all synchronization overheads can also be reduced by 40% with producer-initiated communication.

- (a). Assuming no other overheads, what's the reduction in execution time with producer-initiated communication?
- (b). What memory system and program code features are required for implementing producer-initiated communication? (Hint: Cache coherence protocols and User-Specific hints may be needed).

Suppose that we have a set of activities to schedule among a large number of lecture halls. Let $A = \{a_0, a_1, \dots, a_{n-1}\}$ denote the set of activities; each activity a_j has a start time s_j and a finish time f_j . We wish to schedule all the activities using as few lecture halls as possible. Give an efficient greedy algorithm to determine which activity should use which lecture hall. Prove your algorithm correct and derive its time complexity.

A binary *heap* data structure is an array object that we can view as a nearly complete binary tree. Each node of the tree corresponds to an element of the array. The tree is completely filled on all levels except possibly the lowest, which is filled from the left up to a point. For an element at array location j , its parent is at location $\lfloor j/2 \rfloor$, its left child is at location $2j$, and its right child is at location $2j+1$. In a *max-heap*, for each node, its value is greater than or equal to the value of each of its children.

Design an efficient algorithm to find and delete an element with the smallest value in a max-heap. Determine the time complexity of your algorithm and sketch reasons for its correctness.

The *root* of a directed graph $G = (V, E)$ is defined as a vertex $u \in V$ from which there is a directed path to all the other vertices in the graph G .

The *sink* of a directed graph $G = (V, E)$ is defined as a vertex $u \in V$ to which there is a directed path from all the other vertices in the graph G .

- (a) Design an efficient sequential algorithm to determine if a directed acyclic graph has both a *root* and a *sink*. Prove its correctness. Analyze its running time. Is your algorithm the most efficient sequential algorithm one can design for this problem? Explain.
- (b) Design an efficient sequential algorithm to determine if an arbitrary directed graph (which may or may not have cycles) has both a *root* and a *sink*. Prove its correctness. Analyze its running time.

In each part below, you are given a loop that accesses scalar variables x and y . In each case, assume that the only dependences that arise are those due to the scalar variables x and y . Also, there are no other accesses to x and y .

- (a) Can you execute the iterations of the following loop in parallel? Explain your answer. Show the final code in case you are able to parallelize this loop.

```
do  $i = 1, N$ 
   $\dots = x + y$ 
   $y = \dots$ 
   $x = \dots$ 
   $\dots = \dots y \dots$ 
enddo
```

- (b) Can you execute the iterations of the following loop in parallel? Explain your answer. Show the final code in case you are able to parallelize this loop.

```
do  $i = 1, N$ 
   $\dots = x + y$ 
   $y = \dots$ 
   $x = \dots$ 
   $\dots = \dots x \dots$ 
enddo
```

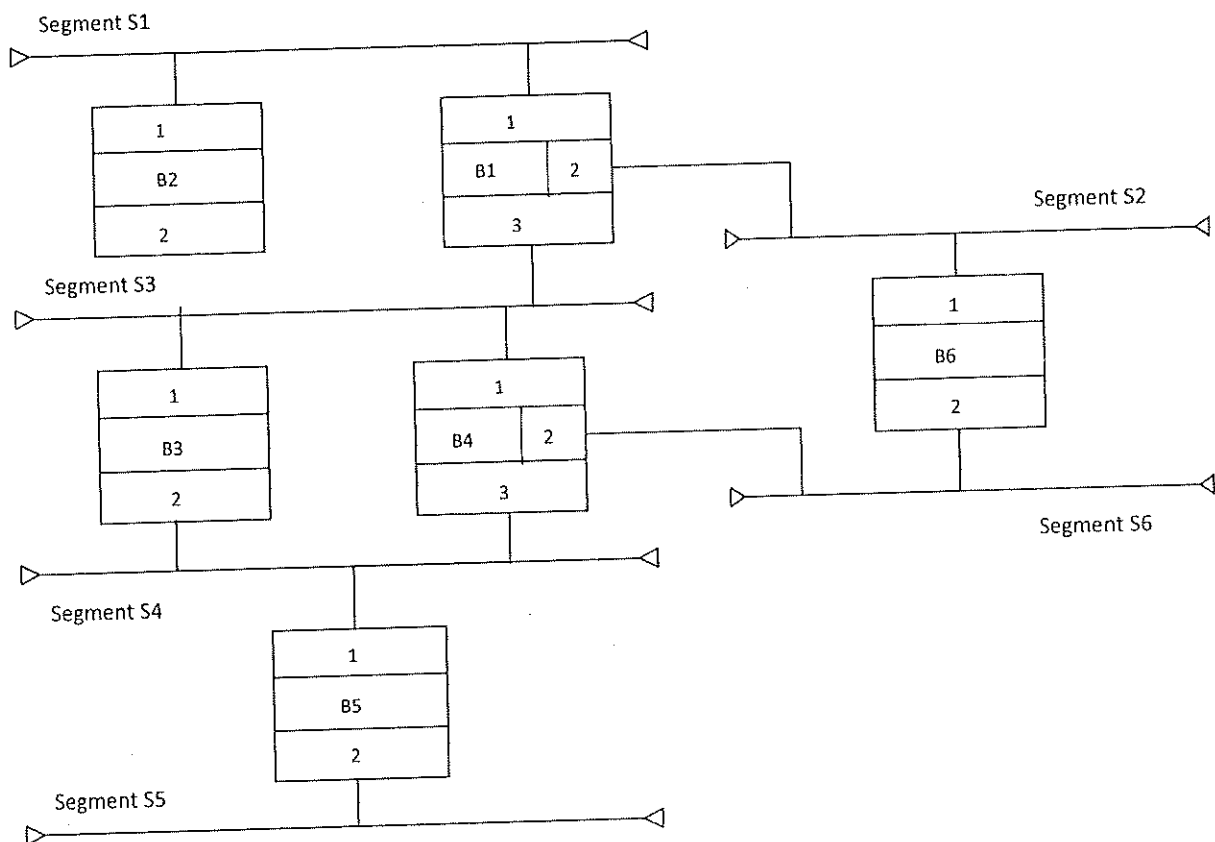
- (c) Can you execute the iterations of the following loop in parallel? Explain your answer. Show the final code in case you are able to parallelize this loop.

```
do  $i = 1, N$ 
   $x = x + y$ 
   $y = \dots$ 
   $\dots = \dots y \dots$ 
   $\dots = \dots x \dots$ 
enddo
```

Computer Application 1

Spring 2012

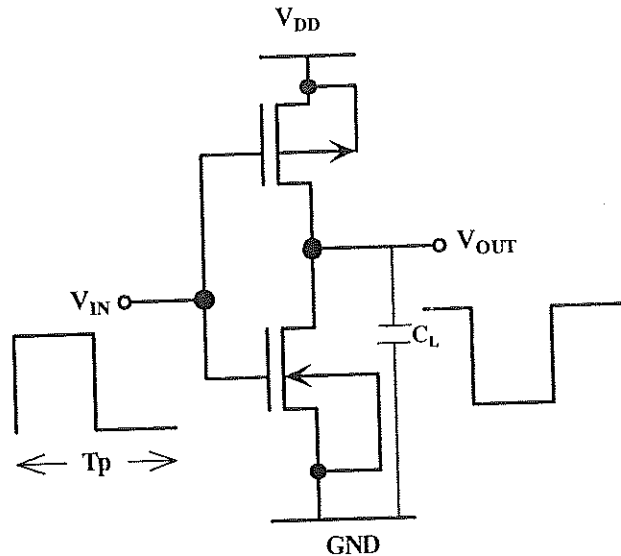
- (a) If the bit string 01110111110111110 is bit stuffed, what is the output string?
- (b) In both IP and ATM, the checksum covers only the header and not the data. Why do you suppose this design was chosen?
- (c) A network has been allocated a block of 1024 contiguous class C addresses from 200.30.0.0 through 200.30.3.255. Assuming the CIDR addressing scheme, obtain both address mask and *netid* of this network.
- (d) Consider a bridged LAN shown below. The unique identifier of each bridge is shown inside the box representing the bridge together with the port numbers in the inner boxes connecting the bridge to each segment. Typically, the additional bridges on each segment are added to improve reliability in the event of a bridge failure. Also, assume that the LAN is just being brought into service, all bridges have equal priority, and all segments have the same designated cost (bit rate) associated with them. Determine the active spanning tree topology. Repeat your exercise if segments S1, S4, and S6 offer a bit rate of 10Mb/sec, while S2, S3, and S5 provide a data rate of 100 Mb/sec.



Spring 2012

Circuits and Systems Problem 1

a) For the CMOS inverter shown below, calculate and plot the current that flows through the transistor as a function of $0 \leq V_{IN} \leq V_{DD}$.



Given: $V_{DD} = 5V$

For n-MOSFET:

$$\mu_n C_{OX} = 20 \mu A/V^2$$

$$W/L = 2 \text{ and } V_{th,n} = 1V$$

For p-MOSFET:

$$\mu_p C_{OX} = 10 \mu A/V^2$$

$$W/L = 4 \text{ and } |V_{th,p}| = 1V$$

Where $V_{th,n}$ and $V_{th,p}$ are threshold voltages of n-and p-MOSFETs. L and W are channel length and gate width of the MOSFET. μ is the mobility of carriers in the channel region. C_{OX} is the gate oxide capacitance /area.

MOSFET I-V Relations:

$$I_D = 0.5\mu C_{OX}(W/L)\{2(V_{GS}-V_{th})V_{DS}-V_{DS}^2\} \text{ (Linear region)}$$

$$I_D = 0.5\mu C_{OX}(W/L)\{(V_{GS}-V_{th})^2\} \text{ (Saturation region)}$$

Where V_{GS} is the gate-to-source voltage and I_D is the drain current.

b) Compute dynamic power dissipation. Given $C_L = 0.01 \text{ pF}$ and $T_P = 100 \text{ nS}$.

Spring 2012

Circuits and Systems Problem 2

Find the output resistance of the double-cascode current mirror shown in following figure. Assume all transistors operate in saturation region with $I_D = 10 \mu\text{A}$, $V_A = 50 \text{ V}$ and $g_m r_o = 50$. Neglect body effect.

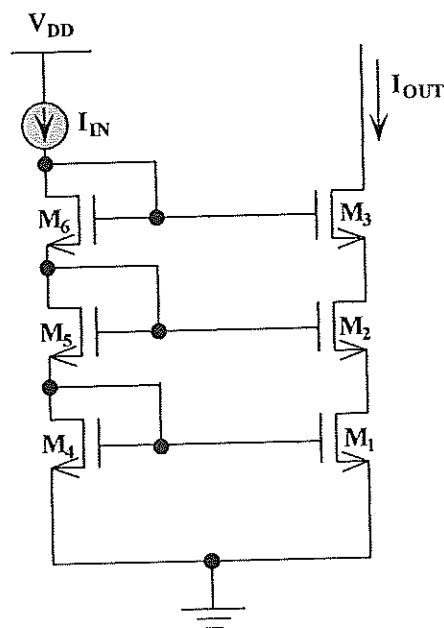


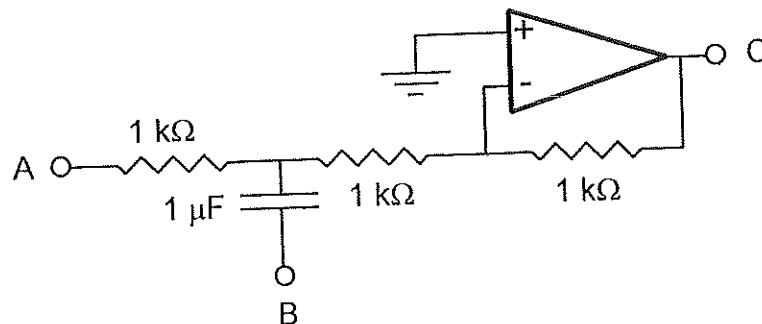
Figure: Double-cascode current mirror.

Spring 2012

Circuits and Systems Problem 3

In the circuit below you may assume the op-amp is ideal. At time $T = 0$ the capacitor is uncharged, and a positive step from 0 to 1 Volt is applied to point A.

- a) Sketch the waveform at point C, if point B is not connected to anything. Indicate the voltage and time scales.
- b) Sketch the waveform at point C, if point B is connected to ground. Indicate the voltage and time scales.
- c) Sketch the waveform at point C, if point B is connected to point C. Indicate the voltage and time scales.

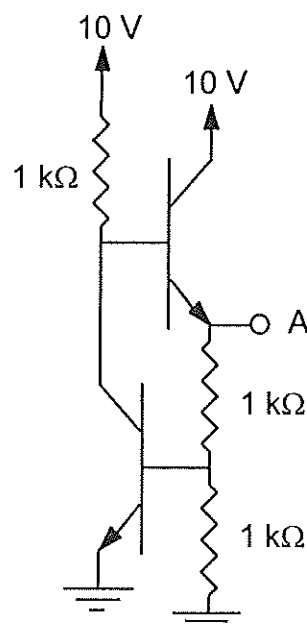


Spring 2012

Circuits and Systems Problem 4

In the circuit below you may assume the transistors have very high current gain, β , and that their base to emitter voltage = 0.7 Volts.

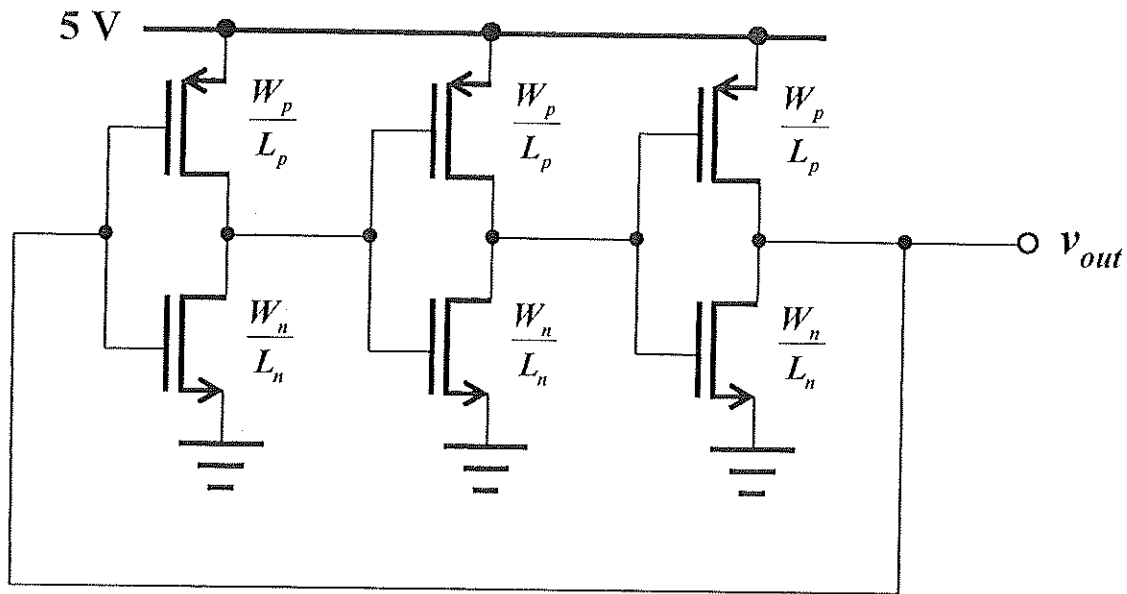
- a) Find the voltage at point A.
- b) Find the current in the right hand transistor.
- c) Find the current in the left hand transistor.
- d) Find the impedance at point A.



Spring 2012

Circuits and Systems Problem 5

For a circuit given below, answer the following questions. In the given circuit, transistors are designed such that t_{PHL} (propagation delay of high-to-low transition) and t_{PLH} (propagation delay of low-to-high transition) of one stage are both 10 ps. All NMOS transistors in the circuit are identical. All PMOS transistors in the circuit are identical as well. Threshold voltages of the NMOS and the PMOS are 1 V and -1 V, respectively. Assume that major contribution to the load capacitance at each stage is from the fanout capacitance (sum of the gate capacitances).



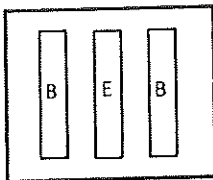
- Draw v_{out} versus time between 0 and 300 ps.
- If all the transistors in the circuit are scaled by a factor of α (greater than 1), i.e. $W_{p_new} = \alpha W_p$, $W_{n_new} = \alpha W_n$, how would the graph in (a) change? State your assumption(s).
- If just the PMOS transistors in the circuit are scaled by a factor of α (greater than 1), i.e. $W_{p_new} = \alpha W_p$, how would the graph in (a) change? State your assumption(s).

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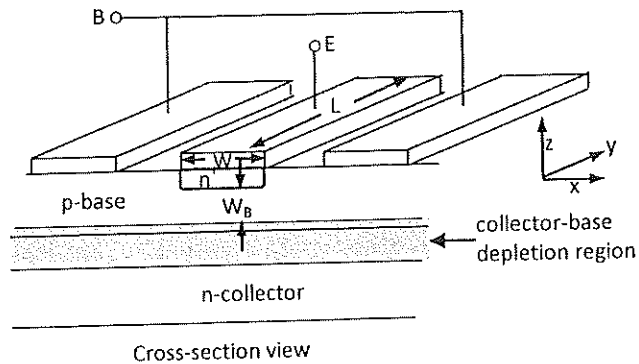
Physical Electronics
Problem 1

A double base stripe-width n-p-n Si bipolar junction transistor (BJT) operating in the active bias mode of operation is shown below. The transistor common-emitter current gain $\beta = 50$. The p-base is uniformly doped with acceptor ion density of 10^{16} cm^{-3} . Diffusion constant $D_n = 30 \text{ cm}^2/\text{s}$ in the base. For Si, intrinsic carrier density $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$ at temperature $T = 300 \text{ K}$. Boltzmann's constant $k = 1.38 \times 10^{-23} \text{ J/K}$. Hole mobility $\mu_p = 420 \text{ cm}^2/\text{V}\cdot\text{s}$ in the base. Emitter junction width $W = 10 \text{ }\mu\text{m}$ and length $L = 20 \text{ }\mu\text{m}$. Quasi-neutral base width $W_b = 0.15 \text{ }\mu\text{m}$.

- What is the average current density J_E (A cm^{-2}) in the device at the emitter-base junction interface if magnitude of total emitter current I_E is 1 mA? You may neglect sidewall injection from the emitter into the base.
- Is the injected emitter current density J_E uniform along the x-direction in the base region? Give physical explanation for your answer.
- Neglecting the effect of base resistance outside the emitter junction area along y-direction, estimate the value of base-emitter junction voltage V_{BE} at which β begins to drop due to high-level injection effect. Explain your answer.
- At the value of V_{BE} found in c) above, $I_E = 6.4 \text{ mA}$. Estimate the ratio of maximum magnitude of J_E to minimum magnitude of J_E at the emitter-base interface along x direction. You must give intermediary details.



Top view showing emitter metal contact (E) and two base contact metal stripes (B). Collector contact is not shown.



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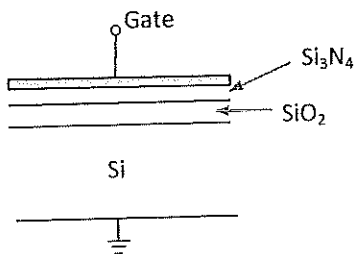
Physical Electronics
Problem 2

Consider a two-terminal MNOS capacitor structure shown below. Silicon substrate is n-type doped with donor density $N_D = 10^{16} \text{ cm}^{-3}$. SiO_2 thickness is 10 nm and Si_3N_4 thickness is 30 nm. Permittivity of free space $\epsilon_0 = 8.854 \times 10^{-14} \text{ F cm}^{-1}$. The relative permittivity of SiO_2 is 3.9, that of Si_3N_4 is 7.5 and that of Si is 11.8. Intrinsic carrier density $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$ at temperature $T = 300 \text{ K}$ in Si. Magnitude of electron charge $q = 1.6 \times 10^{-19} \text{ C}$ and Boltzmann constant $k = 1.38 \times 10^{-23} \text{ J/K}$. the depletion width d in Si under depletion is related to its surface potential ψ_s by $d = (2\epsilon_0\epsilon_s\psi_s/qN_D)^{0.5}$, where ϵ_s is relative permittivity of Si.

a) Under appropriate positive gate bias voltage, the Si-SiO₂ interface is under accumulation. Determine the device capacitance per unit area (F cm^{-2}). Show details.

b) Under appropriate negative gate voltage V_{Th} , the Si-SiO₂ interface is at the on-set of strong inversion. Now if a sheet layer of negative charge density of magnitude $(2q \times 10^{11}) \text{ C cm}^{-2}$ is somehow added at the $\text{Si}_3\text{N}_4 - \text{SiO}_2$ interface, find the difference $(V_{\text{Th}(\text{new})} - V_{\text{Th}})$ in the gate voltage that will be necessary for on-set of strong inversion in this latter case. Show details.

c) How can the observed property in b) above be exploited in practice? Be specific giving details of your application.



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Physical Electronics
Problem 3

A bar of silicon (Si) is 1 μm long and 100 μm^2 in cross sectional area.

a) The bar is doped with a concentration of 10^{17} cm^{-3} of phosphorus (P) such that mobility equals 750 cm^2/Vs . Find the current at 300 K with 10 V applied.

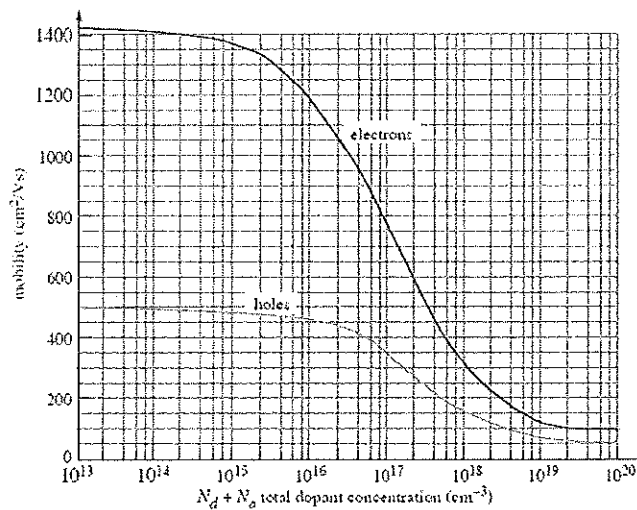
b) Calculate how long it takes for an electron to drift a distance of 1 μm when an electric field of 10^5 V/cm is applied. Assume intrinsic Si.

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Physical Electronics
Problem 4

Given a sample of silicon with n-type doping concentration, $N_D = 10^{17} \text{ cm}^{-3}$. Assume an electric field, E , of magnitude $1 \times 10^3 \text{ V/cm}$ is applied along the sample in the $+x$ direction. Use the figure below, as necessary.

- Calculate the drift velocity for electrons. Indicate both magnitude and sign.
- If an electron drifts a distance of 1 micron along this silicon sample, how long will it take, on average, to drift this distance? (Show your calculation(s).)
- Find the number of collisions that will occur over a distance of 1 micron. (Assume a collision time of $\tau = 0.07$ picoseconds.)

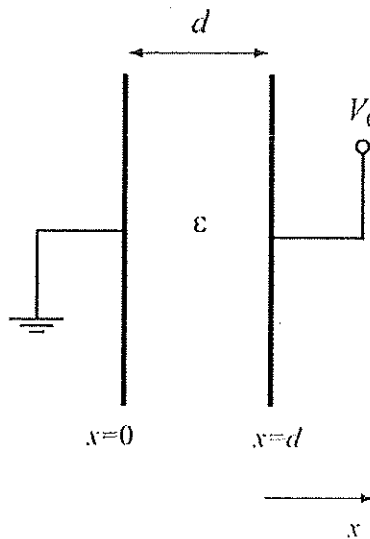


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Physical Electronics
Problem 5

Consider the two conductors shown in the figure below. The left conductor is grounded, while on the right one we apply a voltage V_0 , so that $V(0) = 0$, and $V(d) = V_0$. The dielectric material between the two conductors has permittivity $\epsilon(x) = \epsilon_1 \frac{1}{1 + \frac{x}{d}}$, $0 \leq x \leq d$.

- Show that the potential satisfies the equation $\frac{d}{dx} \left(\epsilon(x) \frac{dV}{dx} \right) = 0$ for $0 \leq x \leq d$.
- Calculate the potential $V(x)$ for $0 \leq x \leq d$.
- Calculate the electric field \mathbf{E} for $0 < x < d$.
- Calculate the per-unit-area capacitance $C = \frac{|\rho_s|}{V_0}$, where ρ_s is the surface charge density.



The following control block diagram is obtained from the linearized synchronous generator's model where $G_{EX}(s) = \frac{K_A}{1+sT_A}$. Using the figure,

- 1- Show generator angle $\Delta\delta$, generator speed $\Delta\omega$, rotor flux $\Delta E'_q$, and field voltage ΔE_{fd} on the figure.
- 2- From the block diagram, write the dynamical (differential) equations for $\frac{d}{dt}\Delta\delta$, $\frac{d}{dt}\Delta\omega$, $\frac{d}{dt}\Delta E'_q$, and $\frac{d}{dt}\Delta E_{fd}$.
- 3- Suppose that a power system stabilizer is added to the block diagram. Show where the new signal (from PSS) is introduced in the block diagram.

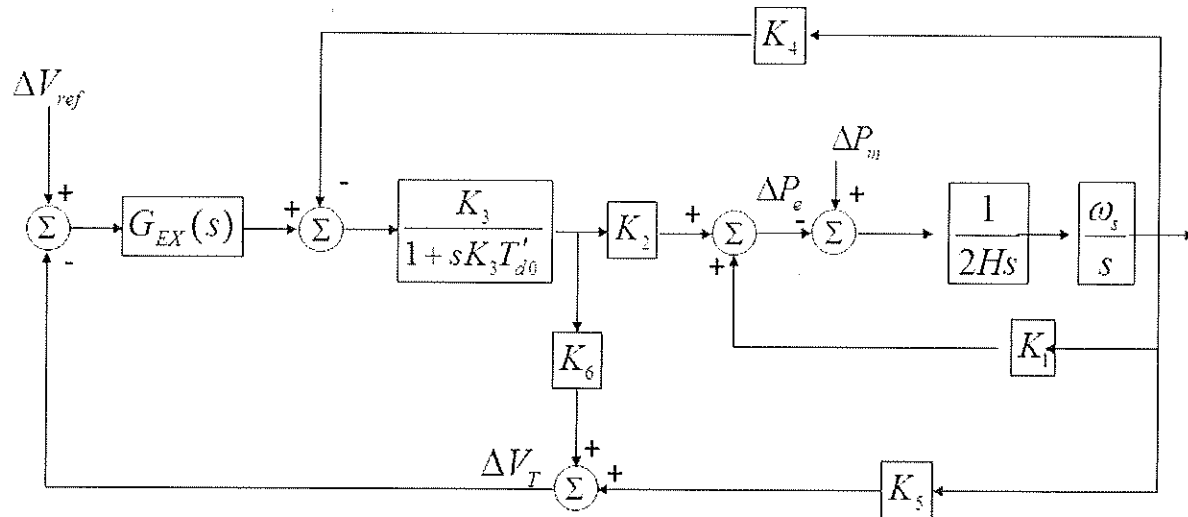


Fig. 1 shows PWM inverter applied as a compensator and Clarke's Vectors of the inverter voltage.

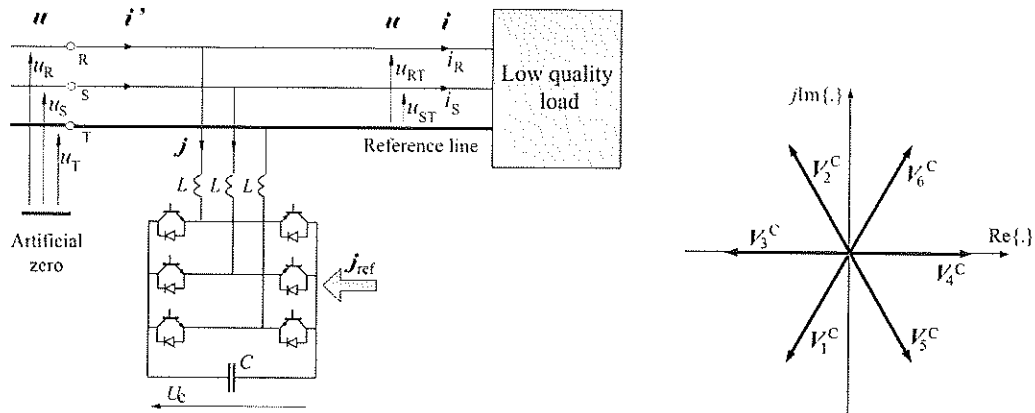


Fig.1 Three-phase system with switching compensator and diagram of Clarke's Vectors of the inverter voltage.

The Clarke's Vector of inverter three-phase voltages is $V^C = 200 e^{j320 \text{ deg}}$ V. The capacitor voltage $U_c = 350$ V. The switching frequency is $f_s = 18$ kHz. Calculate duty factors of inverter switches, assuming that State 7 is used at inverter control.

- 1) Explain the principle of operation of brushless DC motor on the basis of linear motor model
- 2) What are the differences and similarities between synchronous and brushless DC motors
- 3) Explain differences and similarities between DC brush and brushless DC motors
- 4) Draw the equivalent circuit of brushless DC motor in dq system and write the relevant voltage equations and equation for electromagnetic torque.

1. What is the medium in energy conversion process in electric machines? Explain the difference between electric motors and electric generators.
2. What is the input and output power in the motors and in the generators? Can each motor operate as a generator? Explain why.
3. The electromechanical system shown in Fig. 1 is connected to the battery of the voltage $E_s = 12\text{ V}$, and internal resistance $R_s = 0.15\ \Omega$. The coil of resistance $R = 0.05\ \Omega$, consisting of $N = 4$ turns, wound on the iron bar of width $l = 0.2\text{ m}$ moves with speed v with respect to the permanent magnet pole N, which gives the magnetic flux density in the air-gap equal to $B = 1\text{ T}$. The coil is moving with the speed $v = 5\text{ m/s}$. Calculate the value and show in the diagram the actual direction of the following quantities:

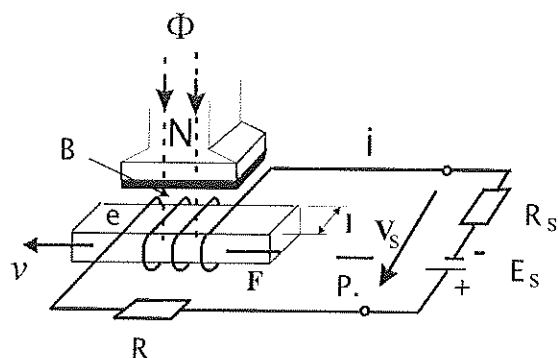
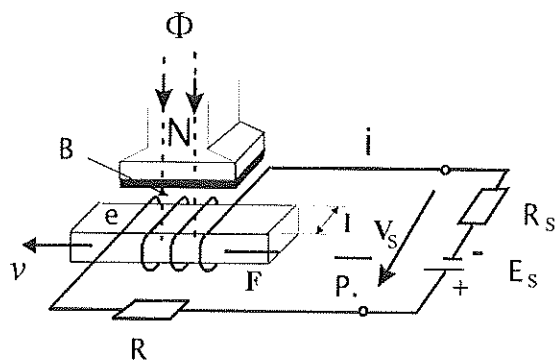


Fig. 1.

- The resultant electromotive force E induced in the coil,
- The current i that flows in the circuit,
- The voltage across the battery terminals,
- The power P drawn by the battery,
- The force F acting on the coil.

4. The electromechanical system shown in Fig. 2 has the same parameters as in point 3 and it is moving with the speed $v = 20\text{ m/s}$. Calculate and show in the diagram the actual direction of the following quantities:



- The resultant electromotive force E induced in the coil,
- The current i that flows in the circuit,
- The voltage across the battery terminals,
- The power P drawn by the battery,
- The force F acting on the coil.

When in both cases shown in Fig. 1 and Fig. 2 does the system operate as a generator, and when does the system operate as the motor?

AUTOMATIC CONTROL 1

SPRING 2012

Sketch root locus for

$$KG(s) = \frac{K(s^2 - 2s + 2)}{s^2(s + 6)}$$

in the cases of

- (i) $0 \leq K < \infty$, and
- (ii) $-\infty < K < 0$.
- (iii) Design a lead/lag compensator together with K for (i) and (ii) to achieve stability of the closed-loop system.

Consider the characteristic polynomial

$$\lambda(s) = s^5 + 2s^4 + 7s^3 + 14s^2 + 16s + 32$$

- (i) Find number of roots on left half plane right half plane and on the imaginary axis.
- (ii) If the above characteristic polynomial has roots on right half plane, can you relocate all the roots on left half plane by changing only one coefficients? Why or why not?

AUTOMATIC CONTROL 3**SPRING 2012**

Consider unity negative feedback control system with loop transfer matrix $P(s)K(s)$ where

$$P(s) = C(sI - A)^{-1}B, \quad K(s) = F(sI - A - BF - LC)^{-1}L$$

1. Show that the closed-loop system is stable, if and only if both $A + BF$ and $A + LC$ are stability matrices (i.e., all eigenvalues lie on open left half plane).
2. Suppose that the command input is at the controller input, i.e., $e(t) = r(t) - y(t) = r(t) - Cx(t)$ with $r(t)$ the command input, and $y(t)$ and $x(t)$ the output and state vector of $P(s)$, respectively. Find the closed-loop transfer matrix from $r(t)$ to $y(t)$.
3. Suppose that the command input is at the plant input, i.e., input to $P(s)$ is: $u(t) = r(t) - F\hat{x}(t)$ with $r(t)$ the command input, and $\hat{x}(t)$ the state vector of $K(s)$. Find the closed-loop transfer matrix from $r(t)$ to $y(t)$.

Let $G_1 = \frac{1}{s + \alpha}$ and $G_2(s) = C(sI - A)^{-1}B$ be a minimal realization of a 2 by 2 transfer matrix.

1. Find a state space realization of $G(s) = G_1(s)G_2(s)$.
2. Find conditions in terms of α , A , B and C so that the state space realization obtained above is controllable and observable.

Consider a unity negative feedback system with loop transfer function

$$L(s) = \frac{K(as + 1)}{s^2(s + 1)}.$$

- (a) Sketch its Nyquist plot for the case $a > 1$ and $a \leq 1$, respectively, and determine the stability of the feedback system.
- (b) Let $a = 2$ and $K = 10$. Find the gain margin and the phase margin of the system.
- (c) Suppose $a = 0$ and $K = 10$. Design a PD controller so that the phase margin is at least 45° .

Assume $X(t)$ is a wide sense stationary (WSS) random process with autocorrelation function $R_X(\tau)$ and the power spectral density $S_X(f)$.

1. Let $g(\alpha) = A(1 - |\alpha|)$ for $\alpha \in [-1, 1]$, and $g(\alpha) = 0$, otherwise. Find the auto-correlation function $R_X(\tau)$ corresponding to the power spectral density $S_X(f) = g(f/W)$.
2. Let $R_X(\tau) = A$ for $\tau \in [-T, T]$ and $R_X(\tau) = 0$ for $\tau \notin [-T, T]$. Is $R_X(\tau)$ a valid auto-correlation function? Justify your answer.
3. Now assume $X(t)$ is a Gaussian WSS random process, which passes through a nonlinear device with its output given by $Y(t) = X^2(t)$. Is $Y(t)$ a WSS process? Justify your answer.
4. How to transform a non-Gaussian distributed random vector $[X_1, X_2]$ to a random vector $[Y_1, Y_2]$ where Y_1 and Y_2 are marginally Gaussian distributed? Upon your transformation, will Y_1 and Y_2 be jointly Gaussian distributed? Justify your answer.

X_n is a zero-mean wide-sense stationary random sequence with autocorrelation function $R_X[k] = E[X_n X_{n+k}]$. The random sequence Y_n is obtained from X_n by

$$Y_n = (-1)^n X_n + X_{n-1}.$$

1. Find the autocorrelation function of Y_n .
2. Find the cross-correlation function of X_n and Y_n .
3. Is Y_n wide sense stationary?
4. Are X_n and Y_n jointly wide sense stationary?

A causal linear and time-invariant (LTI) system has the frequency response

$$H(j\omega) = \frac{2 + j\omega}{3 + 4j\omega - \omega^2},$$

where $j = \sqrt{-1}$.

1. Determine a differential equation relating the input $x(t)$ and output $y(t)$ of the above LTI system.
2. Find the output $y(t)$ of the above LTI system when the input is

$$x(t) = te^{-t}u(t),$$

where $u(t)$ is the unit-step signal defined as 1 for $t > 0$ and 0 otherwise.

3. Let $X(j\omega)$ and $Y(j\omega)$ be the Fourier transforms of the signals $x(t)$ and $y(t)$. Find a signal $z(t)$ in terms of $x(t)$ and $y(t)$ such that its Fourier transform is given by

$$Z(j\omega) = X(-2j(\omega - 1)) + j\omega Y(j\omega).$$

A linear-time-invariant system is characterized by its discrete-time Fourier transform (DTFT), given by

$$H(e^{j\omega}) = \frac{\prod_{i=1}^M (e^{j\omega} - \eta_i e^{j\phi_i})}{\prod_{i=1}^N (e^{j\omega} - \rho_i e^{j\psi_i})},$$

where $j = \sqrt{-1}$, $M \leq N$, and no pole-zero cancelation is possible. Assume that η_i , ϕ_i , ρ_i , ψ_i are real numbers, and $\eta_i \geq 0$, $\rho_i \geq 0$, for all i . The input signal sequence is denoted by $x[n]$, $-\infty < n < \infty$, and the output signal sequence is denoted by $y[n]$, $-\infty < n < \infty$.

1. Determine the transfer function (z -transform) $H(z)$ of this system in terms of η_i 's, ρ_i 's, ϕ_i 's, and ψ_i 's.
2. Determine the region of convergence (ROC) of $H(z)$ so that $H(e^{j\omega})$ exists.
3. Given a particular set of η_i 's, ρ_i 's, ϕ_i 's, and ψ_i 's, is the ROC in (2) unique? Justify your answer.
4. Assume that this system is causal. What should be the corresponding appropriate condition on ρ_i , $i = 1, 2, \dots, N$?

Suppose the binary signal set $\mathcal{S} = \{0, u(t)\}$, where $u(t)$ has duration $[0, T]$, is used to transmit one of two equally likely messages over a channel and the received signal is given by

$$r(t) = \alpha s(t) + N_w(t) \quad 0 \leq t \leq T$$

where $s(t) \in \mathcal{S}$ and where $N_w(t)$ is a zero-mean white Gaussian noise process with power spectral density of $S_{N_w}(f) = N_0/2$. The energy in the signal $u(t)$ is E .

1. Assume that the channel gain $\alpha = 1$. Find the probability of error for the optimal receiver.
2. Now assume that the channel gain α is a random variable with probability distribution given below.

$$P(\alpha = 1) = .2 \quad \text{and} \quad P(\alpha = 2) = .8$$

- (a) Find the average probability of error for the optimal receiver that does not know the value of α and assumes $P(\alpha = 1) = 1$.
- (b) Find the average probability of error for the optimal receiver that does not know the value of α but knows the distribution of α .
- (c) Determine the average probability of error for the optimal receiver that knows the value of α .