A HALF-DAY WORKSHOP
ON
SPICE/COMPACT MOS MODELING
(European SPICE Compact Modeling)

Organizer and Coordinator: Prof. Ashok Srivastava, Electrical & Computer Engineering Department

Sponsors: Electrical & Computer Engineering Department and College of Engineering, Louisiana State University, Baton Rouge

Date: Friday 9 December 2011
Time: 9.15 AM - Noon
Place: EE117 Conference Room

Welcome and Opening Remarks: Prof. Pratul K. Ajmera, Interim Chairman, Electrical & Computer Engineering Department, and **Address** by Prof. Richard Koubek, Dean College of Engineering
Address by Prof. Renuka P. Jindal, Electrical & Computer Engineering Department, University of Louisiana at Lafayette, and President IEEE Electron Devices Society (EDS)
Speaker and Moderator: Dr. Wladyslaw (Wladek) Grabinski, Consultant & Research Scientist, NanoLab, École polytechnique fédérale de Lausanne (EPFL), Lausanne, Switzerland
RSVP to ashok@ece.lsu.edu by 5 December 2011 for participation in workshop.

SUMMARY

The workshop will present the work being done in the area of compact MOS modeling for integrated circuit design integrating powerful modeling and CAD tools under the Compact Modeling Network (COMON). [1] - a consortium of 15 European universities and companies, which came together in an attempt to transfer the scientific and technological knowledge from academia to industry, to strengthen local, European integrated circuit (IC) design capabilities with powerful modeling and CAD methodologies, and to achieve integration of European research in fragmented R&D areas for the benefit of both young and experienced researchers.

The global structure of the project is divided into Working Groups (WGs), each one addressing one specific type of devices: Multiple-gate MOSFETs (WG1), High Voltage MOSFETs (WG2) and advanced III-V HEMTs (WG3). The COMON Work Packages (WPs) focuses on SPICE level modeling and standardization tasks. A compact modeling development and parameter extraction work package (WP1) addresses the modeling and

characterization techniques developed by COMON partners for modeling of target semiconductor devices including such effects as the thermal effects, RF, noise and microwave behavior and process fluctuations. A compact modeling, implementation and benchmarking work package (WP2) is related to the advanced compact models for implementation in open source/GNU and commercial circuit simulators. The model implementation is carried out at higher levels of abstraction using standard VHDL-AMS and Verilog-A description. In the work package WP3, entitled "Evaluation and Demonstration of the Models and Design Tools on Dedicated Test Chips", a comprehensive evaluation of the compact models by simulating a number of analog, digital, RF circuits for the different available semiconductor technologies are considered. Test chips will be fabricated by the industrial COMON partners. A dissemination, training, exploitation and IPR management work package (WP4) addresses the dissemination of COMON modeling results which is to be performed through scientific publications in international journals, presentations at conferences, and maintenance of COMON web site. A series of the workshops on compact modeling (MOS-AK/GSA) [2] are organized twice a year. Training courses and summer schools are planned as well. Finally, within the project management work package (WP5) the network coordination and administration tasks are done.

[1] COMON Compact Moodeling Network FP7 Marie-Curie project web page:
http://www.compactmodelling.net/
[2] MOS-AK/GSA Group Compact Modeling Groupweb page
Corresponding author e-mail: wladek@mos-ak.org

Speaker's Biopgraphy: Dr. Wladek Grabinski received his Ph.D. degree from the Institute of Electron Technology, Warsaw, Poland, in 1991. From 1991 to 1998 he was a Research Assistant at the Integrated Systems Lab, ETH Zürich, Switzerland, supporting the CMOS and BiCMOS technology developments by electrical characterization of the processes and devices. From 1999 to 2000, he was with LEG, EPF Lausanne, and was engaged in the compact MOSFET model developments supporting numerical device simulation and parameter extraction. Later, he was a technical staff engineer at Motorola, and subsequently at Freescale Semiconductor, Geneva Modeling Center, Switzerland. He is now a consultant responsible for modeling, characterization and parameter extraction of MOS transistors for the design of RF CMOS circuits. He is currently consulting on the development of next-generation compact models for the 65–32-nm-technology very large scale integration (VLSI) circuit simulation. His current research interests are in high-frequency characterization, compact modeling and its Verilog-A standardization as well as device numerical simulations of MOSFETs for analog/RF low power applications. He is an editor of the reference modeling book Transistor Level Modeling for Analog/RF IC Design and also authored or coauthored more than 50 papers. Dr. Grabinski has served as a member in IEEE EDS Compact Modeling Committee, Organization Committee of ESSDERC/ESSDERC, TPC of SBMicro, SISPAD, MIXDES Conferences; reviewer of the IEEE TED, IJNM, MEJ. He also serves as European representative for the ITRS Modeling and Simulation working group. He also supports the EPFL IEEE Student Branch acting as its Interim Branch Counselor. Dr. Grabinski is involved in activities of the MOS-AK/GSA compact modeling group and serves as a coordinating manager since 1999. <http://people.epfl.ch/wladyslaw.grabinski>