Modeling of Graphene Nanoribbon Tunnel Field Effect Transistor in Verilog-A for Digital Circuit Design

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Abstract— **Performance of graphene nanoribbon (GNR) tunnel field effect transistor (TFET) has been modeled in Verilog-Analog (Verilog-A) using previously reported physics based compact analytical current transport model. Performance obtained using both analytical model and Verilog-A simulations are compared providing excellent match. Using n-type and p- type GNR TFETs, inverter circuit is designed and simulated in Mentor Graphics® Tanner EDA S-Edit and T-Spice utilizing the developed Verilog-A codes. With suitable choice of supply voltage, our Verilog-A simulated GNR TFET inverter provides low propagation delay, low power dissipation and retains strong signal integrity.**

Keywords- Graphene nanoribbon, GNR tunnel FET, GNR tunnel FET inverter, Verilog-A based simulation

I. INTRODUCTION

Field effect transistors based on planar band-to-band tunneling have attracted great interest over the last decade due to its potential to operate at sub-60 mV/decade subthreshold swing at very low voltage [1]. Compared to conventional bulk three dimensional material systems (Si, Ge, GaAs, InAs), atomically thin two dimensional materials have also been studied for the design of such emerging tunnel field-effect transistors (TFETs) [2]. Graphene nanoribbon, the quantum confined one dimensional form of graphene, is one of the extensively studied materials for TFETs. Numerical simulations and analytical models have shown the promise of GNR TFET for low power circuit design [3-6]. Moreover, modeling of graphene and non-graphene based vertical heterostructure transistors have also attracted interest, recently [7-9]. However, in order to study the GNR TFET's circuit level applicability, SPICE compatible model is required. Since majority of the commercially available SPICE simulators depend on library models such as BSIM or EKV3, GNR TFETs cannot be simulated with these conventional SPICE simulators. In this regard, high level hardware description language such as Verilog-A provides an efficient and accurate way of simulating emerging devices which do not have SPICE level models.

Verilog-A is simple and straightforward way which facilitates the encoding of mathematical expressions describing the device physics of the emerging devices like TFETs [10]. Since research in modeling of TFETs is still in progress, Verilog-A is the tool which can be used very effectively for studying the circuit level performance of TFETs prior to synthesis of large scale integration.

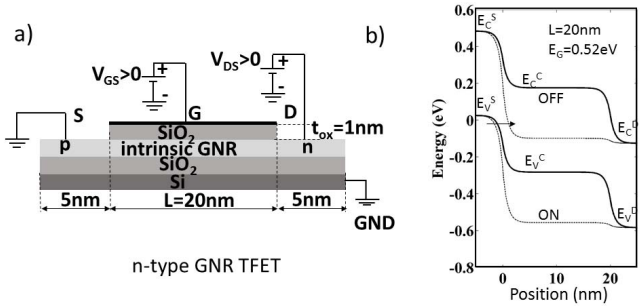

Fig. 1. a) Schematic of the cross-sectional view of an n- type GNR TFET and b) energy band diagram in off- and on- states.

Numerous approaches have been undertaken to study the circuit level performance of GNR TFETs for both digital and analog circuit design.

Universal analytic model of InGaSb/InAs TFET from Lu et al., [11] have been studied using Verilog-A, however, the simulation considers a look-up table based approach which does not meet the criteria of standard electronic design automation (EDA). Yang et al., [3] reported a GNR TFET circuit design which depends largely on the quantum transport based device simulation and look-up table based Verilog-A approach. Compared to look-up table based simulations, physics based analytical current transport models are also required to be validated by numerical quantum transport simulation prior to their Verilog-A implementation.

In this work, we have modeled GNR TFET in Verilog-A written in Mentor Graphics® Tanner EDA S-Edit and compiled in T-Spice based on our physics based compact analytical current transport model of GNR TFET reported earlier [12]. The model in [12] was compared and validated with numerical quantum transport simulation considering non-equilibrium Green's function (NEGF) formalism for which the SPICE level simulation of our GNR TFET circuit is accurate. Details of the compact model and the comparison with NEGF simulations can be found in [12] and is not repeated here. Both n- and p- type GNR TFETs are modeled in Verilog-A first and compared with their analytic models. For brevity, we have only shown the n- type GNR TFET characteristics. Furthermore, GNR TFET inverter circuit is developed where the transient analysis is carried out. Finally, different figure of merits of GNR TFET inverter

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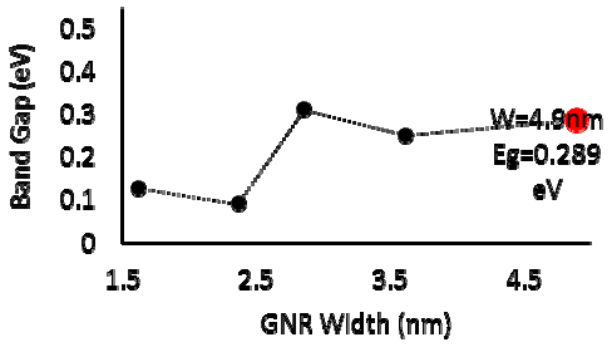

Fig. 2. The relationship between the width of GNR and band gap.

are calculated at different supply voltages and operating frequencies.

II. GNR TFET Device Structure and Operation

Schematic of an n- type GNR TFET and it's operation is shown in Fig. 1(a) and (b), respectively. The channel length is 20nm with source and drain extension of 5nm on each sides. The top gate oxide is 1nm of SiO_2. The energy band diagram shown in Fig. 1(b) depicts the off- and on- state conditions of the GNR TFET. The solid line is for the off-state whereas the dash line is for the on- state. In off- state, the intrinsic channel restricts any source-channel tunneling since both the Fermi levels remain in equilibrium. As the positive bias is applied (for n- type GNR TFET) in on- state, the channel conduction band comes opposite to the source valence band and source-channel band-to-band tunneling occurs. Note that the GNR energy band gap varies with the width. Based on the calculation made in [12] using NanoTCAD ViDES [13], the energy band gap corresponding to varying GNR widths are plotted in Fig. 2 for demonstration. Our model and simulation in Verilog-A

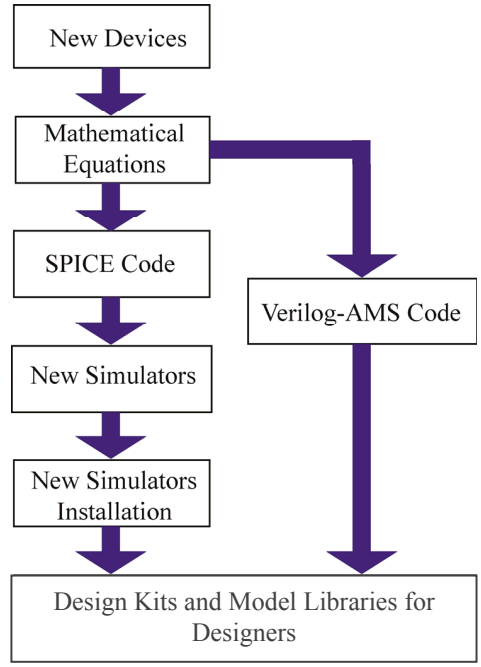

Fig. 3. Flow chart of simulating emerging new devices using compact analytical current transport models in Verilog-A code instead of SPICE based new simulators [14].

considers GNR width of 4.9nm providing an energy band gap of 0.289eV. This has been shown by the larger marker in Fig. 2.

Since conventional CMOS SPICE simulators are unable to provide simulation of GNR TFETs and require additional compact models, Verilog-A provides advantage in this

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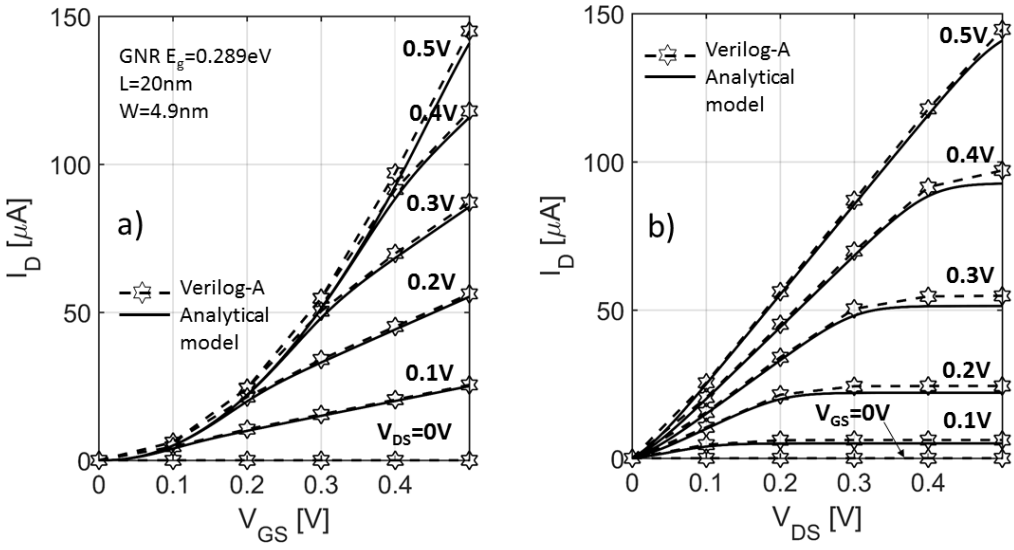

Fig. 4. Comparison of GNR TFET characteristics obtained from Verilog-A simulations with the analytical current transport model reported in [12]. a) I_D-V_{GS} transfer characteristics for different V_{DS} and b) I_D-V_{DS} output characteristics for different V_{GS}.

[12] is written in Verilog-A and compiled in T-Spice. A flow diagram showing different steps to simulate such new devices in Verilog-A is shown in Fig. 3 following the work of Srivastava et al., [14]. For comparison, the transfer characteristics and output characteristics obtained through our Verilog-A simulation are plotted along with the same obtained from analytical model for n- type GNR TFET which are shown in Fig. 4(a) and 4(b), respectively. For the GNR TFET of 20nm channel length, 4.9nm width and 0.289eV band gap, both the transfer and output characteristics obtaned from Verilog-A simulations match closely with the analytical model of [12]. Note, that both the generic GNR TFET simulation for low power digital circuit design reported by Yang et al., [3] and analog model reported by Barboni et al., [4] consider look-up table based approach. Compared to both [3] and [4], our Verilog-A simulated GNR TFET can directly capture the transistor device physics controlling the circuit level performance and thus become more suitable for EDA based design.

Considering the Verilog-A model of both p- and n- type GNR TFETs, complementary GNR TFET inverter is simulated in Mentor Graphics® Tanner EDA T-Spice. The schematic of the GNR TFET inverter is shown in Fig. 5(a). The corresponding input, output and delay waveforms are extracted directly from Mentor Graphics® Tanner EDA W-Edit which are shown in Fig. 5(b), 5(c) and 5(d), respectively. For an input signal of 0.4GHz with 1ps rise and fall times, the delay of the GNR TFET inverter is ~ 60ps. Compared to earlier reported GNR TFET inverter delay of 14ns of Yang et al., [3] for similar GNR width and supply voltage, our GNR TFET inverter shows much small delay.

III. Performance Evaluation of GNR TFET Inverter

Single layer infinite graphene sheet does not possess any band gap. However, observable band gaps are found in the nanoribbon form of graphene and can be used in digital VLSI design. This has already been shown in Fig. 2. The maximum and minimum band gaps are obtained for 2.86nm width and of 2.37nm width, respectively. Considering current IC fabrication, we safely choose 4.9nm width for all of our GNR TFET simulations. It has been observed that the delay and power dissipation change with the change in dielectric oxide material and its corresponding thickness. In order to obtain superior gate control over the channel, we have considered 1nm HfO_2 as the gate dielectric and performed simulations of GNR TFET inverter based on model reported in our work [12].

The inverter schematic shown in Fig. 5(a) is similar to CMOS technology which has been extensively studied for extraction of different figure of merits of the GNR TFET inverter. We have considered supply voltage, operating frequency and load capacitance variations on the performance of GNR TFET inverter as shown in Fig. 6. Figure 6(a) shows the variation of power dissipation with the supply voltage. Under 1.8V operation, the power dissipation is 47.16µW and is 2.09µW for 0.1V. The trend

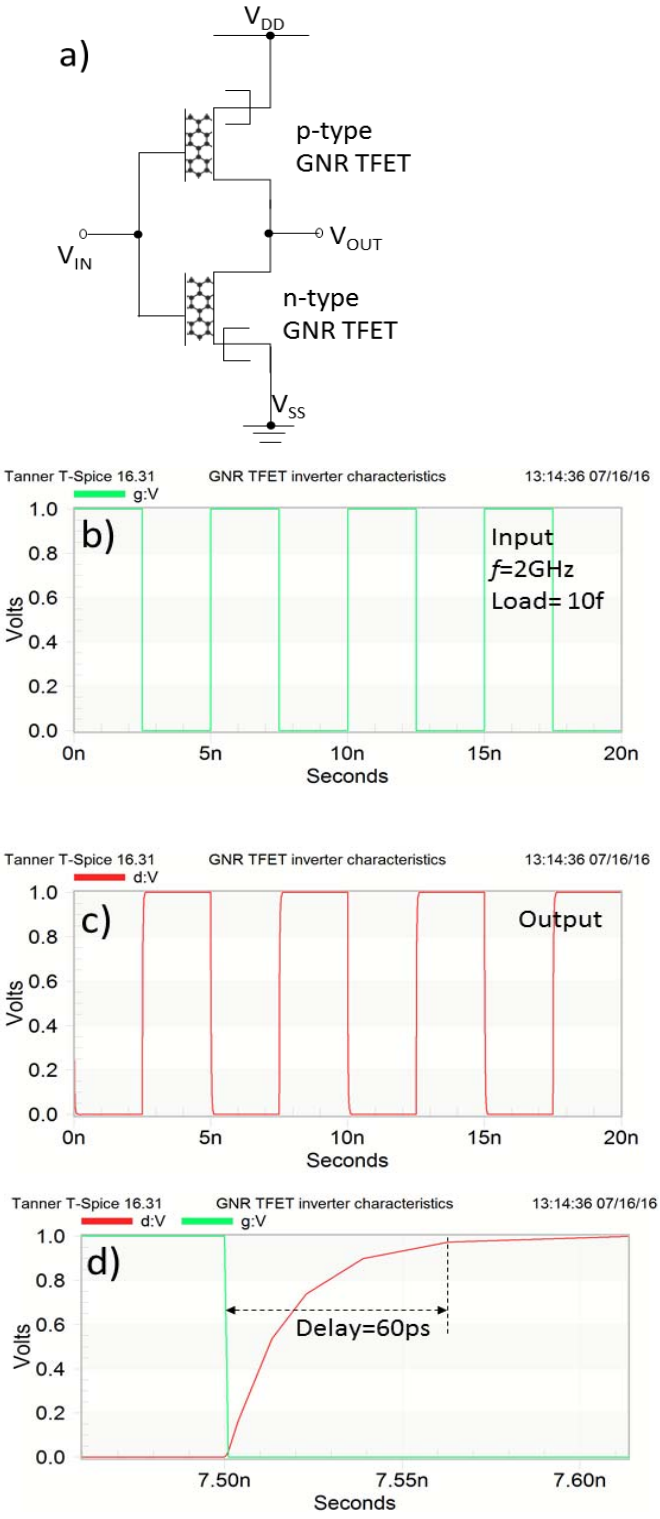

Fig. 5. a) Schematic of GNR TFET inverter considering both p- and n- type GNR TFETs, b) input square-wave signal at 0.4GHz, c) obtained output from GNR TFET inverter at 10fF load capacitance and d) inverter delay calculation.

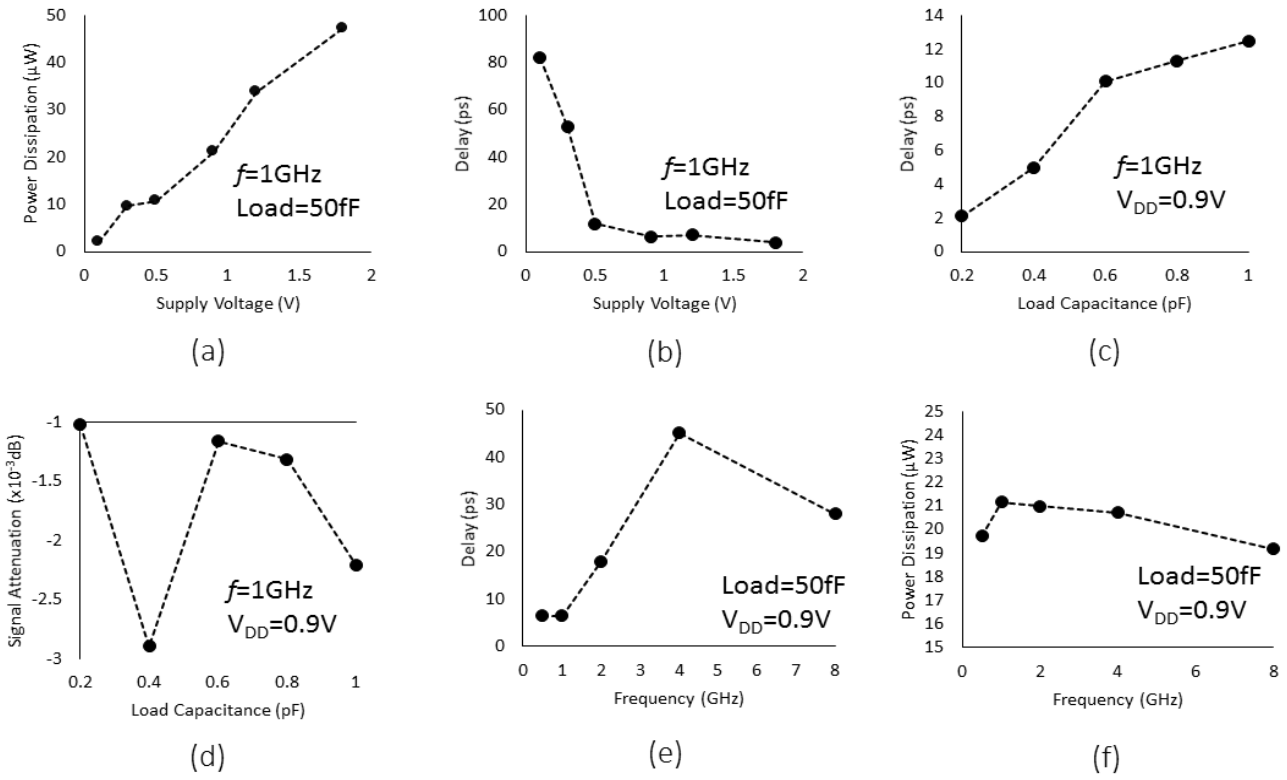

Fig. 6. a) Relationship between supply voltage and power dissipation for GNR TFET inverter for load capacitance of 50fF and test frequency of 1GHz, b) relationship between supply voltage and delay at load capacitance of 50fF and the test frequency at 1GHz, c) relationship between load capacitance and GNR TFET inverter delay for the supply voltage is 0.9V and 1GHz test frequency, d) relationship between the load capacitance and signal attenuation for GNR TFET inverter simulated at supply voltage 0.9V and 1GHz test frequency, e) relationship between operating frequency and GNR TFET inverter delay for load capacitance of 50fF and the supply voltage of 0.9V and f) relationship between frequency and power dissipation for 50fF load capacitance and 0.9V supply voltage.

is approximately linear. In Fig. 6(b), the delay is estimated for change in supply voltage. For low supply voltages, we have observed the maximum delay. This shows that how the supply voltage influences the transmission delay of an inverter. It can be seen that above 0.5V, the delay is smaller than 10ps. Even in extremely scaled supply voltage of 0.1V, the delay is still less than 100ps. The estimated power dissipation at 1.8V supply voltage is 47.16μW, however, the smallest delay as low as 1ps has been observed in this case. Therefore, a trade-off between delay and power dissipation is required while choosing the supply voltages in GNR TFET inverter. Figure 6(c) shows the trend of delay with increasing load capacitance. In worst case, in which load capacitance is 1pF, the delay is only 12.5ps. Signal integrity is also an important performance parameter in digital design. The signal integrity is measured at the central point of real high output logic period which is denoted as V_{high_real}. If the perfect logic high is denoted as $V_{high\_perfect}$ then the signal attenuation can be expressed as follows:

$$Attenuation = 20log\frac{V_{high\_real}}{V_{high\_perfect}} \quad (1)$$

Figure 6(d) shows the simulation of signal attenuation. It can be seen that the worst case happens when the load capacitance is 0.4pF. Note that the the entire signal integrity is within an acceptable range. For the GNR TFET inverter, it is important to study the effect of frequency with both delay and power dissipation. Figure 6(e) shows the trend of inverter delay with the frequency. The largest delay is 45ps when the frequency is 4GHz. Up to 8GHz, the delay is only around 28ps which is also within an acceptable range.

The power dissipation in VLSI circuits is very sensitive to frequency and imperfect charging and discharging happen under high speed transmission. Our model is based on the phenomena of band-to-band tunneling and nearly independent of charge traps or impurities. Thus our proposed GNR TFET is suitable for extremely high speed digital application. Figure 6(f) shows the relationship between frequency and power dissipation. It shows that the power dissipation of our transistor is not very sensitive to frequency. Moreover, the important figure of merit of GNR TFET inverter, power-delay product (PDP) has been plotted in Fig. 7 as well showing very low energy consumption. Hence, our study proves that the modeled GNR TFET has

TABLE I. PERFORMANCE COMPARISON OF FINFET AND GNR TFET

Parameter	FinFET	GNR-TFET
Channel length (nm)	20	20
Supply voltage (V)	0.9	0.9
Delay (ps)	13	2.1
Power-delay product (aJ)	673	126

extremely fast data transmission, acceptable power dissipation and signal integrity. Hence it becomes a good candidate for future digital circuit design. In order to keep our study specific to basic unit cell of logic circuits, we have studied the performance of a single GNR TFET inverter instead of multi-stage ring oscillator. Nevertheless, the model developed in this work can be extended for the design of multistage ring oscillator or other logic gates. Moreover, performance of our simulated GNR TFET inverter has been compared with FinFET using the predictive technology model developed by Nanohub [15] and are enumerated in Table I. From Table I, for equal channel length and supply voltage, competitive performance of GNR TFET is estimated making it suitable for next generation energy efficient logic technology development beyond the Moore's law.

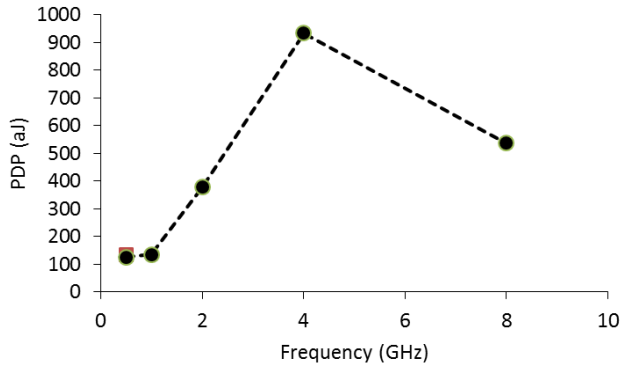

Fig. 7. Power delay product of GNR TFET inverter computed at V_{DD}=0.9V and a load capacitance of 50fF.

IV. CONCLUSION

GNR TFET based digital circuit design has been modeled and simulated in high level hardware description language Verilog-A for the first time. Compared to conventionally reported look-up table based simulation approach of emerging nanoscale devices, direct compact model based Verilog-A simulations become suitable for EDA platforms. The performance obtained from our GNR TFET inverter shows promising for low power energy efficient ultra-fast digital circuit design.

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REFERENCES

[1] A. M. Ionescu and H. Riel H., "Tunnel field-effect transistors as energy-efficient electronic switches," Nature, vol. 479, pp. 329-337, Dec 2011.

[2] D. Jena, "Tunneling transistors based on graphene and 2-D crystals," Proceedings of the IEEE, vol. 101, pp. 1585-1602, 2013.

[3] X. Yang, J. Chauhan, J. Guo, and K. Mohanram, "Graphene tunneling FET and its applications in low-power circuit design," in 20th Great Lakes Symposium on VLSI, Providence, Rhode Island, USA, 2010.

[4] L. Barboni, M. Siniscalchi, and B. Sensale-Rodriguez, "TFET-based circuit design using the transconductance generation efficiency g_m/I_d method," IEEE Journal of the Electron Devices Society, vol. 3, pp. 208-216, 2015.

[5] M. S. Fahad, A. Srivastava, A. K. Sharma and C. Mayberry. (2013). Current transport in graphene tunnel field effect transistor for RF integrated circuits. *2013 IEEE Int. Wireless Symp. (IWS)* Beijing. pp. 1-4.

[6] A. Srivastava, Y.M. Banadaki, Md. S. Fahad, "Dielectrics for graphene transistors for emerging integrated circuits," *ECS Trasactions*, vol. 61, no. 2, pp. 351-361, 2014.

[7] M. Fahad and A. Srivastava, "A graphene switching transistor for vertical circuit design," *ECS J. of Solid State Sci. and Tech.,* vol. 5, pp. M13-M21, 2016.

[8] A. Srivastava and M. S. Fahad, "Vertical MoS2/hBN/MoS2 interlayer tunneling field effect transistor," *Solid-State Elect.* (in press).

[9] M. Fahad, A. Srivastava, A. K. Sharma, C. Mayberry and K.M. Mohsin, **"**Silicene nanoribbon tunnel field effect transistor," *ECS Transactions,* vol. 75, no. 5, pp. 175-181, 2016.

[10] M. A. Chalkiadaki, C. Valla, F. Poullet, and M. Bucher, "Why- and how- to integrate Verilog-A compact models in SPICE simulators, "International Journal of Circuit Theory and Applications," vol. 41, pp. 1203-1211, 2013.

[11] H. Lu, D. Esseni, and A. Seabaugh, "Universal analytic model for tunnel FET circuit simulation," Solid-State Electronics, vol. 108, pp. 110-117, Jun 2015.

[12] M. S. Fahad, A. Srivastava, A. K. Sharma, and C. Mayberry, "Analytical current transport modeling of graphene nanoribbon tunnel field-effect transistors for digital circuit design," IEEE Transactions on Nanotechnology, vol. 15, pp. 39-50, Jan 2016.

[13] G. Fiori and G. Iannaccone, (2013). *NanoTCAD ViDES* [Online].Available: http://vides.nanotcad.com/vides/

[14] A. Srivastava, Y. Xu, and R. Soundararajan, "Energy recovery techniques for CNT-FET circuits," in International Symposium on Electronic System Design (ISED), India, pp. 81-84, 2010.

[15] A. Ravchowdhury, C. Augustine, Y. Gao, M. Lundstrom, K. Roy, "PETE: purdue emerging technology evaluator," https://nanohub.org/resources/pete, 2016.