Fall 2011 Final Exam Review

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This Summary

When / Where

Monday, 5 December 2011, 15:00-17:00 (3:00 PM to 5:00 PM) CST

213 Tureaud (Here)

Conditions

Closed Book, Closed Notes, No Electronics

No use of communication devices, even for accessing Facebook `:-)`.

Format

Lots of short-answer questions.

Resources

Solved test and homework:. `http://www.ece.lsu.edu/koppel/ee2720/prev.html`

Brown and Vranesic (the textbook).

Dr. Skavantos' handouts.

Study Recommendations

Study this semester's homework assignments. Similar problems may appear on the exam.

Solve Old Problems—memorizing solutions **is not the same** as solving.

Following and understanding solutions **is not the same as** solving.

Use the solutions for brief hints and to check your own solutions.

Topics

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Summary of Topics

Number Representations

Boolean Algebra

Logic Gates

Min- and maxterm canonical forms, etc. (*B&V Section 2.6*)

The exclusive-or gate.

Karnaugh maps and all that that implicates. (*B&V Sections 4.1-4.5*)

Multiplexors, decoders, encoders, priority encoders. (*B&V Sections 6.1-6.3*)

Programmable logic devices: PLAs, PALs, FPGAs.

Binary full adder and ripple adder.

EDA/CAD Definitions.

Structural Verilog Modules.

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Number Representation Skills

B&V Sections 5.1, 5.3, 5.3.1, 5.3.2. (Note: 5.2 will also be on test, that comes later in this study guide.)

Know the following representations:

Unsigned binary, octal, hexadecimal, BCD.

Two's complement binary signed.

Sized representations. (*E.g.*, 12-bit binary.)

Gray Code.

Binary Arithmetic

Add and subtract binary unsigned numbers by hand.

How to detect overflow for unsigned and 2's complement.

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Not on Final Exam

Radices other than 2, 8, 10, 16.

ASCII, excess 3, 2 out of 5.

Diminished radix complement (such as 1's complement), signed magnitude.

Multiplication.

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Boolean Algebra and Logic Skills

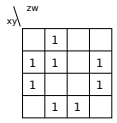
B&V Sections 2.1, 2.2, 2.3, 2.4, 2.4.1, 2.5, 2.5.2, 2.5.3, 2.6, 2.6.1

Convert between any of the following representations of a Boolean function:

A Boolean algebraic expression. $a'(b+c)+e$.

A truth table.

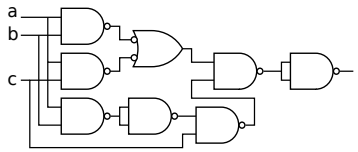
A Karnaugh map:



An expression using this minterm shorthand: $\sum_{x,y,z} m(1,3,7)$.

An expression using this minterm shorthand: $\prod_{a,b,c} M(0,6)$.

A logic diagram:



Determine a Boolean function from a problem description.

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Boolean Algebra and Logic Skills Continued

B&V Sections 2.1, 2.2, 2.3, 2.4, 2.4.1, 2.5, 2.5.2, 2.5.3, 2.6, 2.6.1

Boolean Algebra

Multiply out and factor algebraic expressions.

Know basic simplifications:

Cover: $a + ab = a$

$a\overline{a} = 0, \quad a + \overline{a} = 1.$

DeMorgan's Theorem: $\overline{ab} = \overline{a} + \overline{b}$

DeMorgan's Theorem: $\overline{a + b} = \overline{a}\,\overline{b}$

Not on Final Exam: No need to memorize other theorems.

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Karnaugh Map Skills

B&V Sections 4.1, 4.2, 4.3

Simplify Boolean expressions using a Karnaugh map.

Know how to draw a Karnaugh map.

Know how to find prime implicants on a Karnaugh map.

Know how to find minimum-cost expressions from a map.

Know how to use don't-cares (incompletely specified outputs).

Not On Final Exam:

Multi-output circuits, finding a minimum cover.

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Combinational Circuit Building Blocks (Muxen and friends.)

B&V Sections 6.1, 6.1.1, 6.2, 6.3, 6.3.1, 6.3.2.

Know what multiplexers, decoders, encoders, and priority encoders do.

Know how they are implemented using basic logic gates.

Know how to implement logic functions using these devices.

Know how to make larger devices of these types from smaller ones.

Not On Final Exam:

Demultiplexors, Shannon Expansion.

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Programmable Logic Devices

B&V Sections 3.6, 3.6.1, 3.6.2, 3.6.4, 3.6.5

Simple Devices: PLAs, PALs

Draw a diagram of such a device (like Figure 3.27 of text).

Use it to implement a Boolean function.

Figure out the Boolean function from a diagram.

Complex Devices: CPLDs, FPGAs.

Understand that these consist of multiple simpler devices that can be arbitrarily interconnected.

Understand that FPGAs contain a mixture of lookup tables (LUTs) and specialized logic blocks such as adders.

There will **not be** questions about programming an FPGA or CPLD for a specific function.

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HDL Definitions

B&V Section 2.9

Know Definitions of These Terms

Electronic Design Automation (EDA):
Using computers to design (in this case) digital circuits.

Computer Aided Design (CAD):
An older term for EDA.

Hardware Description Language (HDL):
A language for describing a (usually) digital circuit.

Verilog:
One of two popular HDLs.

VHDL:
One of two popular HDLs.

Design Flow:
The steps used in designing a digital circuit. The first step is entering a design in an HDL,

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the last step is a run of the synthesis program. In between many different programs can be used to evaluate and refine the design.

Functional Simulation:

Determining the outputs of a design described by an HDL (that is, simulating it) using very simple timing rules. The goal is to verify that it works correctly.

Synthesis:

The running of synthesis programs on an HDL description in order to generate files for use in manufacturing a chip (such as an ASIC) or programming a chip (such as an FPGA).

Technology Kit:

A set of files provided by a manufacturer which are read by a synthesis program.

Timing Simulation:

Determining the outputs of a design described by an HDL (that is, simulating it) using accurate timing data. (The timing data is typically determined in the synthesis step.) The goal is to verify that the design is fast enough (and correct, given accurate timing).

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Verilog Skills

B&V Sections 2.10, 2.10.1

Write a structural description of a simple circuit.

Draw a schematic of a structural description of a simple circuit.

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Binary Full Adder

B&V Section 5.2, 5.2.1, 5.2.2

Binary full adder.

Ripple adder.