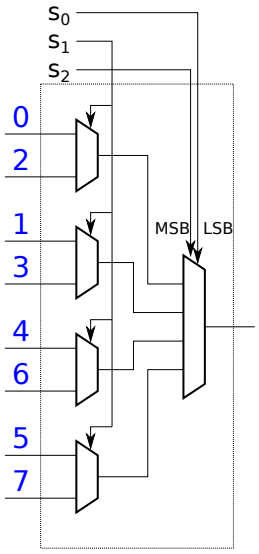
LSU EE 2720-2 Homework 5 Solution Due: 28 November 2011

Please read textbook sections 2.9 and 2.10 (Verilog introduction) in time for Monday's class.

Problem 1: In the 8-input multiplexer below, constructed from smaller multiplexers, the select inputs, s_0, s_1, and s_2, were connected in what would normally be considered the wrong order. That is, if the mux inputs were numbered consecutively starting from the top from 0 to 7 then a select input of 2 would not route the third input to the output.

Number the inputs based on the select bits as connected so that if the select bits represent i then input i (using your numbering) is routed to the output. (**Do not** change the select bit ordering, even though they are wrong.) *Hint: Set the select bits to 3 ($s_2 = 0, s_1 = 1, s_0 = 1$), then figure out which input is routed to the output. Label that input 3. Repeat for the other 7 possible select inputs.*



Solution appears above in blue (the added input labels). As explained in the hint, simply consider each possible select input, from 0 to 7, and see which of the multiplexer inputs is routed to the output. Notice that the numbering can be obtained by swapping the least significant and middle bit of the natural input number. For example, consider the second input, with natural number 1 or 001_2. Swapping bit position 0 (the least significant) with bit position 1 (the middle bit) yields 010_2 or 2, which is the number. This swapping of bit positions corresponds to the swapping of the select input bits (s_1 and s_0 were swapped).

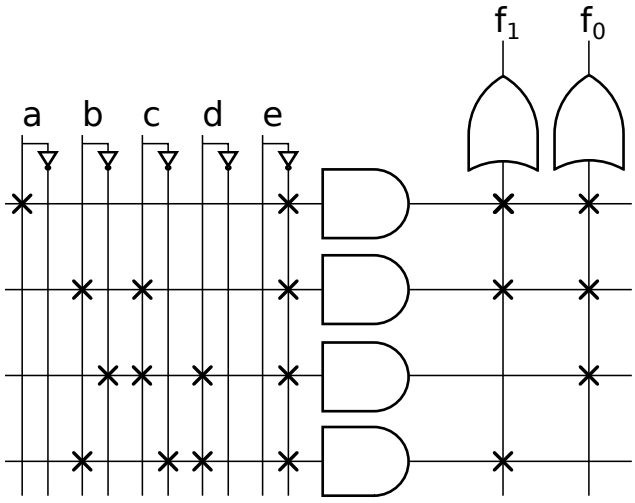
Problem 2: Consider the pair of logic functions:

$$f_0 = \left(a + bc + \overline{b}cd\right)\overline{e}$$

$$f_1 = \left(a + bc + b\overline{c}d\right)\overline{e}$$

(a) Show how these can be implemented using a PLA(without external logic). Indicate: The number of inputs (n), the number of product terms (AND gates, p), and the number of outputs, m. Draw a diagram of the PLA, using the abbreviated form in which a single wire connects to the AND- and OR-gates' inputs.

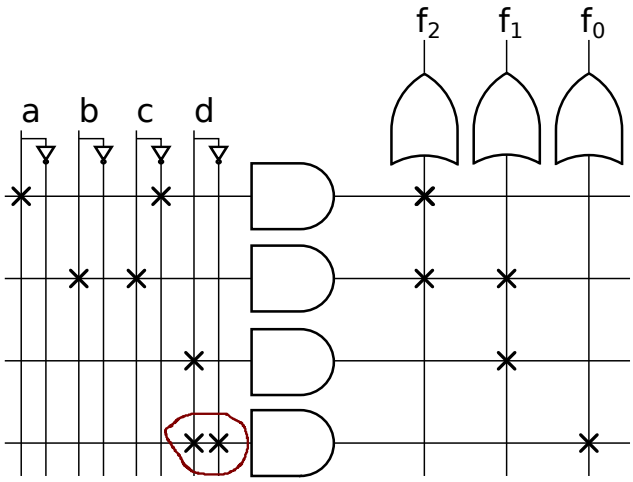
These function require a PLA with $n = 5$ inputs (for a, b, c, d, and e); with $p = 4$ product terms (noting that f_0 and f_1, which each have three product terms, share two of them), and with $m = 2$ outputs. The diagram appears below.



(b) Explain why a PAL would be less suitable than a PLA for the pair of functions above.

Because f_0 and f_1 share two product terms. With a PLA the same product term can be used for multiple outputs, that's because the connections between the AND gates and OR gates can be programmed (shown with the bold $\times$). In a PAL each AND gate connects to just one OR gate (those connections are not programmable) and so product terms cannot be shared. If a PAL were used to implement this function six rather than four AND gates would be needed.

Problem 3: The diagram below is for a PLA.



(*a*) One of the outputs appears to be a mistake. Which one, and why?

Output f_0, because it is set to $d\overline{d}$ which is always false, that's shown in red in the diagram above. It is unlikely that someone would use a PLA just to generate a fixed logic 0 signal, there are less costly ways to do that.

(*b*) Write a Boolean expression for each output.

The expressions are:

$$f_0 = d\,\overline{d}$$
$$f_1 = b\,c + d$$
$$f_2 = a\overline{c} + b\,c$$

(*c*) Draw a logic diagram showing only the gates that are needed.

Solution appears below. Notice that the third AND gate has been replaced by wire but that the fourth AND gate, useless though it may be, has been kept. (The fourth AND gate could be replaced by a fixed logic 0 signal.)