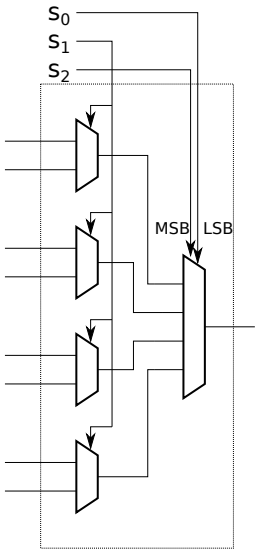
LSU EE 2720-2 **Homework 5** **Due: 28 November 2011**

Please read textbook sections 2.9 and 2.10 (Verilog introduction) in time for Monday's class.

Problem 1: In the 8-input multiplexer below, constructed from smaller multiplexers, the select inputs, s_0, s_1, and s_2, were connected in what would normally be considered the wrong order. That is, if the mux inputs were numbered consecutively starting from the top from 0 to 7 then a select input of 2 would not route the third input to the output.

Number the inputs based on the select bits as connected so that if the select bits represent i then input i (using your numbering) is routed to the output. (**Do not** change the select bit ordering, even though they are wrong.) *Hint: Set the select bits to 3 ($s_2 = 0, s_1 = 1, s_0 = 1$), then figure out which input is routed to the output. Label that input 3. Repeat for the other 7 possible select inputs.*



Problem 2: Consider the pair of logic functions:

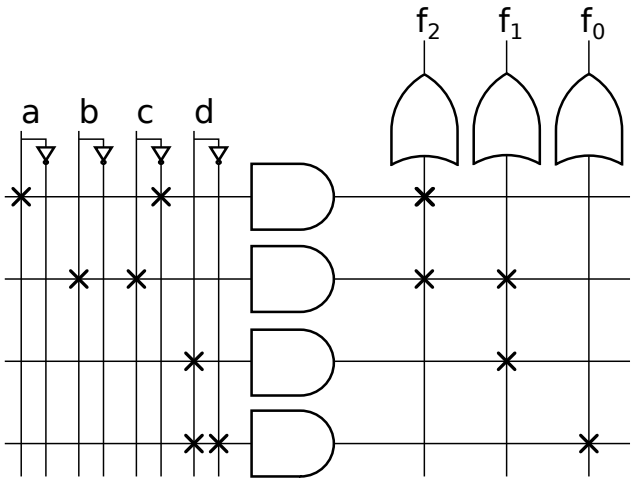
$$f_0 = \left(a + bc + \overline{b}cd\right)\overline{e}$$

$$f_1 = \left(a + bc + b\overline{c}d\right)\overline{e}$$

(a) Show how these can be implemented using a PLA(without external logic). Indicate: The number of inputs (n), the number of product terms (AND gates, p), and the number of outputs, m. Draw a diagram of the PLA, using the abbreviated form in which a single wire connects to the AND- and OR-gates' inputs.

(b) Explain why a PAL would be less suitable than a PLA for the pair of functions above.

Problem 3: The diagram below is for a PLA.



(*a*) One of the outputs appears to be a mistake. Which one, and why?

(*b*) Write a Boolean expression for each output.

(*c*) Draw a logic diagram showing only the gates that are needed.