EE 2720-2: Digital Logic I

Syllabus

Where/When/Web/QR

Room 213 Tureaud Hall
Monday Wednesday 14:40–15:30 **Fall 2011**
`http://www.ece.lsu.edu/koppel/ee2720/`

Who

David M. Koppelman
Room 349 Electrical Engineering Building
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Office Hours: MW 9:30–10:30, TTF 14:00–15:00.

Catalog Description

Digital Logic I (2). Prereq: MATH 1550. Boolean algebra; logic gates; minimization methods; analysis and synthesis of combinational logic networks; design examples.

Text

"Fundamentals of Digital Logic with Verilog Design," second edition, Stephen Brown and Zvonko Vranesic, McGraw-Hill, 2008.

Grading

25% Each of Two Midterm Exams • 30% Final Exam • 20% Homework

Late-homework not accepted. Missed-midterm-exam policy: If student provides a doctor's statement indicating illness on the date of the test then the weight of the other midterm will be increased to 35% and the final to 45%. Daily attendance: optional, however students are responsible for all material, instructions, and notices presented in class.