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Part I: Intel® Itanium® Instruction Set Descriptions
The Intel® Itanium® architecture is a unique combination of innovative features such as explicit parallelism, predication, speculation and more. The architecture is designed to be highly scalable to fill the ever increasing performance requirements of various server and workstation market segments. The Itanium architecture features a revolutionary 64-bit instruction set architecture (ISA), which applies a new processor architecture technology called EPIC, or Explicitly Parallel Instruction Computing. A key feature of the Itanium architecture is IA-32 instruction set compatibility.

The Intel® Itanium® Architecture Software Developer's Manual provides a comprehensive description of the programming environment, resources, and instruction set visible to both the application and system programmer. In addition, it also describes how programmers can take advantage of the features of the Itanium architecture to help them optimize code.

1.1 Overview of Volume 1: Application Architecture

This volume defines the Itanium application architecture, including application level resources, programming environment, and the IA-32 application interface. This volume also describes optimization techniques used to generate high performance software.

1.1.1 Part 1: Application Architecture Guide


Chapter 2, “Introduction to the Intel® Itanium® Architecture” provides an overview of the architecture.

Chapter 3, “Execution Environment” describes the Itanium register set used by applications and the memory organization models.

Chapter 4, “Application Programming Model” gives an overview of the behavior of Itanium application instructions (grouped into related functions).

Chapter 5, “Floating-point Programming Model” describes the Itanium floating-point architecture (including integer multiply).

Chapter 6, “IA-32 Application Execution Model in an Intel® Itanium® System Environment” describes the operation of IA-32 instructions within the Itanium System Environment from the perspective of an application programmer.
1.1.2 Part 2: Optimization Guide for the Intel® Itanium® Architecture

Chapter 1, “About the Optimization Guide” gives an overview of the optimization guide.

Chapter 2, “Introduction to Programming for the Intel® Itanium® Architecture” provides an overview of the application programming environment for the Itanium architecture.

Chapter 3, “Memory Reference” discusses features and optimizations related to control and data speculation.

Chapter 4, “Predication, Control Flow, and Instruction Stream” describes optimization features related to predication, control flow, and branch hints.

Chapter 5, “Software Pipelining and Loop Support” provides a detailed discussion on optimizing loops through use of software pipelining.

Chapter 6, “Floating-point Applications” discusses current performance limitations in floating-point applications and features that address these limitations.

1.2 Overview of Volume 2: System Architecture

This volume defines the Itanium system architecture, including system level resources and programming state, interrupt model, and processor firmware interface. This volume also provides a useful system programmer’s guide for writing high performance system software.

1.2.1 Part 1: System Architecture Guide


Chapter 2, “Intel® Itanium® System Environment” introduces the environment designed to support execution of Itanium-based operating systems running IA-32 or Itanium-based applications.

Chapter 3, “System State and Programming Model” describes the Itanium architectural state which is visible only to an operating system.

Chapter 4, “Addressing and Protection” defines the resources available to the operating system for virtual to physical address translation, virtual aliasing, physical addressing, and memory ordering.

Chapter 5, “Interruptions” describes all interruptions that can be generated by a processor based on the Itanium architecture.

Chapter 6, “Register Stack Engine” describes the architectural mechanism which automatically saves and restores the stacked subset (GR32 – GR 127) of the general register file.

Chapter 7, “Debugging and Performance Monitoring” is an overview of the performance monitoring and debugging resources that are available in the Itanium architecture.

Chapter 8, “Interruption Vector Descriptions” lists all interruption vectors.
Chapter 9, “IA-32 Interruption Vector Descriptions” lists IA-32 exceptions, interrupts and intercepts that can occur during IA-32 instruction set execution in the Itanium System Environment.

Chapter 10, “Itanium®-based Operating System Interaction Model with IA-32 Applications” defines the operation of IA-32 instructions within the Itanium System Environment from the perspective of an Itanium-based operating system.

Chapter 11, “Processor Abstraction Layer” describes the firmware layer which abstracts processor implementation-dependent features.

1.2.2 Part 2: System Programmer’s Guide

Chapter 1, “About the System Programmer’s Guide” gives an introduction to the second section of the system architecture guide.

Chapter 2, “MP Coherence and Synchronization” describes multi-processing synchronization primitives and the Itanium memory ordering model.

Chapter 3, “Interruptions and Serialization” describes how the processor serializes execution around interruptions and what state is preserved and made available to low-level system code when interruptions are taken.

Chapter 4, “Context Management” describes how operating systems need to preserve Itanium register contents and state. This chapter also describes system architecture mechanisms that allow an operating system to reduce the number of registers that need to be spilled/filled on interruptions, system calls, and context switches.

Chapter 5, “Memory Management” introduces various memory management strategies.

Chapter 6, “Runtime Support for Control and Data Speculation” describes the operating system support that is required for control and data speculation.

Chapter 7, “Instruction Emulation and Other Fault Handlers” describes a variety of instruction emulation handlers that Itanium-based operating systems are expected to support.

Chapter 8, “Floating-point System Software” discusses how processors based on the Itanium architecture handle floating-point numeric exceptions and how the software stack provides complete IEEE-754 compliance.

Chapter 9, “IA-32 Application Support” describes the support an Itanium-based operating system needs to provide to host IA-32 applications.

Chapter 10, “External Interrupt Architecture” describes the external interrupt architecture with a focus on how external asynchronous interrupt handling can be controlled by software.

Chapter 11, “I/O Architecture” describes the I/O architecture with a focus on platform issues and support for the existing IA-32 I/O port space.

Chapter 12, “Performance Monitoring Support” describes the performance monitor architecture with a focus on what kind of support is needed from Itanium-based operating systems.

Chapter 13, “Firmware Overview” introduces the firmware model, and how various firmware layers (PAL, SAL, EFI) work together to enable processor and system initialization, and operating system boot.
1.3 Overview of Volume 3: Instruction Set Reference

This volume is a comprehensive reference to the Itanium and IA-32 instruction sets, including instruction format/encoding.

1.3.1 Part 1: Intel® Itanium® Instruction Set Descriptions


Chapter 2, “Instruction Reference” provides a detailed description of all Itanium instructions, organized in alphabetical order by assembly language mnemonic.

Chapter 3, “Pseudo-Code Functions” provides a table of pseudo-code functions which are used to define the behavior of the Itanium instructions.

Chapter 4, “Instruction Formats” describes the encoding and instruction format instructions.

Chapter 5, “Resource and Dependency Semantics” summarizes the dependency rules that are applicable when generating code for processors based on the Itanium architecture.

1.3.2 Part 2: IA-32 Instruction Set Descriptions

Chapter 1, “Base IA-32 Instruction Reference” provides a detailed description of all base IA-32 instructions, organized in alphabetical order by assembly language mnemonic.

Chapter 2, “IA-32 Intel® MMX™ Technology Instruction Reference” provides a detailed description of all IA-32 Intel® MMX™ technology instructions designed to increase performance of multimedia intensive applications. Organized in alphabetical order by assembly language mnemonic.

Chapter 3, “IA-32 Streaming SIMD Extension Instruction Reference” provides a detailed description of all IA-32 Streaming SIMD Extension instructions designed to increase performance of multimedia intensive applications, and is organized in alphabetical order by assembly language mnemonic.

1.2.3 Appendices

Appendix A, “Code Examples” provides OS boot flow sample code.
1.4 Terminology

The following definitions are for terms related to the Itanium architecture and will be used throughout this document:

**Instruction Set Architecture (ISA)** – Defines application and system level resources. These resources include instructions and registers.

**Itanium Architecture** – The new ISA with 64-bit instruction capabilities, new performance-enhancing features, and support for the IA-32 instruction set.

**IA-32 Architecture** – The 32-bit and 16-bit Intel® architecture as described in the *IA-32 Intel® Architecture Software Developer’s Manual*.

**Itanium System Environment** – The operating system environment that supports the execution of both IA-32 and Itanium-based code.

**IA-32 System Environment** – The operating system privileged environment and resources as defined by the *IA-32 Intel® Architecture Software Developer’s Manual*. Resources include virtual paging, control registers, debugging, performance monitoring, machine checks, and the set of privileged instructions.

**Itanium-Based Firmware** – The Processor Abstraction Layer (PAL) and System Abstraction Layer (SAL).

**Processor Abstraction Layer (PAL)** – The firmware layer which abstracts processor features that are implementation dependent.

**System Abstraction Layer (SAL)** – The firmware layer which abstracts system features that are implementation dependent.

1.5 Related Documents

The following documents can be downloaded at the Intel’s Developer Site at http://developer.intel.com:

- **Intel® Itanium® 2 Processor Reference Manual for Software Development and Optimization** – This document describes model-specific architectural features incorporated into the Intel® Itanium® 2 processor, the second processor based on the Itanium architecture. (Document Number 251110)
- **Intel® Itanium® Processor Reference Manual for Software Development** – This document describes model-specific architectural features incorporated into the Intel® Itanium® processor, the first processor based on the Itanium architecture. (Document Number 245320)
- **IA-32 Intel® Architecture Software Developer’s Manual** – This set of manuals describes the Intel 32-bit architecture. (Document Numbers 245470, 245471, and 245472)
- **Itanium™ Software Conventions and Runtime Architecture Guide** – This document defines general information necessary to compile, link, and execute a program on an Itanium-based operating system. (Document Number 245358)
- **Itanium® Processor Family System Abstraction Layer Specification** – This document specifies requirements to develop platform firmware for Itanium-based systems. (Document Number 245359)
- **Extensible Firmware Interface Specification** – This document defines a new model for the interface between operating systems and platform firmware.
## 1.6 Revision History

<table>
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<th>Description</th>
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<td>Description</td>
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<tr>
<td>December 2001</td>
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<td>Faults in ld.c that hits ALAT clarification (Section 4.4.5.3.1).</td>
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<td>Class pr-writers-int clarification (Table A-5).</td>
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<td>IA-32 IBR/DBR match clarification (Section 7.1.1).</td>
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<td>ISR figure changes (pp. 8-5, 8-26, 8-33 and 8-36).</td>
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<td>PAL_CACHE_FLUSH return argument change - added new status return argument (Section 11.8.3).</td>
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<td>PAL self-test Control and PAL_A procedure requirement change - added new arguments, figures, requirements (Section 11.2).</td>
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<td>PAL_CACHE_FLUSH clarifications (Section 11).</td>
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<td>Non-speculative reference clarification (Section 4.4.6).</td>
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<td>RID and Preferred Page Size usage clarification (Section 4.1).</td>
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<td>VHPT read atomicity clarification (Section 4.1).</td>
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<td>IIP and WC flush clarification (Section 4.4.5).</td>
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<td>PAL_PROC_GET/SET_FEATURES changes - extend calls to allow implementation-specific feature control (Section 11.8.3).</td>
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<td>Split PAL_A architecture changes (Section 11.1.6).</td>
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<td>PAL memory accesses and restrictions clarification (Section 11.9).</td>
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<td>PSP validity on INITs from PAL_MC_ERROR_INFO clarification (Section 11.8.3).</td>
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<td>Speculation attributes clarification (Section 4.4.6).</td>
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<td></td>
<td></td>
<td>PAL_A FIT entry, PAL_VM_TR_READ, PSP, PAL_VERSION clarifications (Sections 11.8.3 and 11.3.2.1).</td>
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<td>TLB searching clarifications (Section 4.1).</td>
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<td>IA-32 related changes (Section 10.3, Section 10.3.2, Section 10.3.2, Section 10.3.3.1, Section 10.10.1).</td>
</tr>
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<td>IPSR.ri and ISR.ei changes (Table 3-2, Section 3.3.5.1, Section 3.3.5.2, Section 5.5, Section 8.3, and Section 2.2).</td>
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<td>IA-32 CPUID clarification (p. 5-71).</td>
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<td>RCPPS, RCPPSS, RSQRTPS, and RSQRTSS clarification (Section 7.12).</td>
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<td>IA-32 related changes (Section 5.3).</td>
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| July 2000        | 1.1             | Volume 1:
Processor Serial Number feature removed (Chapter 3).
Clarification on exceptions to instruction dependency (Section 3.4.3).
Volume 2:
Clarifications regarding “reserved” fields in ITIR (Chapter 3).
Instruction and Data translation must be enabled for executing IA-32 instructions (Chapters 3, 4 and 10).
FCR/FDR mappings, and clarification to the value of PSR.ri after an RFI (Chapters 3 and 4).
Clarification regarding ordering data dependency.
Out-of-order IPI delivery is now allowed (Chapters 4 and 5).
Content of EFLAGS field changed in IIM (p. 9-24).
PAL_CHECK and PAL_INIT calls – exit state changes (Chapter 11).
PAL_CHECK processor state parameter changes (Chapter 11).
PAL_BUS_GET/SETFEATURES calls – added two new bits (Chapter 11).
PAL_MC_ERROR_INFO call – Changes made to enhance and simplify the call to provide more information regarding machine check (Chapter 11).
PAL_ENTER_IA_32_Env call changes – entry parameter represents the entry order; SAL needs to initialize all the IA-32 registers properly before making this call (Chapter 11).
PAL_CACHE_FLUSH – added a new cache_type argument (Chapter 11).
PAL_SHUTDOWN – removed from list of PAL calls (Chapter 11).
Clarified memory ordering changes (Chapter 13).
Clarification in dependence violation table (Appendix A).|
| January 2000     | 1.0             | Initial release of document. |
This chapter describes the function of each Itanium instruction. The pages of this chapter are sorted alphabetically by assembly language mnemonic.

## 2.1 Instruction Page Conventions

The instruction pages are divided into multiple sections as listed in Table 2-1. The first three sections are present on all instruction pages. The last three sections are present only when necessary. Table 2-2 lists the font conventions which are used by the instruction pages.

### Table 2-1. Instruction Page Description

<table>
<thead>
<tr>
<th>Section Name</th>
<th>Contents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Format</td>
<td>Assembly language syntax, instruction type and encoding format</td>
</tr>
<tr>
<td>Description</td>
<td>Instruction function in English</td>
</tr>
<tr>
<td>Operation</td>
<td>Instruction function in C code</td>
</tr>
<tr>
<td>FP Exceptions</td>
<td>IEEE floating-point traps</td>
</tr>
<tr>
<td>Interruptions</td>
<td>Prioritized list of interruptions that may be caused by the instruction</td>
</tr>
<tr>
<td>Serialization</td>
<td>Serializing behavior or serialization requirements</td>
</tr>
</tbody>
</table>

### Table 2-2. Instruction Page Font Conventions

<table>
<thead>
<tr>
<th>Font</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>regular</td>
<td>(Format section) Required characters in an assembly language mnemonic</td>
</tr>
<tr>
<td>italic</td>
<td>(Format section) Assembly language field name that must be filled with one of a range of legal values listed in the Description section</td>
</tr>
<tr>
<td>code</td>
<td>(Operation section) C code specifying instruction behavior</td>
</tr>
<tr>
<td>code_italic</td>
<td>(Operation section) Assembly language field name corresponding to a italic field listed in the Format section</td>
</tr>
</tbody>
</table>

In the Format section, register addresses are specified using the assembly mnemonic field names given in the third column of Table 2-3. For instructions that are predicated, the Description section assumes that the qualifying predicate is true (except for instructions that modify architectural state when their qualifying predicate is false). The test of the qualifying predicate is included in the Operation section (when applicable).

In the Operation section, registers are addressed using the notation \texttt{reg[addr]}.\texttt{field}. The register file being accessed is specified by \texttt{reg}, and has a value chosen from the second column of Table 2-3. The \texttt{addr} field specifies a register address as an assembly language field name or a register mnemonic. For the general, floating-point, and predicate register files which undergo register renaming, \texttt{addr} is the register address prior to renaming and the renaming is not shown. The \texttt{field} option specifies a named bit field within the register. If \texttt{field} is absent, then all fields of the register are accessed. The only exception is when referencing the data field of the general registers (64-bits not including the NaT bit) where the notation \texttt{GR[addr]} is used. The syntactical differences between the code found in the Operation section and ANSI C is listed in Table 2-4.
The Operation section contains code that specifies only the execution semantics of each instruction and does not include any behavior relating to instruction fetch (e.g., interrupts and faults caused during fetch). The Interruptions section does not list any faults that may be caused by instruction fetch or by mandatory RSE loads. The code to raise certain pervasive faults and actions is not included in the code in the Operation section. These faults and actions are listed in Table 2-5. The Single step trap applies to all instructions and is not listed in the Interruptions section.

### Table 2-3. Register File Notation

<table>
<thead>
<tr>
<th>Register File</th>
<th>C Notation</th>
<th>Assembly Mnemonic</th>
<th>Indirect Access</th>
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</thead>
<tbody>
<tr>
<td>Application registers</td>
<td>AR</td>
<td>ar</td>
<td></td>
</tr>
<tr>
<td>Branch registers</td>
<td>BR</td>
<td>b</td>
<td></td>
</tr>
<tr>
<td>Control registers</td>
<td>CR</td>
<td>cr</td>
<td></td>
</tr>
<tr>
<td>CPU identification registers</td>
<td>CPUID</td>
<td>cpuid</td>
<td>Y</td>
</tr>
<tr>
<td>Data breakpoint registers</td>
<td>DBR</td>
<td>dbr</td>
<td>Y</td>
</tr>
<tr>
<td>Instruction breakpoint registers</td>
<td>IBR</td>
<td>ibr</td>
<td>Y</td>
</tr>
<tr>
<td>Data TLB translation cache</td>
<td>DTC</td>
<td>n/a</td>
<td></td>
</tr>
<tr>
<td>Data TLB translation registers</td>
<td>DTR</td>
<td>dtr</td>
<td>Y</td>
</tr>
<tr>
<td>Floating-point registers</td>
<td>FR</td>
<td>f</td>
<td></td>
</tr>
<tr>
<td>General registers</td>
<td>GR</td>
<td>r</td>
<td></td>
</tr>
<tr>
<td>Instruction TLB translation cache</td>
<td>ITC</td>
<td>n/a</td>
<td></td>
</tr>
<tr>
<td>Instruction TLB translation registers</td>
<td>ITR</td>
<td>itr</td>
<td>Y</td>
</tr>
<tr>
<td>Protection key registers</td>
<td>PKR</td>
<td>pkr</td>
<td>Y</td>
</tr>
<tr>
<td>Performance monitor configuration registers</td>
<td>PMC</td>
<td>pmc</td>
<td>Y</td>
</tr>
<tr>
<td>Performance monitor data registers</td>
<td>PMD</td>
<td>pmd</td>
<td>Y</td>
</tr>
<tr>
<td>Predicate registers</td>
<td>PR</td>
<td>p</td>
<td></td>
</tr>
<tr>
<td>Region registers</td>
<td>RR</td>
<td>rr</td>
<td>Y</td>
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### Table 2-4. C Syntax Differences

<table>
<thead>
<tr>
<th>Syntax</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>{msb:lsb}, {bit}</td>
<td>Bit field specifier. When appended to a variable, denotes a bit field extending from the most significant bit specified by &quot;msb&quot; to the least significant bit specified by &quot;lsb&quot; including bits &quot;msb&quot; and &quot;lsb&quot;. If &quot;msb&quot; and &quot;lsb&quot; are equal then a single bit is accessed. The second form denotes a single bit.</td>
</tr>
<tr>
<td>u&gt;, u&gt;&gt;, u&lt;, u&lt;=</td>
<td>Unsigned inequality relations. Variables on either side of the operator are treated as unsigned.</td>
</tr>
<tr>
<td>u&gt;&gt;, u&gt;&gt;=</td>
<td>Unsigned right shift. Zeroes are shifted into the most significant bit position.</td>
</tr>
<tr>
<td>u+</td>
<td>Unsigned addition. Operands are treated as unsigned, and zero-extended.</td>
</tr>
<tr>
<td>u*</td>
<td>Unsigned multiplication. Operands are treated as unsigned.</td>
</tr>
</tbody>
</table>

The remainder of this chapter provides a description of each of the Itanium instructions.
add — Add

Format:

\[
(qp) \text{ add } r_1 = r_2, r_3 \quad \text{register_form A1}
\]
\[
(qp) \text{ add } r_1 = r_2, r_3, 1 \quad \text{plus1_form, register_form A1}
\]
\[
(qp) \text{ add } r_1 = \text{imm}, r_3 \quad \text{pseudo-op A1}
\]
\[
(qp) \text{ adds } r_1 = \text{imm}_{14}, r_3 \quad \text{imm14_form A4}
\]
\[
(qp) \text{ add } r_1 = \text{imm}_{22}, r_3 \quad \text{imm22_form A5}
\]

Description:

The two source operands (and an optional constant 1) are added and the result placed in GR \(r_1\). In the register form the first operand is GR \(r_2\); in the imm_{14} form the first operand is taken from the sign-extended \(\text{imm}_{14}\) encoding field; in the imm_{22} form the first operand is taken from the sign-extended \(\text{imm}_{22}\) encoding field. In the imm_{22} form, GR \(r_3\) can specify only GRs 0, 1, 2 and 3. The plus1_form is available only in the register_form (although the equivalent effect in the immediate forms can be achieved by adjusting the immediate).

The immediate-form pseudo-op chooses the imm_{14} form or imm_{22} form based upon the size of the immediate operand and the value of \(r_3\).

Operation:

```c
if (PR[qp]) {
    check_target_register(r_1);

    if (register_form) // register form
        tmp_src = GR[r_2];
    else if (imm14_form) // 14-bit immediate form
        tmp_src = sign_ext(imm_{14}, 14);
    else // 22-bit immediate form
        tmp_src = sign_ext(imm_{22}, 22);

    tmp_nat = (register_form ? GR[r_2].nat : 0);

    if (plus1_form)
        GR[r_1] = tmp_src + GR[r_3] + 1;
    else
        GR[r_1] = tmp_src + GR[r_3];

    GR[r_1].nat = tmp_nat \| GR[r_3].nat;
}
```

Interruptions: Illegal Operation fault
addp4 — Add Pointer

Format:  

\[(qp) \text{ addp4 } r_1 = r_2, r_3 \quad \text{register_form} \quad A1\]
\[(qp) \text{ addp4 } r_1 = \text{imm14}, r_3 \quad \text{imm14_form} \quad A4\]

Description:  
The two source operands are added. The upper 32 bits of the result are forced to zero, and then bits \{31:30\} of GR \(r_3\) are copied to bits \{62:61\} of the result. This result is placed in GR \(r_1\). In the register_form the first operand is GR \(r_2\); in the imm14_form the first operand is taken from the sign-extended \text{imm14} encoding field.

**Figure 2-1. Add Pointer**

![Figure 2-1. Add Pointer](image)

Operation:  

```c
if (PR[qp]) {
    check_target_register(r1);
    tmp_src = (register_form ? GR[r2] : sign_ext(imm14, 14));
    tmp_nat = (register_form ? GR[r2].nat : 0);
    tmp_res = tmp_src + GR[r3];
    tmp_res = zero_ext(tmp_res{31:0}, 32);
    tmp_res{62:61} = GR[r3]{31:30};
    GR[r1] = tmp_res;
    GR[r1].nat = tmp_nat || GR[r3].nat;
}
```

Interruptions:  
Illegal Operation fault
**alloc — Allocate Stack Frame**

**Format:**

\[(qp) \text{ alloc } r_1 = \text{ar.pfs}, i, l, o, r\]

**Description:** A new stack frame is allocated on the general register stack, and the Previous Function State register (PFS) is copied to GR \(r_1\). The change of frame size is immediate. The write of GR \(r_1\) and subsequent instructions in the same instruction group use the new frame.

The four parameters, \(i\) (size of inputs), \(l\) (size of locals), \(o\) (size of outputs), and \(r\) (size of rotating) specify the sizes of the regions of the stack frame.

**Figure 2-2. Stack Frame**

![Stack Frame Diagram](image)

The size of the frame (sof) is determined by \(i + l + o\). Note that this instruction may grow or shrink the size of the current register stack frame. The size of the local region (sol) is given by \(i + l\). There is no real distinction between inputs and locals. They are given as separate operands in the instruction only as a hint to the assembler about how the local registers are to be used.

The rotating registers must fit within the stack frame and be a multiple of 8 in number. If this instruction attempts to change the size of CFM.sor, and the register rename base registers (CFM.rrb.gr, CFM.rrb.fr, CFM.rrb.pr) are not all zero, then the instruction will cause a Reserved Register/Field fault.

Although the assembler does not allow illegal combinations of operands for alloc, illegal combinations can be encoded in the instruction. Attempting to allocate a stack frame larger than 96 registers, or with the rotating region larger than the stack frame, or with the size of locals larger than the stack frame, or specifying a qualifying predicate other than PR 0, will cause an Illegal Operation fault.

This instruction must be the first instruction in an instruction group and must either be in instruction slot 0 or in instruction slot 1 of a template having a stop after slot 0; otherwise, the results are undefined.

If insufficient registers are available to allocate the desired frame alloc will stall the processor until enough dirty registers are written to the backing store. Such mandatory RSE stores may cause the data related faults listed below.
Operation:

// tmp_sof, tmp_sol, tmp_sor are the fields encoded in the instruction

\[
\begin{align*}
\text{tmp_sof} &= i + l + o; \\
\text{tmp_sol} &= i + l; \\
\text{tmp_sor} &= r \uparrow\uparrow 3; \\
\end{align*}
\]

check_target_register_sof(r, tmp_sof);
if (tmp_sof > 96 || r > tmp_sof || tmp_sol > tmp_sof || qp != 0)
   illegal_operation_fault();
if (tmp_sor != CFM.sor &&
    (CFM.rrb.gr != 0 || CFM.rrb.fr != 0 || CFM.rrb.pr != 0))
   reserved_register_field_fault();
alat_frame_update(0, tmp_sof - CFM.sof);
rse_new_frame(CFM.sof, tmp_sof); // Make room for new registers; Mandatory
   // RSE stores can raise faults listed below.

   CFM.sof = tmp_sof;
   CFM.sol = tmp_sol;
   CFM.sor = tmp_sor;
   \[
   \begin{align*}
   \text{GR}[r] &= \text{AR[PFS]}; \\
   \text{GR}[r].nat &= 0; \\
   \end{align*}
   \]

Interruptions:

Illegal Operation fault
Reserved Register/Field fault
Unimplemented Data Address fault
VHPT Data fault
Data Nested TLB fault
Data TLB fault
Alternate Data TLB fault
Data Page Not Present fault

Data NaT Page Consumption fault
Data Key Miss fault
Data Key Permission fault
Data Access Rights fault
Data Dirty Bit fault
Data Access Bit fault
Data Debug fault
and — Logical And

**Format:**

<table>
<thead>
<tr>
<th>Format</th>
<th>Description</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>$(qp)$ and $r_1 = r_2, r_3$</td>
<td>register_form</td>
<td>A1</td>
</tr>
<tr>
<td>$(qp)$ and $r_1 = imm_8, r_3$</td>
<td>imm8_form</td>
<td>A3</td>
</tr>
</tbody>
</table>

**Description:** The two source operands are logically ANDed and the result placed in GR $r_1$. In the register_form the first operand is GR $r_2$; in the imm8_form the first operand is taken from the $imm_8$ encoding field.

**Operation:**

```c
if (PR[qp]) {
    check_target_register(r_1);

    tmp_src = (register_form ? GR[r_2] : sign_ext(imm_8, 8));
    tmp_nat = (register_form ? GR[r_2].nat : 0);

    GR[r_1] = tmp_src & GR[r_3];
    GR[r_1].nat = tmp_nat || GR[r_3].nat;
}
```

**Interruptions:** Illegal Operation fault
**andcm — And Complement**

**Format:**
- \((qp)\) andcm \(r_1 = r_2, r_3\)  \hspace{1cm} \text{register\_form} \hspace{1cm} A1
- \((qp)\) andcm \(r_1 = \text{imm}_8, r_3\)  \hspace{1cm} \text{imm8\_form} \hspace{1cm} A3

**Description:** The first source operand is logically ANDed with the 1’s complement of the second source operand and the result placed in \(GR\ r_1\). In the register_form the first operand is \(GR\ r_2\); in the imm8_form the first operand is taken from the \(imm_8\) encoding field.

**Operation:**
```c
if (PR[qp]) {
    check_target_register(r1);
    tmp_src = (register_form ? GR[r2] : sign_ext(imm8, 8));
    tmp_nat = (register_form ? GR[r2].nat : 0);
    GR[r1] = tmp_src & ~GR[r3];
    GR[r1].nat = tmp_nat || GR[r3].nat;
}
```

**Interruptions:** Illegal Operation fault
br — Branch

Format:  
\[(qp) \text{br.btype.bwh.ph.dh target25} \]
\[(qp) \text{br.btype.bwh.ph.dh } b_1 = \text{target25} \]
\[(qp) \text{br.btype.bwh.ph.dh target25} \]
\[(qp) \text{br.ph.dh target25} \]
\[(qp) \text{br.btype.bwh.ph.dh b2} \]
\[(qp) \text{br.btype.bwh.ph.dh } b_1 = b_2 \]
\[(qp) \text{br.ph.dh } b_2 \]

Description:  
A branch condition is evaluated, and either a branch is taken, or execution continues with the next sequential instruction. The execution of a branch logically follows the execution of all previous non-branch instructions in the same instruction group. On a taken branch, execution begins at slot 0.

Branches can be either IP-relative, or indirect. For IP-relative branches, the target operand, in assembly, specifies a label to branch to. This is encoded in the branch instruction as a signed immediate displacement \((imm_{21})\) between the target bundle and the bundle containing this instruction \((imm_{21} = \text{target25} – \text{IP} >> 4)\). For indirect branches, the target address is taken from BR \(b_2\).

<table>
<thead>
<tr>
<th>btype</th>
<th>Function</th>
<th>Branch Condition</th>
<th>Target Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>cond or none</td>
<td>Conditional branch</td>
<td>Qualifying predicate</td>
<td>IP-rel or Indirect</td>
</tr>
<tr>
<td>call</td>
<td>Conditional procedure call</td>
<td>Qualifying predicate</td>
<td>IP-rel or Indirect</td>
</tr>
<tr>
<td>ret</td>
<td>Conditional procedure return</td>
<td>Qualifying predicate</td>
<td>Indirect</td>
</tr>
<tr>
<td>ia</td>
<td>Invoke IA-32 instruction set</td>
<td>Unconditional</td>
<td>Indirect</td>
</tr>
<tr>
<td>cloop</td>
<td>Counted loop branch</td>
<td>Loop count</td>
<td>IP-rel</td>
</tr>
<tr>
<td>clop, cexit</td>
<td>Mod-scheduled counted loop</td>
<td>Loop count and epilog count</td>
<td>IP-rel</td>
</tr>
<tr>
<td>wtop, wexit</td>
<td>Mod-scheduled while loop</td>
<td>Qualifying predicate and epilog count</td>
<td>IP-rel</td>
</tr>
</tbody>
</table>

There are two pseudo-ops for unconditional branches. These are encoded like a conditional branch \((\text{btype} = \text{cond})\), with the \(qp\) field specifying PR 0, and with the \(bwh\) hint of sptk.

The branch type determines how the branch condition is calculated and whether the branch has other effects (such as writing a link register). For the basic branch types, the branch condition is simply the value of the specified predicate register. These basic branch types are:

- **cond**: If the qualifying predicate is 1, the branch is taken. Otherwise it is not taken.
- **call**: If the qualifying predicate is 1, the branch is taken and several other actions occur:
  - The current values of the Current Frame Marker (CFM), the EC application register and the current privilege level are saved in the Previous Function State application register.
  - The caller’s stack frame is effectively saved and the callee is provided with a frame containing only the caller’s output region.
  - The rotation rename base registers in the CFM are reset to 0.
  - A return link value is placed in BR \(b_1\).
• **return:** If the qualifying predicate is 1, the branch is taken and the following occurs:
  - CFM, EC, and the current privilege level are restored from PFS. (The privilege level is restored only if this does not increase privilege.)
  - The caller’s stack frame is restored.
  - If the return lowers the privilege, and PSR.lp is 1, then a Lower-Privilege Transfer trap is taken.

• **ia:** The branch is taken unconditionally, if it is not intercepted by the OS. The effect of the branch is to invoke the IA-32 instruction set (by setting PSR.is to 1) and begin processing IA-32 instructions at the virtual linear target address contained in BR \( b_2^{31:0} \). If the qualifying predicate is not PR 0, an Illegal Operation fault is raised. If instruction set transitions are disabled (PSR.di is 1), then a Disabled Instruction Set Transition fault is raised. The IA-32 target effective address is calculated relative to the current code segment, i.e. \( \text{EIP}^{31:0} = \text{BR}^{31:0} - \text{CSD.base} \). The IA-32 instruction set can be entered at any privilege level, provided PSR.di is 0. If PSR.dih is 1, a Disabled FP Register fault is raised on the target IA-32 instruction. No register bank switch nor change in privilege level occurs during the instruction set transition.

Software must ensure the code segment descriptor (CSD) and selector (CS) are loaded before issuing the branch. If the target EIP value exceeds the code segment limit or has a code segment privilege violation, an IA-32_Exception(GPFault) is raised on the target IA-32 instruction. For entry into 16-bit IA-32 code, if \( b_2 \) is not within 64K-bytes of CSD.base a GPFault is raised on the target instruction. EFLAGrf is unmodified until the successful completion of the first IA-32 instruction. PSR.da, PSR.id, PSR.ia, PSR.dd, and PSR.ed are cleared to zero after br.ia completes execution and before the first IA-32 instruction begins execution. EFLAGrf is not cleared until the target IA-32 instruction successfully completes.

Software must issue a `mf` instruction before the branch if memory ordering is required between IA-32 processor consistent and Itanium unordered memory references. The processor does not ensure Itanium-instruction-set-generated writes into the instruction stream are seen by subsequent IA-32 instruction fetches. br.ia does not perform an instruction serialization operation. The processor does ensure that prior writes (even in the same instruction group) to GRs and FRs are observed by the first IA-32 instruction. Writes to ARs within the same instruction group as br.ia are not allowed, since br.ia may implicitly reads all ARs. If an illegal RAW dependency is present between an AR write and br.ia, the first IA-32 instruction fetch and execution may or may not see the updated AR value.

IA-32 instruction set execution leaves the contents of the ALAT undefined. Software can not rely on ALAT values being preserved across an instruction set transition. All registers left in the current register stack frame are undefined across an instruction set transition. On entry to IA-32 code, existing entries in the ALAT are ignored. If the register stack contains any dirty registers, an Illegal Operation fault is raised on the br.ia instruction. The current register stack frame is forced to zero. To flush the register file of dirty registers, the `flushrs` instruction must be issued in an instruction group preceding the br.ia instruction. To enhance the performance of the instruction set transition, software can start the register stack flush in parallel with starting the IA-32 instruction set by 1) ensuring `flushrs` is exactly one instruction group before the br.ia, and 2) br.ia is in the first B-slot. br.ia should always be executed in the first B-slot with a hint of “static-taken” (default), otherwise processor performance will be degraded.

If a br.ia causes any Itanium traps (e.g., Single Step trap, Taken Branch trap, or Unimplemented Instruction Address trap), IIP will contain the original 64-bit target IP. (The value will not have been zero extended from 32 bits.)
Another branch type is provided for simple counted loops. This branch type uses the Loop Count application register (LC) to determine the branch condition, and does not use a qualifying predicate:

- **cloop**: If the LC register is not equal to zero, it is decremented and the branch is taken.

In addition to these simple branch types, there are four types which are used for accelerating modulo-scheduled loops (see also Section 4.5.1, “Modulo-scheduled Loop Support” on page 1:66). Two of these are for counted loops (which use the LC register), and two for while loops (which use the qualifying predicate). These loop types use register rotation to provide register renaming, and they use predication to turn off instructions that correspond to empty pipeline stages.

The Epilog Count application register (EC) is used to count epilog stages and, for some while loops, a portion of the prolog stages. In the epilog phase, EC is decremented each time around and, for most loops, when EC is one, the pipeline has been drained, and the loop is exited. For certain types of optimized, unrolled software-pipelined loops, the target of **br.cexit** or **br.wexit** is set to the next sequential bundle. In this case, the pipeline may not be fully drained when EC is one, and continues to drain while EC is zero.

For these modulo-scheduled loop types, the calculation of whether the branch is taken or not depends on the kernel branch condition (LC for counted types, and the qualifying predicate for while types) and on the epilog condition (whether EC is greater than one or not).

These branch types are of two categories: top and exit. The top types (ctop and wtop) are used when the loop decision is located at the bottom of the loop body and therefore a taken branch will continue the loop while a fall through branch will exit the loop. The exit types (cexit and wexit) are used when the loop decision is located somewhere other than the bottom of the loop and therefore a fall through branch will continue the loop and a taken branch will exit the loop. The exit types are also used at intermediate points in an unrolled pipelined loop. (For more details, see Section 4.5.1, “Modulo-scheduled Loop Support” on page 1:66).

The modulo-scheduled loop types are:

- **ctop** and **cexit**: These branch types behave identically, except in the determination of whether to branch or not. For **br.ctop**, the branch is taken if either LC is non-zero or EC is greater than one. For **br.cexit**, the opposite is true. It is not taken if either LC is non-zero or EC is greater than one and is taken otherwise.

  These branch types also use LC and EC to control register rotation and predicate initialization. During the prolog and kernel phase, when LC is non-zero, LC counts down. When **br.ctop** or **br.cexit** is executed with LC equal to zero, the epilog phase is entered, and EC counts down. When **br.ctop** or **br.cexit** is executed with LC equal to zero and EC equal to one, a final decrement of EC and a final register rotation are done. If LC and EC are equal to zero, register rotation stops. These other effects are the same for the two branch types, and are described in Figure 2-3.

- **wtop** and **wexit**: These branch types behave identically, except in the determination of whether to branch or not. For **br.wtop**, the branch is taken if either the qualifying predicate is one or EC is greater than one. For **br.wexit**, the opposite is true. It is not taken if either the qualifying predicate is one or EC is greater than one, and is taken otherwise.
These branch types also use the qualifying predicate and EC to control register rotation and predicate initialization. During the prolog phase, the qualifying predicate is either zero or one, depending upon the scheme used to program the loop. During the kernel phase, the qualifying predicate is one. During the epilog phase, the qualifying predicate is zero, and EC counts down. When br.wtop or br.wexit is executed with the qualifying predicate equal to zero and EC equal to one, a final decrement of EC and a final register rotation are done. If the qualifying predicate and EC are zero, register rotation stops. These other effects are the same for the two branch types, and are described in Figure 2-4.

The loop-type branches (br.cloop, br.ctop, br.cexit, br.wtop, and br.wexit) are only allowed in instruction slot 2 within a bundle. Executing such an instruction in either slot 0 or 1 will cause an Illegal Operation fault, whether the branch would have been taken or not.
Read after Write (RAW) and Write after Read (WAR) dependency requirements are slightly different for branch instructions. Changes to BRs, PRs, and PFS by non-branch instructions are visible to a subsequent branch instruction in the same instruction group (i.e., a limited RAW is allowed for these resources). This allows for a low-latency compare-branch sequence, for example. The normal RAW requirements apply to the LC and EC application registers, and the RRBs.

Within an instruction group, a WAR dependency on PR 63 is not allowed if both the reading and writing instructions are branches. For example, a `br.wtop` or `br.wexit` may not use PR[63] as its qualifying predicate and PR[63] cannot be the qualifying predicate for any branch preceding a `br.wtop` or `br.wexit` in the same instruction group.

For dependency purposes, the loop-type branches effectively always write their associated resources, whether they are taken or not. The cloop type effectively always writes LC. When LC is 0, a cloop branch leaves it unchanged, but hardware may implement this as a re-write of LC with the same value. Similarly, `br.ctop` and `br.cexit` effectively always write LC, EC, the RRBs, and PR[63].

Values for various branch hint completers are shown in the following tables. Whether Prediction Strategy hints are shown in Table 2-7. Sequential Prefetch hints are shown in Table 2-8. Branch Cache Deallocation hints are shown in Table 2-9. See Section 4.5.2, “Branch Prediction Hints” on page 1:68.

### Table 2-7. Branch Whether Hint

<table>
<thead>
<tr>
<th>bwh Completer</th>
<th>Branch Whether Hint</th>
</tr>
</thead>
<tbody>
<tr>
<td>spnt</td>
<td>Static Not-Taken</td>
</tr>
<tr>
<td>spkt</td>
<td>Static Taken</td>
</tr>
<tr>
<td>dpnt</td>
<td>Dynamic Not-Taken</td>
</tr>
<tr>
<td>dpkt</td>
<td>Dynamic Taken</td>
</tr>
</tbody>
</table>

### Table 2-8. Sequential Prefetch Hint

<table>
<thead>
<tr>
<th>ph Completer</th>
<th>Sequential Prefetch Hint</th>
</tr>
</thead>
<tbody>
<tr>
<td>few or none</td>
<td>Few lines</td>
</tr>
<tr>
<td>many</td>
<td>Many lines</td>
</tr>
</tbody>
</table>

### Table 2-9. Branch Cache Deallocation Hint

<table>
<thead>
<tr>
<th>dh Completer</th>
<th>Branch Cache Deallocation Hint</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Don’t deallocate</td>
</tr>
<tr>
<td>clr</td>
<td>Deallocate branch information</td>
</tr>
</tbody>
</table>

**Operation:**

```c
if (ip_relative_form) // determine branch target
    tmp_IP = IP + sign_ext((imm_21 << 4), 25);
else // indirect_form
    tmp_IP = BR[b2];

if (btype != ‘ia’) // for Itanium branches,
    tmp_IP = tmp_IP & ~0xf; // ignore bottom 4 bits of target
lower_priv_transition = 0;

switch (btype) {
    case ‘cond’: // simple conditional branch
        tmp_taken = PR[qp];
        break;
```
case 'call': // call saves a return link
    tmp_taken = PR[qp];
    if (tmp_taken) {
        BR[b] = IP + 16;
        AR[PFS].pfm = CFM; // ... and saves the stack frame
        AR[PFS].pec = AR[EC];
        AR[PFS].ppl = PSR.cpl;
        alat_frame_update(CFM.sol, 0);
        rse_preserve_frame(CFM.sol);
        CFM.sof -= CFM.sol; // new frame size is size of outs
        CFM.sol = 0;
        CFM.sor = 0;
        CFM.rrb.gr = 0;
        CFM.rrb.fr = 0;
    }
    break;

case 'ret': // return restores stack frame
    tmp_taken = PR[qp];
    if (tmp_taken) {
        // tmp_growth indicates the amount to move logical TOP *up*:
        // tmp_growth = sizeof(previous out) - sizeof(current frame)
        // a negative amount indicates a shrinking stack
        tmp_growth = (AR[PFS].pfm.sof - AR[PFS].pfm.sol) - CFM.sof;
        alat_frame_update(-AR[PFS].pfm.sol, 0);
        rse_fatal = rse_restore_frame(AR[PFS].pfm.sol, tmp_growth, CFM.sof);
        if (rse_fatal) { // See Section 6.4, “RSE Operation” on page 2:119
            CFM.sof = 0;
            CFM.sol = 0;
            CFM.sor = 0;
            CFM.rrb.gr = 0;
            CFM.rrb.fr = 0;
        } else // normal branch return
        CFM = AR[PFS].pfm;
        rse_enable_current_frame_load();
        AR[EC] = AR[PFS].pec;
        if (PSR.cpl < AR[PFS].ppl) { // ... and restores privilege
            PSR.cpl = AR[PFS].ppl;
            lower_priv_transition = 1;
        }
    }
    break;

case 'ia': // switch to IA mode
    tmp_taken = 1;
    if (qp != 0)
        illegal_operation_fault();
    if (AR[BSPSTORE] != AR[BSP])
        illegal_operation_fault();
    if (PSR.di)
        disabled_instruction_set_transition_fault();
    PSR.is = 1; // set IA-32 Instruction Set Mode
    CFM.sof = 0; //force current stack frame
    CFM.sol = 0; //to zero
CFM.sor = 0;
CFM.rrb.gr = 0;
CFM.rrb.fr = 0;
CFM.rrb.pr = 0;
rsr_invalidate_non_current_regs();
// compute effective instruction pointer
EIP{31:0} = tmp_IP{31:0} - AR[CSD].Base;

// Note the register stack is disabled during IA-32 instruction
// set execution
break;

case 'cloop': // simple counted loop
if (slot != 2)
    illegal_operation_fault();
tmp_taken = (AR[LC] != 0);
if (AR[LC] != 0)
    AR[LC]--;
break;

case 'ctop':
case 'cexit': // SW pipelined counted loop
if (slot != 2)
    illegal_operation_fault();
if (btype == 'ctop') tmp_taken = ((AR[LC] != 0) || (AR[EC] u> 1));
if (btype == 'cexit') tmp_taken = !((AR[LC] != 0) || (AR[EC] u> 1));
if (AR[LC] != 0) {
    AR[LC]--;
    AR[EC] = AR[EC];
    PR[63] = 1;
    rotate_regs();
} else if (AR[EC] != 0) {
    AR[LC] = AR[LC];
    AR[EC]--;
    PR[63] = 0;
    rotate_regs();
} else {
    AR[LC] = AR[LC];
    AR[EC] = AR[EC];
    PR[63] = 0;
    CFM.rrb.gr = CFM.rrb.gr;
    CFM.rrb.fr = CFM.rrb.fr;
    CFM.rrb.pr = CFM.rrb.pr;
}
break;

case 'wtop':
case 'wexit': // SW pipelined while loop
if (slot != 2)
    illegal_operation_fault();
if (btype == 'wtop') tmp_taken = (PR[qp] || (AR[EC] u> 1));
if (btype == 'wexit') tmp_taken = !(PR[qp] || (AR[EC] u> 1));
if (PR[qp]) {
    AR[EC] = AR[EC];
    PR[63] = 0;
    rotate_regs();
} else if (AR[EC] != 0) {
    AR[EC]--;
    PR[63] = 0;
    rotate_regs();
} else {
    AR[EC] = AR[EC];
PR[63] = 0;
CFM.rrb.gr = CFM.rrb.gr;
CFM.rrb.fr = CFM.rrb.fr;
CFM.rrb.pr = CFM.rrb.pr;
}
break;
}
if (tmp_taken) {
    taken_branch = 1;
    IP = tmp_IP;       // set the new value for IP
    if ((PSR.it && unimplemented_virtual_address(tmp_IP))
        || (!PSR.it && unimplemented_physical_address(tmp_IP)))
        unimplemented_instruction_address_trap(lower_priv_transition,
                                                  tmp_IP);
    if (lower_priv_transition && PSR.lp)
        lower_privilege_transfer_trap();
    if (PSR.tb)
        taken_branch_trap();
}

**Interruptions:**
- Illegal Operation fault
- Lower-Privilege Transfer trap
- Disabled Instruction Set Transition fault
- Taken Branch trap
- Unimplemented Instruction Address trap

Additional Faults on IA-32 target instructions:
- IA-32_Exception(GPFault)
- Disabled FP Reg Fault if PSR.dfh is 1
break — Break

Format:

\[
(qp) \text{ break }\ imm_{21} \\
(qp) \text{ break.i } \ imm_{21} \\
(qp) \text{ break.b } \ imm_{21} \\
(qp) \text{ break.m } \ imm_{21} \\
(qp) \text{ break.f } \ imm_{21} \\
(qp) \text{ break.x } \ imm_{62}
\]

pseudo-op
i_unit_form I19
b_unit_form B9
m_unit_form M37
f_unit_form F15
x_unit_form X1

Description: A Break Instruction fault is taken. For the i_unit_form, f_unit_form and m_unit_form, the value specified by \( imm_{21} \) is zero-extended and placed in the Interruption Immediate control register (IIM).

For the b_unit_form, \( imm_{21} \) is ignored and the value zero is placed in the Interruption Immediate control register (IIM).

For the x_unit_form, the lower 21 bits of the value specified by \( imm_{62} \) is zero-extended and placed in the Interruption Immediate control register (IIM). The L slot of the bundle contains the upper 41 bits of \( imm_{62} \).

A break.i instruction may be encoded in an MLI-template bundle, in which case the L slot of the bundle is ignored.

This instruction has five forms, each of which can be executed only on a particular execution unit type. The pseudo-op can be used if the unit type to execute on is unimportant.

Operation:

\[
\text{if (PR[qp])} \\
\hspace{1em} \text{if (b_unit_form)} \\
\hspace{2em} \text{immediate} = 0; \\
\hspace{1em} \text{else if (x_unit_form)} \\
\hspace{2em} \text{immediate} = \text{zero_ext}(imm_{62}, 21); \\
\hspace{1em} \text{else} // i_unit_form | | m_unit_form | | f_unit_form \\
\hspace{2em} \text{immediate} = \text{zero_ext}(imm_{21}, 21); \\
\hspace{1em} \text{break_instruction_fault(immediate);} \\
\]

Interruptions: Break Instruction fault
**brl — Branch Long**

**Format:**

\[
\begin{align*}
(qp) & \text{ brl.btype.bwh.ph.dh } target_{64} & \text{ X3} \\
(qp) & \text{ brl.btype.bwh.ph.dh } b_1 = target_{64} & \text{ call_form } X4 \\
& \text{ brl.ph.dh } target_{64} & \text{ pseudo-op}
\end{align*}
\]

**Description:** A branch condition is evaluated, and either a branch is taken, or execution continues with the next sequential instruction. The execution of a branch logically follows the execution of all previous non-branch instructions in the same instruction group. On a taken branch, execution begins at slot 0.

Long branches are always IP-relative. The \texttt{target}_{64} operand, in assembly, specifies a label to branch to. This is encoded in the long branch instruction as an immediate displacement (\texttt{imm}_{60}) between the target bundle and the bundle containing this instruction (\texttt{imm}_{60} = \texttt{target}_{64} – IP >> 4). The L slot of the bundle contains 39 bits of \texttt{imm}_{60}.

<table>
<thead>
<tr>
<th>\texttt{btype}</th>
<th>Function</th>
<th>Branch Condition</th>
<th>Target Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>cond or none</td>
<td>Conditional branch</td>
<td>Qualifying predicate</td>
<td>IP-relative</td>
</tr>
<tr>
<td>call</td>
<td>Conditional procedure call</td>
<td>Qualifying predicate</td>
<td>IP-relative</td>
</tr>
</tbody>
</table>

There is a pseudo-op for long unconditional branches, encoded like a conditional branch (\texttt{btype = cond}), with the \texttt{qp} field specifying PR 0, and with the \texttt{bwh} hint of sptk.

The branch type determines how the branch condition is calculated and whether the branch has other effects (such as writing a link register). For all long branch types, the branch condition is simply the value of the specified predicate register:

- **cond:** If the qualifying predicate is 1, the branch is taken. Otherwise it is not taken.
- **call:** If the qualifying predicate is 1, the branch is taken and several other actions occur:
  - The current values of the Current Frame Marker (CFM), the EC application register and the current privilege level are saved in the Previous Function State application register.
  - The caller’s stack frame is effectively saved and the callee is provided with a frame containing only the caller’s output region.
  - The rotation rename base registers in the CFM are reset to 0.
  - A return link value is placed in BR \texttt{b1}.

Read after Write (RAW) and Write after Read (WAR) dependency requirements for long branch instructions are slightly different than for other instructions but are the same as for branch instructions. See page 3:21 for details.

This instruction must be immediately followed by a stop; otherwise its behavior is undefined.

Values for various branch hint completers are the same as for branch instructions. Whether Prediction Strategy hints are shown in Table 2-7 on page 3:21, Sequential Prefetch hints are shown in Table 2-8 on page 3:21, and Branch Cache Deallocation hints are shown in Table 2-9 on page 3:21. See Section 4.5.2, “Branch Prediction Hints” on page 1:68.

This instruction is not implemented on the Itanium processor, which takes an Illegal Operation fault whenever a long branch instruction is encountered, regardless of whether the branch is taken or not. To support the Itanium processor, the operating system is required to provide an Illegal Operation fault handler which emulates taken and not-taken long branches. Presence of this instruction is indicated by a 1 in the lb bit of CPUID register 4. See Section 3.1.11, “Processor Identification Registers” on page 1:29.
Operation:

tmp_IP = IP + (imm_{60} \ll 4);  // determine branch target
if (!followed_by_stop())
    undefined_behavior();
if (!long_branch_implemented())
    illegal_operation_fault();

switch (btype) {
    case 'cond':  // simple conditional branch
        tmp_taken = PR[qp];
        break;
    case 'call':  // call saves a return link
        tmp_taken = PR[qp];
        if (tmp_taken) {
            BR[b_1] = IP + 16;

            AR[PFS].pfm = CFM;  // ... and saves the stack frame
            AR[PFS].pec = AR[EC];
            AR[PFS].ppl = PSR.cpl;

            alat_frame_update(CFM.sol, 0);
            rse_preserve_frame(CFM.sol);
            CFM.sof -= CFM.sol;  // new frame size is size of outs
            CFM.sol = 0;
            CFM.sor = 0;
            CFM.rrb.gr = 0;
            CFM.rrb.fr = 0;
            CFM.rrb.pr = 0;
        }
        break;
}
if (tmp_taken) {
    taken_branch = 1;
    IP = tmp_IP;  // set the new value for IP
    if ((PSR.it && unimplemented_virtual_address(tmp_IP))
        || ((PSR.it && unimplemented_physical_address(tmp_IP)))
        unimplemented_instruction_address_trap(0,tmp_IP);
    if (PSR.tb)
        taken_branch_trap();
}

Interruptions:
Illegal Operation fault  Taken Branch trap
Unimplemented Instruction Address trap
**brp — Branch Predict**

**Format:**
- `brp.ipwh.ih  target25, tag13`
- `brp.indwh.ih  b2, tag13`
- `brp.ret.indwh.ih  b2, tag13`

**Description:**
This instruction can be used to provide to hardware early information about a future branch. It has no effect on architectural machine state, and operates as a `nop` instruction except for its performance effects.

The `tag13` operand, in assembly, specifies the address of the branch instruction to which this prediction information applies. This is encoded in the branch predict instruction as a signed immediate displacement (`timm9`) between the bundle containing the presaged branch and the bundle containing this instruction (`timm9 = tag13 - IP >> 4`).

The `target25` operand, in assembly, specifies the label that the presaged branch will have as its target. This is encoded in the branch predict instruction exactly as in branch instructions, with a signed immediate displacement (`imm21`) between the target bundle and the bundle containing this instruction (`imm21 = target25 - IP >> 4`). The indirect_form can be used to presage an indirect branch. In the indirect_form, the target of the presaged branch is given by `BR b2`.

The return_form is used to indicate that the presaged branch will be a return.

Other hints can be given about the presaged branch. Values for various hint completers are shown in the following tables. For more details, refer to Section 4.5.2, “Branch Prediction Hints” on page 1:68.

The `ipwh` and `indwh` completers provide information about how best the branch condition should be predicted, when the branch is reached.

### Table 2-11. IP-relative Branch Predict Whether Hint

<table>
<thead>
<tr>
<th><code>ipwh</code> Completer</th>
<th>IP-relative Branch Predict Whether Hint</th>
</tr>
</thead>
<tbody>
<tr>
<td>sptk</td>
<td>Presaged branch should be predicted Static Taken</td>
</tr>
<tr>
<td>loop</td>
<td>Presaged branch will be br.cloop,br.ctop,br.wtop</td>
</tr>
<tr>
<td>exit</td>
<td>Presaged branch will be br.cexit or br.wexit</td>
</tr>
<tr>
<td>dptk</td>
<td>Presaged branch should be predicted Dynamically</td>
</tr>
</tbody>
</table>

### Table 2-12. Indirect Branch Predict Whether Hint

<table>
<thead>
<tr>
<th><code>indwh</code> Completer</th>
<th>Indirect Branch Predict Whether Hint</th>
</tr>
</thead>
<tbody>
<tr>
<td>sptk</td>
<td>Presaged branch should be predicted Static Taken</td>
</tr>
<tr>
<td>dptk</td>
<td>Presaged branch should be predicted Dynamically</td>
</tr>
</tbody>
</table>

The `ih` completer can be used to mark a small number of very important branches (e.g., an inner loop branch). This can signal to hardware to use faster, smaller prediction structures for this information.

### Table 2-13. Importance Hint

<table>
<thead>
<tr>
<th><code>ih</code> Completer</th>
<th>Branch Predict Importance Hint</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Less important</td>
</tr>
<tr>
<td>imp</td>
<td>More important</td>
</tr>
</tbody>
</table>
Operation:

\[
\text{tmp}\_\text{tag} = \text{IP} + \text{sign\_ext}((\text{timm}_9 << 4), 13);
\]

if (ip\_relative\_form) {
    \[
    \text{tmp}\_\text{target} = \text{IP} + \text{sign\_ext}((\text{imm}_{21} << 4), 25);
    \]
    \[
    \text{tmp}\_\text{wh} = \text{ipwh};
    \]
} else { // indirect\_form
    \[
    \text{tmp}\_\text{target} = \text{BR}[b_2];
    \]
    \[
    \text{tmp}\_\text{wh} = \text{indwh};
    \]
}

branch\_predict(tmp\_wh, ih, return\_form, tmp\_target, tmp\_tag);

Interruptions: None
bsw — Bank Switch

**Format:**
- bsw.0  
  zero_form  B8
- bsw.1  
  one_form  B8

**Description:**
This instruction switches to the specified register bank. The zero_form specifies Bank 0 for GR16 to GR31. The one_form specifies Bank 1 for GR16 to GR31. After the bank switch the previous register bank is no longer accessible but does retain its current state. If the new and old register banks are the same, bsw is effectively a *nop*, although there may be a performance degradation.

A bsw instruction must be the last instruction in an instruction group. Otherwise, an Illegal Operation fault is taken. Instructions in the same instruction group that access GR16 to GR31 reference the previous register bank. Subsequent instruction groups reference the new register bank.

This instruction can only be executed at the most privileged level.

This instruction cannot be predicated.

**Operation:**
```c
if (!followed_by_stop())
    illegal_operation_fault();

if (PSR.cpl != 0)
    privileged_operation_fault(0);

if (zero_form)
    PSR.bn = 0;
else // one_form
    PSR.bn = 1;
```

**Interruptions:**
- Illegal Operation fault
- Privileged Operation fault

**Serialization:**
This instruction does not require any additional instruction or data serialization operation. The bank switch occurs synchronously with its execution.
chk — Speculation Check

Format:

- `(qp) chk.s r2, target25` pseudo-op
- `(qp) chk.s.i r2, target25` control_form, i_unit_form, gr_form I20
- `(qp) chk.s.m r2, target25` control_form, m_unit_form, gr_form M20
- `(qp) chk.s f2, target25` control_form, fr_form M21
- `(qp) chk.a.aclr r1, target25` data_form, gr_form M22
- `(qp) chk.a.aclr f1, target25` data_form, fr_form M23

Description: The result of a control- or data-speculative calculation is checked for success or failure. If the check fails, a branch to `target25` is taken.

In the control_form, success is determined by a NaT indication for the source register. If the NaT bit corresponding to GR `r2` is 1 (in the gr_form), or FR `f2` contains a NaTVal (in the fr_form), the check fails.

In the data_form, success is determined by the ALAT. The ALAT is queried using the general register specifier `r1` (in the gr_form), or the floating-point register specifier `f1` (in the fr_form). If no ALAT entry matches, the check fails. An implementation may optionally cause the check to fail independent of whether an ALAT entry matches. A `chk.a` with general register specifier `r0` or floating-point register specifiers `f0` or `f1` always fails.

The `target25` operand, in assembly, specifies a label to branch to. This is encoded in the instruction as a signed immediate displacement (`imm21`) between the target bundle and the bundle containing this instruction (`imm21 = target25 – IP >> 4`).

The branching behavior of this instruction can be optionally unimplemented. If the instruction would have branched, and the branching behavior is not implemented, then a Speculative Operation fault is taken and the value specified by `imm21` is zero-extended and placed in the Interruption Immediate control register (IIM). The fault handler emulates the branch by sign-extending the IIM value, adding it to IIP and returning.

The control_form of this instruction for checking general registers can be encoded on either an I-unit or an M-unit. The pseudo-op can be used if the unit type to execute on is unimportant.

For the data_form, if an ALAT entry matches, the matching ALAT entry can be optionally invalidated, based on the value of the `aclr` completer (See Table 2-14).

**Table 2-14. ALAT Clear Completer**

<table>
<thead>
<tr>
<th>aclr Completer</th>
<th>Effect on ALAT</th>
</tr>
</thead>
<tbody>
<tr>
<td>clr</td>
<td>Invalidate matching ALAT entry</td>
</tr>
<tr>
<td>nc</td>
<td>Don’t invalidate</td>
</tr>
</tbody>
</table>

Note that if the `clr` value of the `aclr` completer is used and the check succeeds, the matching ALAT entry is invalidated. However, if the check fails (which may happen even if there is a matching ALAT entry), any matching ALAT entry may optionally be invalidated, but this is not required. Recovery code for data speculation, therefore, cannot rely on the absence of a matching ALAT entry.
Operation: if (PR[gp]) {
    if (control_form) {
        if (fr_form && (tmp_isrcode = fp_reg_disabled(f2, 0, 0, 0)))
            disabled_fp_register_fault(tmp_isrcode, 0);
        check_type = gr_form ? CHKS_GENERAL : CHKS_FLOAT;
        fail = (gr_form && GR[r2].nat) || (fr_form && FR[f2] == NATVAL);
    } else { // data_form
        if (gr_form) {
            reg_type = GENERAL;
            check_type = CHKA_GENERAL;
            alat_index = r1;
            always_fail = (alat_index == 0);
        } else { // fr_form
            reg_type = FLOAT;
            check_type = CHKA_FLOAT;
            alat_index = f1;
            always_fail = ((alat_index == 0) || (alat_index == 1));
        }
        fail = (always_fail || (!alat_cmp(reg_type, alat_index)));
    }
    if (fail) {
        if (check_branch_implemented(check_type)) {
            taken_branch = 1;
            IP = IP + sign_ext((imm21 << 4), 25);
            if ((PSR.it && unimplemented_virtual_address(IP))
                || (PSR.it && unimplemented_physical_address(IP))
                || unimplemented_instruction_address_trap(0, IP);
                if (PSR.tb)
                    taken_branch_trap();
            } else
                speculation_fault(check_type, zero_ext(imm21, 21));
        } else if (data_form && (aclr == 'clr'))
            alat_inval_single_entry(reg_type, alat_index);
    }
}

Interruptions: Disabled Floating-point Register fault Unimplemented Instruction Address trap
Speculative Operation fault Taken Branch trap
**clrrrb — Clear RRB**

**Format:**

```plaintext
clrrb
clrrb.pr
```

**all_form**

```plaintext
B8
```

**pred_form**

```plaintext
B8
```

**Description:**

In the all_form, the register rename base registers (CFM.rrb.gr, CFM.rrb.fr, and CFM.rrb.pr) are cleared. In the pred_form, the single register rename base register for the predicates (CFM.rrb.pr) is cleared.

This instruction must be the last instruction in an instruction group, or an Illegal Operation fault is taken.

This instruction cannot be predicated.

**Operation:**

```plaintext
if (!followed_by_stop())
    illegal_operation_fault();

if (all_form) {
    CFM.rrb.gr = 0;
    CFM.rrb.fr = 0;
    CFM.rrb.pr = 0;
} else // pred_form
    CFM.rrb.pr = 0;
```

**Interruptions:**

Illegal Operation fault
**cmp — Compare**

**Format:**

- \((qp)\) cmp.crel.ctype \(p_1, p_2 = r_2, r_3\)  \(\text{register\_form}\)  \(A6\)
- \((qp)\) cmp.crel.ctype \(p_1, p_2 = \text{imm8}, r_3\)  \(\text{imm8\_form}\)  \(A8\)
- \((qp)\) cmp.crel.ctype \(p_1, p_2 = r_0, r_3\)  \(\text{parallel\_inequality\_form}\)  \(A7\)
- \((qp)\) cmp.crel.ctype \(p_1, p_2 = r_3, r_0\)  \(\text{pseudo-op}\)

**Description:**

The two source operands are compared for one of ten relations specified by `crel`. This produces a boolean result which is 1 if the comparison condition is true, and 0 otherwise. This result is written to the two predicate register destinations, \(p_1\) and \(p_2\). The way the result is written to the destinations is determined by the compare type specified by `ctype`.

The compare types describe how the predicate targets are updated based on the result of the comparison. The normal type simply writes the compare result to one target, and the complement to the other. The parallel types update the targets only for a particular comparison result. This allows multiple simultaneous OR-type or multiple simultaneous AND-type compares to target the same predicate register.

The `unc` type is special in that it first initializes both predicate targets to 0, independent of the qualifying predicate. It then operates the same as the normal type. The behavior of the compare types is described in Table 2-15. A blank entry indicates the predicate target is left unchanged.

**Table 2-15. Comparison Types**

<table>
<thead>
<tr>
<th><code>ctype</code></th>
<th>pseudo-op of</th>
<th>(\text{PR}{qp}==0)</th>
<th>(\text{PR}{qp}==1)</th>
<th>(\text{PR}{qp}==0), No Source NaTs</th>
<th>(\text{PR}{qp}==1), No Source NaTs</th>
<th>One or More Source NaTs</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td></td>
<td>(\text{PR}{p_1}) (\text{PR}{p_2})</td>
<td>(\text{PR}{p_1}) (\text{PR}{p_2})</td>
<td>(\text{PR}{p_1}) (\text{PR}{p_2})</td>
<td>(\text{PR}{p_1}) (\text{PR}{p_2})</td>
<td>(\text{PR}{p_1}) (\text{PR}{p_2})</td>
</tr>
<tr>
<td>unc</td>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>or</td>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>and</td>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>or.andcm</td>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>orcm</td>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>andcm</td>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>or.cm</td>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>or.cm</td>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
<tr>
<td>and.orcm</td>
<td></td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
<td>00</td>
</tr>
</tbody>
</table>

In the \(\text{register\_form}\) the first operand is GR \(r_2\); in the \(\text{imm8\_form}\) the first operand is taken from the sign-extended \(\text{imm8}\) encoding field; and in the \(\text{parallel\_inequality\_form}\) the first operand must be GR 0. The \(\text{parallel\_inequality\_form}\) is only used when the compare type is one of the parallel types, and the relation is an inequality (\(>,\geq,\leq,\text{or}\) \(\text{or}\)). See below.

If the two predicate register destinations are the same (\(p_1\) and \(p_2\) specify the same predicate register), the instruction will take an Illegal Operation fault, if the qualifying predicate is 1, or if the compare type is unc.

Of the ten relations, not all are directly implemented in hardware. Some are actually pseudo-ops. For these, the assembler simply switches the source operand specifiers and/or switches the predicate target specifiers and uses an implemented relation. For some of the pseudo-op compares in the \(\text{imm8\_form}\), the assembler subtracts 1 from the immediate value, making the allowed immediate range slightly different. Of the six parallel compare types, three of the types are actually pseudo-ops. The assembler simply uses the negative relation with an implemented type. The implemented relations and how the pseudo-ops map onto them are shown in Table 2-16 (for normal and `unc` type compares), and Table 2-17 (for parallel type compares).
The parallel compare types can be used only with a restricted set of relations and operands. They can be used with equal and not-equal comparisons between two registers or between a register and an immediate, or they can be used with inequality comparisons between a register and GR 0. Unsigned relations are not provided, since they are not of much use when one of the operands is zero. For the parallel inequality comparisons, hardware only directly implements the ones where the first operand (GR \( r_2 \)) is GR 0. Comparisons where the second operand is GR 0 are pseudo-ops for which the assembler switches the register specifiers and uses the opposite relation.

### Table 2-16. 64-bit Comparison Relations for Normal and unc Compares

<table>
<thead>
<tr>
<th>( \text{crel} )</th>
<th>Compare Relation ((a \ rel \ b))</th>
<th>Register Form is a Pseudo-op of</th>
<th>Immediate Form is a Pseudo-op of</th>
<th>Immediate Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>eq</td>
<td>( a = b )</td>
<td>eq ( p_1 \leftrightarrow p_2 )</td>
<td>eq ( p_1 \leftrightarrow p_2 )</td>
<td>-128 .. 127</td>
</tr>
<tr>
<td></td>
<td>( a = b )</td>
<td></td>
<td></td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>lt</td>
<td>( a &lt; b )</td>
<td>signed</td>
<td></td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>le</td>
<td>( a \leq b )</td>
<td>( \text{lt} ) a \leftrightarrow b</td>
<td>( \text{lt} ) a \leftrightarrow b</td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>gt</td>
<td>( a &gt; b )</td>
<td>( \text{lt} ) a \leftrightarrow b</td>
<td>( \text{lt} ) a \leftrightarrow b</td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>ge</td>
<td>( a \geq b )</td>
<td>( \text{lt} ) ( p_1 \leftrightarrow p_2 )</td>
<td>( \text{lt} ) ( p_1 \leftrightarrow p_2 )</td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>itu</td>
<td>( a &lt; b )</td>
<td>unsigned</td>
<td>( \text{ltu} ) ( p_1 \leftrightarrow p_2 )</td>
<td>0 .. 127, 2^{64}-128 .. 2^{64}</td>
</tr>
<tr>
<td>leu</td>
<td>( a \leq b )</td>
<td>( \text{ltu} ) a \leftrightarrow b</td>
<td>( \text{ltu} ) a \leftrightarrow b</td>
<td>1 .. 128, 2^{64}-128 .. 2^{64}</td>
</tr>
<tr>
<td>glu</td>
<td>( a &gt; b )</td>
<td>( \text{ltu} ) a \leftrightarrow b</td>
<td>( \text{ltu} ) a \leftrightarrow b</td>
<td>1 .. 128, 2^{64}-128 .. 2^{64}</td>
</tr>
<tr>
<td>geu</td>
<td>( a \geq b )</td>
<td>( \text{ltu} ) ( p_1 \leftrightarrow p_2 )</td>
<td>( \text{ltu} ) ( p_1 \leftrightarrow p_2 )</td>
<td>0 .. 127, 2^{64}-128 .. 2^{64}</td>
</tr>
</tbody>
</table>

### Table 2-17. 64-bit Comparison Relations for Parallel Compares

<table>
<thead>
<tr>
<th>( \text{crel} )</th>
<th>Compare Relation ((a \ rel \ b))</th>
<th>Register Form is a</th>
<th>Immediate Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>eq</td>
<td>( a = b )</td>
<td></td>
<td>-128 .. 127</td>
</tr>
<tr>
<td></td>
<td>( a = b )</td>
<td></td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>lt</td>
<td>( 0 &lt; b )</td>
<td>signed</td>
<td>no immediate forms</td>
</tr>
<tr>
<td>lt</td>
<td>( a &lt; 0 )</td>
<td>( \text{gt} ) a \leftrightarrow b</td>
<td></td>
</tr>
<tr>
<td>le</td>
<td>( 0 \leq b )</td>
<td>( \text{ge} ) a \leftrightarrow b</td>
<td></td>
</tr>
<tr>
<td>gt</td>
<td>( 0 &gt; b )</td>
<td>( \text{lt} ) a \leftrightarrow b</td>
<td></td>
</tr>
<tr>
<td>ge</td>
<td>( 0 \geq b )</td>
<td>( \text{le} ) a \leftrightarrow b</td>
<td></td>
</tr>
<tr>
<td>ge</td>
<td>( a \geq 0 )</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Operation: if (PR[qp]) {
    if (p1 == p2)
        illegal_operation_fault();
    tmp_nat = (register_form ? GR[r2].nat : 0) || GR[r3].nat;
    if (register_form)
        tmp_src = GR[r3];
    else if (imm8_form)
        tmp_src = sign_ext(imm8, 8);
    else // parallel_inequality_form
        tmp_src = 0;
    if (crel == 'eq') tmp_rel = tmp_src == GR[r3];
    else if (crel == 'ne') tmp_rel = tmp_src != GR[r3];
    else if (crel == 'lt') tmp_rel = lesser_signed(tmp_src, GR[r3]);
    else if (crel == 'le') tmp_rel = lesser_equal_signed(tmp_src, GR[r3]);
    else if (crel == 'gt') tmp_rel = greater_signed(tmp_src, GR[r3]);
    else if (crel == 'ge') tmp_rel = greater_equal_signed(tmp_src, GR[r3]);
    else if (crel == 'ltu') tmp_rel = lesser(tmp_src, GR[r3]);
    else if (crel == 'leu') tmp_rel = lesser_equal(tmp_src, GR[r3]);
    else if (crel == 'gtu') tmp_rel = greater(tmp_src, GR[r3]);
    else tmp_rel = greater_equal(tmp_src, GR[r3]);
    switch (ctype) {
        case 'and': // and-type compare
            break;
        case 'or': // or-type compare
            break;
        case 'or.andcm': // or.andcm-type compare
            break;
        case 'unc': // unc-type compare
            break;
        default: // normal compare
            if (tmp_nat) {
                PR[p1] = 0;
                PR[p2] = 0;
            } else {
                PR[p1] = tmp_rel;
                PR[p2] = !tmp_rel;
            }
            break;
    }
    if (ctype == 'unc') {
        if (p1 == p2)
            illegal_operation_fault();
        PR[p1] = 0;
        PR[p2] = 0;
    }
}

Interruptions: Illegal Operation fault
cmp4 — Compare 4 Bytes

Format:  

\[(\text{qp}) \text{cmp4.crel.type} p_1, p_2 = r_2, r_3\]  
\[(\text{qp}) \text{cmp4.crel.type} p_1, p_2 = \text{imm}_8, r_3\]  
\[(\text{qp}) \text{cmp4.crel.type} p_1, p_2 = \text{r}_0, r_3\]  
\[(\text{qp}) \text{cmp4.crel.type} p_1, p_2 = r_3, \text{r}_0\]

Description:  
The least significant 32 bits from each of two source operands are compared for one of ten relations specified by \text{crel}. This produces a boolean result which is 1 if the comparison condition is true, and 0 otherwise. This result is written to the two predicate register destinations, \(p_1\) and \(p_2\). The way the result is written to the destinations is determined by the compare type specified by \text{ctype}. See the Compare instruction and Table 2-15 on page 3:34.

In the register_form the first operand is GR \(r_2\); in the imm8_form the first operand is taken from the sign-extended \text{imm}_8 encoding field; and in the parallel_inequality_form the first operand must be GR 0. The parallel_inequality_form is only used when the compare type is one of the parallel types, and the relation is an inequality (\(>, >=, <, <=\)). See the Compare instruction and Table 2-17 on page 3:35.

If the two predicate register destinations are the same (\(p_1\) and \(p_2\) specify the same predicate register), the instruction will take an Illegal Operation fault, if the qualifying predicate is 1, or if the compare type is unc.

Of the ten relations, not all are directly implemented in hardware. Some are actually pseudo-ops. See the Compare instruction and Table 2-16 and Table 2-17 on page 3:35. The range for immediates is given below.

Table 2-18. Immediate Range for 32-bit Compares

<table>
<thead>
<tr>
<th>\text{crel}</th>
<th>\text{Compare Relation} ((a \text{ rel } b))</th>
<th>Immediate Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>eq</td>
<td>(a == b)</td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>ne</td>
<td>(a != b)</td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>lt</td>
<td>(a &lt; b)</td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>le</td>
<td>(a &lt;= b)</td>
<td>-127 .. 128</td>
</tr>
<tr>
<td>gt</td>
<td>(a &gt; b)</td>
<td>-127 .. 128</td>
</tr>
<tr>
<td>ge</td>
<td>(a &gt;= b)</td>
<td>-128 .. 127</td>
</tr>
<tr>
<td>ltu</td>
<td>(a &lt; b)</td>
<td>0 .. 127, (2^{32} - 128 \ldots 2^{32} - 1)</td>
</tr>
<tr>
<td>leu</td>
<td>(a &lt;= b)</td>
<td>1 .. 128, (2^{32} - 127 \ldots 2^{32} - 1)</td>
</tr>
<tr>
<td>gtu</td>
<td>(a &gt; b)</td>
<td>1 .. 128, (2^{32} - 127 \ldots 2^{32} - 1)</td>
</tr>
<tr>
<td>geu</td>
<td>(a &gt;= b)</td>
<td>0 .. 127, (2^{32} - 128 \ldots 2^{32} - 1)</td>
</tr>
</tbody>
</table>
Operation:

```c
if (PR[qp]) {
    if (p1 == p2)
        illegal_operation_fault();

    tmp_nat = (register_form ? GR[r2].nat : 0) || GR[r2].nat;

    if (register_form)
        tmp_src = GR[r2];
    else if (imm8_form)
        tmp_src = sign_ext(imm, 8);
    else // parallel_inequality_form
        tmp_src = 0;

    if (crel == 'eq')
        tmp_rel = sign_ext(tmp_src, 32);
    else if (crel == 'ne')
        tmp_rel = sign_ext(tmp_src, 32);
    else if (crel == 'lt')
        tmp_rel = lesser_signed(tmp_src, 32);
    else if (crel == 'le')
        tmp_rel = lesser_equal_signed(tmp_src, 32);
    else if (crel == 'gt')
        tmp_rel = greater_signed(tmp_src, 32);
    else if (crel == 'ge')
        tmp_rel = greater_equal_signed(tmp_src, 32);
    else if (crel == 'ltu')
        tmp_rel = lesser(Zero(tmp_src, 32));
    else if (crel == 'leu')
        tmp_rel = lesser_equal(Zero(tmp_src, 32));
    else if (crel == 'gtu')
        tmp_rel = greater(Zero(tmp_src, 32));
    else // 'geu'
        tmp_rel = greater_equal(Zero(tmp_src, 32));

    switch (ctype) {
        case 'and':  // and-type compare
            if (tmp_nat || !tmp_rel) {
                PR[p1] = 0;
                PR[p2] = 0;
            }
            break;
        case 'or':   // or-type compare
            if (!tmp_nat && tmp_rel) {
                PR[p1] = 1;
                PR[p2] = 1;
            }
            break;
        case 'or.andcm':  // or.andcm-type compare
            if (!tmp_nat && tmp_rel) {
                PR[p1] = 1;
                PR[p2] = 0;
            }
            break;
        case 'unc':  // unc-type compare
            default:    // normal compare
            if (tmp_nat) {
```

PR[p1] = 0;
PR[p2] = 0;
} else {
    PR[p1] = tmp_rel;
    PR[p2] = !tmp_rel;
    break;
}
} else {
    if (ctype == 'unc') {
        if (p1 == p2)
            illegal_operation_fault();
        PR[p1] = 0;
        PR[p2] = 0;
    }
}

**Interruptions:** Illegal Operation fault
cmpxchg — Compare and Exchange

Format:

(qp) cmpxchg|sz| sem.ldhint r1 = [r3], r2, ar.ccv

(qp) cmp8xchg16|sz| sem.ldhint r1 = [r3], r2, ar.csd, ar.ccv

Description:

A value consisting of sz bytes (8 bytes for cmp8xchg16) is read from memory starting at the address specified by the value in GR r3. The value is zero extended and compared with the contents of the cmpxchg Compare Value application register (AR[CCV]). If the two are equal, then the least significant sz bytes of the value in GR r2 are written to memory starting at the address specified by the value in GR r3. For cmp8xchg16, if the two are equal, then 8-bytes from GR r2 are stored at the specified address ignoring bit 3 (GR r3 & ~0x4), and 8 bytes from the Compare and Store Data application register (AR[CSD]) are stored at that address + 8 ((GR r3 & ~0x4) + 8). The zero-extended value read from memory is placed in GR r1 and the NaT bit corresponding to GR r1 is cleared.

The values of the sz completer are given in Table 2-19. The sem completer specifies the type of semaphore operation. These operations are described in Table 2-20. See Section 4.4.7, “Sequentiality Attribute and Ordering” on page 2:69 for details on memory ordering.

Table 2-19. Memory Compare and Exchange Size

<table>
<thead>
<tr>
<th>sz Completer</th>
<th>Bytes Accessed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
</tr>
</tbody>
</table>

Table 2-20. Compare and Exchange Semaphore Types

<table>
<thead>
<tr>
<th>sem Completer</th>
<th>Ordering Semantics</th>
<th>Semaphore Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>acq</td>
<td>Acquire</td>
<td>The memory read/write is made visible prior to all subsequent data memory accesses.</td>
</tr>
<tr>
<td>rel</td>
<td>Release</td>
<td>The memory read/write is made visible after all previous data memory accesses.</td>
</tr>
</tbody>
</table>

If the address specified by the value in GR r3 is not naturally aligned to the size of the value being accessed in memory, an Unaligned Data Reference fault is taken independent of the state of the User Mask alignment checking bit, UM.ac (PSR.ac in the Processor Status Register). For the cmp8xchg16 instruction, the address specified must be 8-byte aligned.

The memory read and write are guaranteed to be atomic. For the cmp8xchg16 instruction, the 8-byte memory read and the 16-byte memory write are guaranteed to be atomic.

Both read and write access privileges for the referenced page are required. The write access privilege check is performed whether or not the memory write is performed.

This instruction is only supported to cacheable pages with write-back write policy. Accesses to NaTPages cause a Data NaT Page Consumption fault. Accesses to pages with other memory attributes cause an Unsupported Data Reference fault.

The value of the ldhint completer specifies the locality of the memory access. The values of the ldhint completer are given in Table 2-34 on page 3:132. Locality hints do not affect program functionality and may be ignored by the implementation. See Section 4.4.6, “Memory Hierarchy Control and Consistency” on page 1:60 for details.
Operation:

```c
if (PR[qp]) {
    check_target_register(r1);
    if (GR[r2].nat || GR[r3].nat)
        register_nat_consumption_fault(SEMAPHORE);
    if (sixteen_byte_form)
        sz = 8;
    paddr = tlb_translate(GR[r3], sz, SEMAPHORE, PSR.cpl, &mattr,
                             &tmp_unused);
    if (!ma_supports_semaphores(mattr))
        unsupported_data_reference_fault(SEMAPHORE, GR[r3]);

    if (sixteen_byte_form) {
        if (sem == 'acq')
            val = mem_xchg16_cond(AR[CCV], GR[r2], AR[CSD], paddr, UM.be,
                                  mattr, ACQUIRE, ldhint);
        else // 'rel'
            val = mem_xchg16_cond(AR[CCV], GR[r2], AR[CSD], paddr, UM.be,
                                  mattr, RELEASE, ldhint);
    } else {
        if (sem == 'acq')
            val = mem_xchg_cond(AR[CCV], GR[r2], paddr, sz, UM.be, mattr,
                                ACQUIRE, ldhint);
        else // 'rel'
            val = mem_xchg_cond(AR[CCV], GR[r2], paddr, sz, UM.be, mattr,
                                RELEASE, ldhint);
        val = zero_ext(val, sz * 8);
    }
    if (AR[CCV] == val)
        alat_inval_multiple_entries(paddr, sz);
    GR[r1] = val;
    GR[r1].nat = 0;
}
```

Interruptions:

- Illegal Operation fault
- Register NaT Consumption fault
- Unimplemented Data Address fault
- Data Nested TLB fault
- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault
- Data NaT Page Consumption fault
- Data Key Miss fault
- Data Key Permission fault
- Data Access Rights fault
- Data Dirty Bit fault
- Data Access Bit fault
- Data Debug fault
- Unaligned Data Reference fault
- Unsupported Data Reference fault
cover — Cover Stack Frame

Format:  cover

Description:  A new stack frame of zero size is allocated which does not include any registers from the previous frame (as though all output registers in the previous frame had been locals). The register rename base registers are reset. If interruption collection is disabled (PSR.ic is zero), then the old value of the Current Frame Marker (CFM) is copied to the Interruption Function State register (IFS), and IFS.v is set to one.

A cover instruction must be the last instruction in an instruction group. Otherwise, an Illegal Operation fault is taken.

This instruction cannot be predicated.

Operation:

```c
if (!followed_by_stop())
    illegal_operation_fault();

alat_frame_update(CFM.sof, 0);
rsr_preserve_frame(CFM.sof);
if (PSR.ic == 0) {
    CR[IFS].ifm = CFM;
    CR[IFS].v = 1;
}

CFM.sof = 0;
CFM.sol = 0;
CFM.sor = 0;
CFM.rrb.gr = 0;
CFM.rrb.fr = 0;
CFM.rrb.pr = 0;
```

Interruptions:  Illegal Operation fault
**czx — Compute Zero Index**

**Format:**

\[
\begin{align*}
(qp) & \text{czx1.l } r_1 = r_3 \\
(qp) & \text{czx1.r } r_1 = r_3 \\
(qp) & \text{czx2.l } r_1 = r_3 \\
(qp) & \text{czx2.r } r_1 = r_3
\end{align*}
\]

**one_byte_form, left_form** & 129

\[
\begin{align*}
(qp) & \text{czx1.l } r_1 = r_3 \\
(qp) & \text{czx1.r } r_1 = r_3 \\
(qp) & \text{czx2.l } r_1 = r_3 \\
(qp) & \text{czx2.r } r_1 = r_3
\end{align*}
\]

**one_byte_form, right_form** & 129

\[
\begin{align*}
(qp) & \text{czx2.l } r_1 = r_3 \\
(qp) & \text{czx2.r } r_1 = r_3
\end{align*}
\]

**two_byte_form, left_form** & 129

**two_byte_form, right_form** & 129

**Description:**

GR \( r_3 \) is scanned for a zero element. The element is either an 8-bit aligned byte (one_byte_form) or a 16-bit aligned pair of bytes (two_byte_form). The index of the first zero element is placed in GR \( r_1 \). If there are no zero elements in GR \( r_3 \), a default value is placed in GR \( r_1 \). Table 2-21 gives the possible result values. In the left_form, the source is scanned from most significant element to least significant element, and in the right_form it is scanned from least significant element to most significant element.

**Table 2-21. Result Ranges for czx**

<table>
<thead>
<tr>
<th>Size</th>
<th>Element Width</th>
<th>Range of Result if Zero Element Found</th>
<th>Default Result if No Zero Element Found</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>8 bit</td>
<td>0-7</td>
<td>8</td>
</tr>
<tr>
<td>2</td>
<td>16 bit</td>
<td>0-3</td>
<td>4</td>
</tr>
</tbody>
</table>

**Operation:**

```c
if (PR[qp]) {
  check_target_register(r1);
  if (one_byte_form) {
    // scan from most significant down
    if ((GR[r3] & 0xff00000000000000) == 0) GR[r1] = 0;
    else if ((GR[r3] & 0x00ff000000000000) == 0) GR[r1] = 1;
    else if ((GR[r3] & 0x0000ff0000000000) == 0) GR[r1] = 2;
    else if ((GR[r3] & 0x000000ff00000000) == 0) GR[r1] = 3;
    else if ((GR[r3] & 0x00000000ff000000) == 0) GR[r1] = 4;
    else if ((GR[r3] & 0x0000000000ff0000) == 0) GR[r1] = 5;
    else if ((GR[r3] & 0x000000000000ff00) == 0) GR[r1] = 6;
    else if ((GR[r3] & 0x00000000000000ff) == 0) GR[r1] = 7;
    else GR[r1] = 8;
  } else { // right_form  scan from least significant up
    if ((GR[r3] & 0x00ff000000000000) == 0) GR[r1] = 0;
    else if ((GR[r3] & 0x0000ff0000000000) == 0) GR[r1] = 1;
    else if ((GR[r3] & 0x000000ff00000000) == 0) GR[r1] = 2;
    else if ((GR[r3] & 0x00000000ff000000) == 0) GR[r1] = 3;
    else if ((GR[r3] & 0x0000000000ff0000) == 0) GR[r1] = 4;
    else if ((GR[r3] & 0x000000000000ff00) == 0) GR[r1] = 5;
    else if ((GR[r3] & 0x00000000000000ff) == 0) GR[r1] = 6;
    else if ((GR[r3] & 0x00ff000000000000) == 0) GR[r1] = 7;
    else GR[r1] = 8;
  }
} else { // two_byte_form
  // scan from most significant down
  if ((GR[r3] & 0xffff000000000000) == 0) GR[r1] = 0;
  else if ((GR[r3] & 0x0000ffff00000000) == 0) GR[r1] = 1;
  else if ((GR[r3] & 0x00000000ffff0000) == 0) GR[r1] = 2;
  else if ((GR[r3] & 0x000000000000ffff) == 0) GR[r1] = 3;
  else GR[r1] = 4;
} else { // right_form  scan from least significant up
  if ((GR[r3] & 0x0000ffff00000000) == 0) GR[r1] = 0;
  else if ((GR[r3] & 0x00000000ffff0000) == 0) GR[r1] = 1;
  else if ((GR[r3] & 0x000000000000ffff) == 0) GR[r1] = 2;
  else if ((GR[r3] & 0x00000000000000ff) == 0) GR[r1] = 3;
  else GR[r1] = 4;
```

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GR[r_3].nat = GR[r_3].nat;

**Interruptions:** Illegal Operation fault
dep — Deposit

Format:

- (q) dep \( r_1 = r_2, r_3, pos_6, len_4 \)  
  merge_form, register_form  I15
- (q) dep \( r_1 = imm_1, r_3, pos_6, len_6 \)  
  merge_form, imm_form  I14
- (q) dep.z \( r_1 = r_2, pos_6, len_6 \)  
  zero_form, register_form  I12
- (q) dep.z \( r_1 = imm_0, pos_6, len_6 \)  
  zero_form, imm_form  I13

Description: In the merge_form, a right justified bit field taken from the first source operand is deposited into the value in GR \( r_3 \) at an arbitrary bit position and the result is placed in GR \( r_1 \). In the register_form the first source operand is GR \( r_2 \); and in the imm_form it is the sign-extended value specified by \( imm_1 \) (either all ones or all zeroes). The deposited bit field begins at the bit position specified by the \( pos_6 \) immediate and extends to the left (towards the most significant bit) a number of bits specified by the \( len \) immediate. Note that \( len \) has a range of 1-16 in the register_form and 1-64 in the imm_form. The \( pos_6 \) immediate has a range of 0 to 63.

In the zero_form, a right justified bit field taken from either the value in GR \( r_2 \) (in the register_form) or the sign-extended value in \( imm_8 \) (in the imm_form) is deposited into GR \( r_1 \) and all other bits in GR \( r_1 \) are cleared to zero. The deposited bit field begins at the bit position specified by the \( pos_6 \) immediate and extends to the left (towards the most significant bit) a number of bits specified by the \( len \) immediate. The \( len \) immediate has a range of 1-64 and the \( pos_6 \) immediate has a range of 0 to 63.

In the event that the deposited bit field extends beyond bit 63 of the target, i.e., \( len + pos_6 > 64 \), the most significant \( len + pos_6 - 64 \) bits of the deposited bit field are truncated. The \( len \) immediate is encoded as \( len \) minus 1 in the instruction.

The operation of \( \text{dep} r_1 = r_2, r_3, 36, 16 \) is illustrated in Figure 2-5.

**Figure 2-5. Deposit Example (merge_form)**

![Deposit Example (merge_form)](image)

The operation of \( \text{dep.z} r_1 = r_2, 36, 16 \) is illustrated in Figure 2-6.

**Figure 2-6. Deposit Example (zero_form)**

![Deposit Example (zero_form)](image)
Operation:

```c
if (PR[qp]) {
    check_target_register(r1);
    if (imm_form) {
        tmp_src = (merge_form ? sign_ext(imm1, 1) : sign_ext(imm8, 8));
        tmp_nat = merge_form ? GR[r3].nat : 0;
        tmp_len = len6;
    } else { // register_form
        tmp_src = GR[r2];
        tmp_nat = (merge_form ? GR[r3].nat : 0) || GR[r2].nat;
        tmp_len = merge_form ? len4 : len6;
    }
    if ((pos6 + tmp_len u> 64)
        tmp_len = 64 - pos6;
    if (merge_form)
        GR[r2] = GR[r3];
    else // zero_form
        GR[r2] = 0;
    GR[r2]{{pos6 + tmp_len - 1}:pos6} = tmp_src{{tmp_len - 1}:0};
    GR[r2].nat = tmp_nat;
}
```

Interruptions: Illegal Operation fault
epc — Enter Privileged Code

**Format:** epc

**Description:** This instruction increases the privilege level. The new privilege level is given by the TLB entry for the page containing this instruction. This instruction can be used to implement calls to higher-privileged routines without the overhead of an interruption.

Before increasing the privilege level, a check is performed. The PFS.ppl (previous privilege level) is checked to ensure that it is not more privileged than the current privilege level. If this check fails, the instruction takes an Illegal Operation fault.

If the check succeeds, then the privilege is increased as follows:

- If instruction address translation is enabled and the page containing the epc instruction has execute-only page access rights and the privilege level assigned to the page is higher than (numerically less than) the current privilege level, then the current privilege level is set to the privilege level field in the translation for the page containing the epc instruction. This instruction can promote but cannot demote, and the new privilege comes from the TLB entry.

  If instruction address translation is disabled, then the current privilege level is set to 0 (most privileged).

  Instructions after the epc in the same instruction group may be executed at the old privilege level or the new, higher privilege level. Instructions in subsequent instruction groups will be executed at the new, higher privilege level.

- If the page containing the epc instruction has any other access rights besides execute-only, or if the privilege level assigned to the page is lower or equal to (numerically greater than or equal to) the current privilege level, then no action is taken (the current privilege level is unchanged).

Note that the ITLB is actually only read once, at instruction fetch. Information from the access rights and privilege level fields from the translation is then used in executing this instruction.

This instruction cannot be predicated.

**Operation:**

```c
if (AR[PFS].ppl u< PSR.cpl)
    illegal_operation_fault();

if (PSR.it)
    PSR.cpl = tlb_enterprivileged_code();
else
    PSR.cpl = 0;
```

**Interruptions:** Illegal Operation fault
extr — Extract

Format: 

(qp) extr $r_1 = r_3, pos_6, len_6$

(qp) extr.u $r_1 = r_3, pos_6, len_6$

Description: A field is extracted from GR $r_3$, either zero extended or sign extended, and placed right-justified in GR $r_1$. The field begins at the bit position given by the second operand and extends $len_6$ bits to the left. The bit position where the field begins is specified by the $pos_6$ immediate. The extracted field is sign extended in the signed_form or zero extended in the unsigned_form. The sign is taken from the most significant bit of the extracted field. If the specified field extends beyond the most significant bit of GR $r_3$, the sign is taken from the most significant bit of GR $r_3$. The immediate value $len_6$ can be any number in the range 1 to 64, and is encoded as $len_6 - 1$ in the instruction. The immediate value $pos_6$ can be any value in the range 0 to 63.

The operation of $extr r_1 = r_3, 7, 50$ is illustrated in Figure 2-7.

Figure 2-7. Extract Example

![Extract Example Diagram]

Operation:

if (PR[qp]) {
    check_target_register($r_1$);

    tmp_len = len_6;

    if ($pos_6 + tmp_len > 64$)
        tmp_len = 64 - $pos_6$;

    if (unsigned_form)
        GR[$r_1$] = zero_ext(shift_right_unsigned(GR[$r_3$], $pos_6$), tmp_len);
    else // signed_form
        GR[$r_1$] = sign_ext(shift_right_unsigned(GR[$r_3$], $pos_6$), tmp_len);

    GR[$r_1$].nat = GR[$r_3$].nat;
}

Interruptions: Illegal Operation fault
fabs — Floating-point Absolute Value

Format: \( (qp) \text{ fabs } f_1 = f_3 \quad \text{pseudo-op of: } (qp) \text{ fmerge.s } f_1 = f_0, f_3 \)

Description: The absolute value of the value in FR\( f_3 \) is computed and placed in FR\( f_1 \).
If FR\( f_3 \) is a NaTVal, FR\( f_1 \) is set to NaTVal instead of the computed result.

**fadd — Floating-point Add**

**Format:**

\[ \text{\texttt{fadd.pcsf_f1 = f3, f2}} \]

pseudo-op of: \( \text{\texttt{fma.pcsf_f1 = f3, f1, f2}} \)

**Description:**

FR \( f_j \) and FR \( f_k \) are added (computed to infinite precision), rounded to the precision indicated by \( pc \) (and possibly FPSR.\( sf.pc \) and FPSR.\( sf.wre \)) using the rounding mode specified by FPSR.\( sf.rc \), and placed in FR \( f_j \). If either FR \( f_3 \) or FR \( f_2 \) is a NaTVal, FR \( f_j \) is set to NaTVal instead of the computed result.

The mnemonic values for the opcode’s \( pc \) are given in Table 2-22. The mnemonic values for \( sf \) are given in Table 2-23. For the encodings and interpretation of the status field’s \( pc, wre, \) and \( rc \), refer to Table 5-6 and Table 5-5 on page 1:80.

**Table 2-22. Specified \( pc \) Mnemonic Values**

<table>
<thead>
<tr>
<th>( pc ) Mnemonic</th>
<th>Precision Specified</th>
</tr>
</thead>
<tbody>
<tr>
<td>.s</td>
<td>single</td>
</tr>
<tr>
<td>.d</td>
<td>double</td>
</tr>
<tr>
<td>none</td>
<td>dynamic</td>
</tr>
<tr>
<td></td>
<td>(i.e. use pc value in status field)</td>
</tr>
</tbody>
</table>

**Table 2-23. \( sf \) Mnemonic Values**

<table>
<thead>
<tr>
<th>( sf ) Mnemonic</th>
<th>Status Field Accessed</th>
</tr>
</thead>
<tbody>
<tr>
<td>.s0 or none</td>
<td>sf0</td>
</tr>
<tr>
<td>.s1</td>
<td>sf1</td>
</tr>
<tr>
<td>.s2</td>
<td>sf2</td>
</tr>
<tr>
<td>.s3</td>
<td>sf3</td>
</tr>
</tbody>
</table>

**Operation:** See “fma — Floating-point Multiply Add” on page 3:70.
**famax — Floating-point Absolute Maximum**

**Format:**  
\[(qp) \text{famx.sf} f_1 = f_2, f_3\]

**Description:**  
The operand with the larger absolute value is placed in FR\(f_1\). If the magnitude of FR\(f_2\) equals the magnitude of FR\(f_3\), FR\(f_1\) gets FR\(f_3\).

- If either FR\(f_2\) or FR\(f_3\) is a NaN, FR\(f_1\) gets FR\(f_3\).
- If either FR\(f_2\) or FR\(f_3\) is a NaTVal, FR\(f_1\) is set to NaTVal instead of the computed result.

This operation does not propagate NaNs the same way as other arithmetic floating-point instructions. The Invalid Operation is signaled in the same manner as the \(f\text{cmp}\lt\) operation.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

**Operation:**  
```c
if (FR[qp]) {
    fp_check_target_register(f_1);
    if (tmp_isrcode = fp_reg_disabled(f_1, f_2, f_3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (fp_is_natval(FR[f_2]) || fp_is_natval(FR[f_3])) {
        FR[f_1] = NATVAL;
    } else {
        fminmax_exception_fault_check(f_2, f_3, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));
        tmp_right = fp_reg_read(FR[f_2]);
        tmp_left = fp_reg_read(FR[f_3]);
        tmp_right.sign = FP_SIGN_POSITIVE;
        tmp_left.sign = FP_SIGN_POSITIVE;
        tmp_right_res = fp_less_than(tmp_left, tmp_right);
        fp_update_fpsr(sf, tmp_fp_env);
    }
    fp_update_psr(f_1);
} 
```

**FP Exceptions:** Invalid Operation (V)  
Denormal/Unnormal Operand (D)  
Software Assist (SWA) fault

**Interruptions:** Illegal Operation fault  
Floating-point Exception fault  
Disabled Floating-point Register fault
famin — Floating-point Absolute Minimum

Format: \((qp)\) famin.sf \(f_1 = f_2, f_3\)

Description: The operand with the smaller absolute value is placed in \(f_{1}\). If the magnitude of \(f_{2}\) equals the magnitude of \(f_{3}\), \(f_{1}\) gets \(f_{3}\).

If either \(f_{2}\) or \(f_{3}\) is a NaN, \(f_{1}\) gets \(f_{3}\).

If either \(f_{2}\) or \(f_{3}\) is a NaTVal, \(f_{1}\) is set to NaTVal instead of the computed result.

This operation does not propagate NaNs the same way as other arithmetic floating-point instructions. The Invalid Operation is signaled in the same manner as the \(fcmp.lt\) operation.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

Operation:

if \((PR[qp])\) {
    fp_check_target_register\((f_{1})\);
    if (tmp_isrcode = fp_reg_disabled\((f_{1}, f_{2}, f_{3}, 0)\))
        disabled_fp_register_fault\(\text{tmp_isrcode, } 0\);}

if (fp_is_natval\((f_{2})\) || fp_is_natval\((f_{3})\)) {
    \(f_{1} = \text{NATVAL};\}
else {
    fminmax_exception_fault_check\(f_{2}, f_{3}, sf, \&\text{tmp_fp_env});
    if (fp_raise_fault\(\text{tmp_fp_env})
        fp_exception_fault\(fp_decode_fault\(\text{tmp_fp_env});\)
        tmp_left = fp_reg_read\(f_{2});
        tmp_right = fp_reg_read\(f_{3});
        \text{tmp_left.sign} = \text{FP\_SIGN\_POSITIVE};
        \text{tmp_right.sign} = \text{FP\_SIGN\_POSITIVE};
        \text{tmp_bool_res} = fp_less_than\(\text{tmp_left, tmp_right});
        \text{FR}\[f_{1}\] = \text{tmp_bool_res} ? \text{FR}\[f_{2}\] : \text{FR}\[f_{3}\];
        \text{fp_update_fpsr\(sf, \text{tmp_fp_env);\)
    }
    \text{fp_update_psr}\(f_{1});\}

FP Exceptions: Invalid Operation (V)

Denormal/Unnormal Operand (D)

Software Assist (SWA) fault

Interruptions: Illegal Operation fault

Floating-point Exception fault

Disabled Floating-point Register fault
**fand — Floating-point Logical And**

**Format:**

\[(qp) \text{ fand } f_1 = f_2, f_3\]

**Description:**

The bit-wise logical AND of the significand fields of \(FR_{f2}\) and \(FR_{f3}\) is computed. The resulting value is stored in the significand field of \(FR_{f1}\). The exponent field of \(FR_{f1}\) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of \(FR_{f1}\) is set to positive (0).

If either \(FR_{f2}\) or \(FR_{f3}\) is a NaTVal, \(FR_{f1}\) is set to NaTVal instead of the computed result.

**Operation:**

if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
    } else {
        FR[f1].significand = FR[f2].significand & FR[f3].significand;
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;
    }
    fp_update_psr(f1);
}

**FP Exceptions:** None

**Interruptions:** Illegal Operation fault Disabled Floating-point Register fault
fandcm — Floating-point And Complement

Format:  \((qp)\) fandcm \(f_1 = f_2, f_3\)

Description: The bit-wise logical AND of the significand field of FR \(f_2\) with the bit-wise complemented significand field of FR \(f_3\) is computed. The resulting value is stored in the significand field of FR \(f_1\). The exponent field of FR \(f_1\) is set to the biased exponent for \(2.063\) (0x1003E) and the sign field of FR \(f_1\) is set to positive (0).

If either FR \(f_2\) or FR \(f_2\) is a NaTVal, FR \(f_1\) is set to NaTVal instead of the computed result.

Operation:  
if (PR[qp]) { 
  fandcm_check_target_register(f1);
  if (tmp_isrcode = fandcm_reg_disabled(f1, f2, f3, 0))
    disabled_fandcm_register_fault(tmp_isrcode, 0);

  if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
    FR[f1] = NATVAL;
  } else {
    FR[f1].significand = FR[f2].significand & ~FR[f3].significand;
    FR[f1].exponent = FP_INTEGER_EXP;
    FR[f1].sign = FP_SIGN_POSITIVE;
  }
  fp_update_psr(f1);
}

FP Exceptions: None

Interruptions:  
Illegal Operation fault
Disabled Floating-point Register fault
**fc — Flush Cache**

**Format:**

\[(qp) \quad fc \ r_3\]

\[(qp) \quad fc.i \ r_3\]

**Description:**

In the invalidate_line form, the cache line associated with the address specified by the value of GR \( r_3 \) is invalidated from all levels of the processor cache hierarchy. The invalidation is broadcast throughout the coherence domain. If, at any level of the cache hierarchy, the line is inconsistent with memory it is written to memory before invalidation. The line size affected is at least 32-bytes (aligned on a 32-byte boundary). An implementation may flush a larger region.

In the instruction_cache_coherent form, the cache line specified by GR \( r_3 \) is flushed in an implementation-specific manner that ensures that the instruction caches are coherent with the data caches. The \( fc.i \) instruction is not required to invalidate the targeted cache line nor write the targeted cache line back to memory if it is inconsistent with memory, but may do so if this is required to make the instruction caches coherent with the data caches. The \( fc.i \) instruction is broadcast throughout the coherence domain if necessary to make all instruction caches coherent. The line size affected is at least 32-bytes (aligned on a 32-byte boundary). An implementation may flush a larger region.

When executed at privilege level 0, \( fc \) and \( fc.i \) perform no access rights or protection key checks. At other privilege levels, \( fc \) and \( fc.i \) perform access rights checks as if they were 1-byte reads, but do not perform any protection key checks (regardless of PSR.pk).

The memory attribute of the page containing the affected line has no effect on the behavior of these instructions. The \( fc \) instruction can be used to remove a range of addresses from the cache by first changing the memory attribute to non-cacheable and then flushing the range.

These instructions follow data dependency rules; they are ordered with respect to preceding and following memory references to the same line. \( fc \) and \( fc.i \) have data dependencies in the sense that any prior stores by this processor will be included in the flush operation. \( fc \) and \( fc.i \) are unordered operations, and are not affected by a memory fence (\( mf \)) instruction. These instructions are ordered with respect to the \( sync.i \) instruction.

**Operation:**

```plaintext
if (PR[qp]) {
    itype = NON_ACCESS|FC|READ;
    if (GR[r_3].nat)
        register_nat_consumption_fault(itype);
    tmp_paddr = tlb_translate_nonaccess(GR[r_3], itype);

    if (invalidate_line_form)
        mem_flush(tmp_paddr);
    else // instruction_cache_coherent_form
        make_icache_coherent(tmp_paddr);
}
```

**Interruptions:**

- Register NaT Consumption fault
- Unimplemented Data Address fault
- Data Nested TLB fault
- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault
- Data NaT Page Consumption fault
- Data Access Rights fault
fchkf — Floating-point Check Flags

Format: \((qp)\) fchkf.sf target25

Description: The flags in FPSR.sf.flags are compared with FPSR.s0.flags and FPSR.traps. If any flags set in FPSR.sf.flags correspond to FPSR.traps which are enabled, or if any flags set in FPSR.sf.flags are not set in FPSR.s0.flags, then a branch to target25 is taken.

The target25 operand, specifies a label to branch to. This is encoded in the instruction as a signed immediate displacement \((imm21)\) between the target bundle and the bundle containing this instruction \((imm21 = target25 – IP >> 4)\).

The branching behavior of this instruction can be optionally unimplemented. If the instruction would have branched, and the branching behavior is not implemented, then a Speculative Operation fault is taken and the value specified by \(imm21\) is zero-extended and placed in the Interruption Immediate control register (IIM). The fault handler emulates the branch by sign-extending the IIM value, adding it to IIP and returning.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

Operation:

```c
if (PR[qp]) {
    switch (sf) {
    case 's0':
        tmp_flags = AR[FPSR].sf0.flags;
        break;
    case 's1':
        tmp_flags = AR[FPSR].sf1.flags;
        break;
    case 's2':
        tmp_flags = AR[FPSR].sf2.flags;
        break;
    case 's3':
        tmp_flags = AR[FPSR].sf3.flags;
        break;
    }
    if ((tmp_flags & ~AR[FPSR].traps) || (tmp_flags & ~AR[FPSR].sf0.flags)) {
        if (check_branch_implemented(FCHKF)) {
            taken_branch = 1;
            IP = IP + sign_ext((imm21 << 4), 25);
            if ((PSR.it && unimplemented_virtual_address(IP)) || (!PSR.it && unimplemented_physical_address(IP)))
                unimplemented_instruction_address_trap(0, IP);
            if (PSR.tb)
                taken_branch_trap();
        } else
            speculation_fault(FCHKF, zero_ext(imm21, 21));
    }
}
```

FP Exceptions: None

Interruptions: Speculative Operation fault
Taken Branch trap
Unimplemented Instruction Address trap
**fclass — Floating-point Class**

**Format:**

\[(q) \text{fclass.fcrel.fctype} \quad p_1, p_2 = f_2, \text{fclass}_0\]

**Description:**

The contents of FR \(f_2\) are classified according to the \(\text{fclass}_0\) completer as shown in Table 2-25. This produces a boolean result based on whether the contents of FR \(f_2\) agrees with the floating-point number format specified by \(\text{fclass}_0\), as specified by the \(\text{fcrel}\) completer. This result is written to the two predicate register destinations, \(p_1\) and \(p_2\). The result written to the destinations is determined by the compare type specified by \(\text{fctype}\).

The allowed types are Normal (or none) and unc. See Table 2-26 on page 3:60. The assembly syntax allows the specification of membership or non-membership and the assembler swaps the target predicates to achieve the desired effect.

**Table 2-24. Floating-point Class Relations**

<table>
<thead>
<tr>
<th>(\text{fcrel})</th>
<th>Test Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>(m)</td>
<td>FR (f_2) agrees with the pattern specified by (\text{fclass}_0) (is a member)</td>
</tr>
<tr>
<td>(nm)</td>
<td>FR (f_2) does not agree with the pattern specified by (\text{fclass}_0) (is not a member)</td>
</tr>
</tbody>
</table>

A number agrees with the pattern specified by \(\text{fclass}_0\) if:

- the number is NaTVal and \(\text{fclass}_0\) \(\{8\}\) is 1, or
- the number is a quiet NaN and \(\text{fclass}_0\) \(\{7\}\) is 1, or
- the number is a signaling NaN and \(\text{fclass}_0\) \(\{6\}\) is 1, or
- the sign of the number agrees with the sign specified by one of the two low-order bits of \(\text{fclass}_0\), and the type of the number (disregarding the sign) agrees with the number-type specified by the next 4 bits of \(\text{fclass}_0\), as shown in Table 2-25.

**Note:** An \(\text{fclass}_0\) of 0x1FF is equivalent to testing for any supported operand. The class names used in Table 2-25 are defined in Table 5-2, “Floating-point Register Encodings” on page 1:77.

**Table 2-25. Floating-point Classes**

<table>
<thead>
<tr>
<th>(\text{fclass}_0)</th>
<th>Class</th>
<th>Mnemonic</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0100</td>
<td>NaTVal</td>
<td>@nat</td>
</tr>
<tr>
<td>0x080</td>
<td>Quiet NaN</td>
<td>@qnan</td>
</tr>
<tr>
<td>0x040</td>
<td>Signaling NaN</td>
<td>@snan</td>
</tr>
<tr>
<td>or the OR of the following two cases</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x001</td>
<td>Positive</td>
<td>@pos</td>
</tr>
<tr>
<td>0x002</td>
<td>Negative</td>
<td>@neg</td>
</tr>
<tr>
<td>AND’ed with OR of the following four cases</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x004</td>
<td>Zero</td>
<td>@zero</td>
</tr>
<tr>
<td>0x008</td>
<td>Unnormalized</td>
<td>@unorm</td>
</tr>
<tr>
<td>0x010</td>
<td>Normalized</td>
<td>@norm</td>
</tr>
<tr>
<td>0x020</td>
<td>Infinity</td>
<td>@inf</td>
</tr>
</tbody>
</table>
Operation:

```c
if (PR[qp]) {
    if (p1 == p2)
        illegal_operation_fault();

    if (tmp_isrcode = fp_reg_disabled(f2, 0, 0, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    tmp_rel = ((fclass_9_0 && !FR[f2].sign || fclass_9_1 && FR[f2].sign)
                && ((fclass_9_2 && fp_is_zero(FR[f2]))
                    || (fclass_9_3 && fp_is_unorm(FR[f2])))
                || (fclass_9_4 && fp_is_normal(FR[f2]))
                || (fclass_9_5 && fp_is_inf(FR[f2]))
                || (fclass_9_6 && fp_is_snan(FR[f2]))
                || (fclass_9_7 && fp_is_qnan(FR[f2]))
                || (fclass_9_8 && fp_is_natval(FR[f2])));

    tmp_nat = fp_is_natval(FR[f2]) && (!fclass_9_8);

    if (tmp_nat) {
        PR[p1] = 0;
        PR[p2] = 0;
    } else {
        PR[p1] = tmp_rel;
        PR[p2] = !tmp_rel;
    }
} else {
    if (fctype == 'unc') {
        if (p1 == p2)
            illegal_operation_fault();
        PR[p1] = 0;
        PR[p2] = 0;
    }
}
```

FP Exceptions: None

Interruptions: Illegal Operation fault

Disabled Floating-point Register fault
**fclrf — Floating-point Clear Flags**

**Format:**

\[(qp)fclrf.sf\]

**Description:**

The status field’s 6-bit flags field is reset to zero. The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

**Operation:**

\[
\text{if (PR[qp]) \{ \\
\quad \text{fp_set_sf_flags}(sf, 0); \}}
\]

**FP Exceptions:** None

**Interruptions:** None
fcmp — Floating-point Compare

Format:  
\[(qp) \text{ fcmparelctype} s f \ p_1, p_2 = f_2, f_3\]  

Description: The two source operands are compared for one of twelve relations specified by `frel`. This produces a boolean result which is 1 if the comparison condition is true, and 0 otherwise. This result is written to the two predicate register destinations, \(p_1\) and \(p_2\). The way the result is written to the destinations is determined by the compare type specified by `fctype`. The allowed types are Normal (or `none`) and `unc`.

Table 2-26. Floating-point Comparison Types

<table>
<thead>
<tr>
<th>fctype</th>
<th>PR([p_1]) PR([p_2])</th>
<th>PR([p_1]) PR([p_2])</th>
<th>PR([p_1]) PR([p_2])</th>
<th>PR([p_1]) PR([p_2])</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>0 0</td>
<td>0 1</td>
<td>1 0</td>
<td>0 0</td>
</tr>
<tr>
<td>unc</td>
<td>0 0</td>
<td>0 1</td>
<td>1 0</td>
<td>0 0</td>
</tr>
</tbody>
</table>

The mnemonic values for `sf` are given in Table 2-23 on page 3:50.

The relations are defined for each of the comparison types in Table 2-27. Of the twelve relations, not all are directly implemented in hardware. Some are actually pseudo-ops. For these, the assembler simply switches the source operand specifiers and/or switches the predicate target specifiers and uses an implemented relation.

Table 2-27. Floating-point Comparison Relations

<table>
<thead>
<tr>
<th>frel</th>
<th>frel Completer Unabbreviated</th>
<th>Relation</th>
<th>Pseudo-op of</th>
<th>Quiet NaN as Operand Signals Invalid</th>
</tr>
</thead>
<tbody>
<tr>
<td>eq</td>
<td>equal</td>
<td>(f_2 \equiv f_3)</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>lt</td>
<td>less than</td>
<td>(f_2 &lt; f_3)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>le</td>
<td>less than or equal</td>
<td>(f_2 \leq f_3)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>gt</td>
<td>greater than</td>
<td>(f_2 &gt; f_3)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>ge</td>
<td>greater than or equal</td>
<td>(f_2 \geq f_3)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>unord</td>
<td>unordered</td>
<td>(f_2 \neq f_3)</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>neq</td>
<td>not equal</td>
<td>!((f_2 \equiv f_3))</td>
<td>eq</td>
<td>(p_1 \leftrightarrow p_2)</td>
</tr>
<tr>
<td>nlt</td>
<td>not less than</td>
<td>!((f_2 &lt; f_3))</td>
<td>lt</td>
<td>(p_1 \leftrightarrow p_2)</td>
</tr>
<tr>
<td>nle</td>
<td>not less than or equal</td>
<td>!((f_2 \leq f_3))</td>
<td>le</td>
<td>(p_1 \leftrightarrow p_2)</td>
</tr>
<tr>
<td>ngt</td>
<td>not greater than</td>
<td>!((f_2 &gt; f_3))</td>
<td>lt</td>
<td>(f_2 \leftrightarrow f_3)</td>
</tr>
<tr>
<td>nge</td>
<td>not greater than or equal</td>
<td>!((f_2 \geq f_3))</td>
<td>le</td>
<td>(f_2 \leftrightarrow f_3)</td>
</tr>
<tr>
<td>ord</td>
<td>ordered</td>
<td>!((f_2 \neq f_3))</td>
<td>unord</td>
<td>(p_1 \leftrightarrow p_2)</td>
</tr>
</tbody>
</table>
Operation:  if (PR[qp]) {
  if (p1 == p2)
    illegal_operation_fault();

  if (tmp_isrcode = fp_reg_disabled(f2, f3, 0, 0))
    disabled_fp_register_fault(tmp_isrcode, 0);

  if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
    PR[p1] = 0;
    PR[p2] = 0;
  } else {
    fcmp_exception_fault_check(f2, f3, frel, sf, &tmp_fp_env);
    if (fp_raise_fault(tmp_fp_env))
      fp_exception_fault(fp_decode_fault(tmp_fp_env));

    tmp_fr2 = fp_reg_read(FR[f2]);
    tmp_fr3 = fp_reg_read(FR[f3]);

    if (frel == 'eq') tmp_rel = fp_equal(tmp_fr2, tmp_fr3);
    else if (frel == 'lt') tmp_rel = fp_less_than(tmp_fr2, tmp_fr3);
    else if (frel == 'le') tmp_rel = fp_lesser_or_equal(tmp_fr2, tmp_fr3);
    else if (frel == 'gt') tmp_rel = fp_less_than(tmp_fr3, tmp_fr2);
    else if (frel == 'ge') tmp_rel = fp_lesser_or_equal(tmp_fr3, tmp_fr2);
    else if (frel == 'unord') tmp_rel = fp_unordered(tmp_fr2, tmp_fr3);
    else if (frel == 'nlt') tmp_rel = !fp_less_than(tmp_fr2, tmp_fr3);
    else if (frel == 'nle') tmp_rel = !fp_lesser_or_equal(tmp_fr2, tmp_fr3);
    else if (frel == 'ngt') tmp_rel = !fp_less_than(tmp_fr3, tmp_fr2);
    else if (frel == 'nge') tmp_rel = !fp_lesser_or_equal(tmp_fr3, tmp_fr2);
    else tmp_rel = !fp_unordered(tmp_fr2, tmp_fr3); //'ord'

    PR[p1] = tmp_rel;
    PR[p2] = !tmp_rel;

    fp_update_fpsr(sf, tmp_fp_env);
  }
} else {
  if (fctype == 'unc') {
    if (p1 == p2)
      illegal_operation_fault();
    PR[p1] = 0;
    PR[p2] = 0;
  }
}

FP Exceptions: Invalid Operation (V)
Denormal/Unnormal Operand (D)
Software Assist (SWA) fault
**Interruptions:**
- Illegal Operation fault
- Disabled Floating-point Register fault
- Floating-point Exception fault
fcvt.fx — Convert Floating-point to Integer

**Format:**

- $(qp)$ fcvt.fx.$sf \ f_1 = f_2$
- $(qp)$ fcvt.fx.trunc.$sf \ f_1 = f_2$
- $(qp)$ fcvt.fxu.$sf \ f_1 = f_2$
- $(qp)$ fcvt.fxu.trunc.$sf \ f_1 = f_2$

**Description:**

$fr_{f_2}$ is treated as a register format floating-point value and converted to a signed (signed_form) or unsigned integer (unsigned_form) using either the rounding mode specified in the FPSR.$sf,rc$, or using Round-to-Zero if the trunc_form of the instruction is used. The result is placed in the 64-bit significand field of $fr_{f_1}$. The exponent field of $fr_{f_1}$ is set to the biased exponent for $2.0^{63}$ (0x1003E) and the sign field of $fr_{f_1}$ is set to positive (0). If the result of the conversion cannot be represented as a 64-bit integer, the 64-bit integer indefinite value 0x8000000000000000 is used as the result, if the IEEE Invalid Operation Floating-point Exception fault is disabled.

If $fr_{f_2}$ is a NaTVal, $fr_{f_1}$ is set to NaTVal instead of the computed result.

The mnemonic values for $sf$ are given in Table 2-23 on page 3:50.

**Operation:**

```c
if (PR[qp]) {
    fp_check_target_register(f_1);
    if (tmp_isrcode = fp_reg_disabled(f_1, f_2, 0, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (fp_is_natval(FR[f_2])) {
        FR[f_1] = NATVAL;
        fp_update_psr(f_1);
    } else {
        tmp_default_result = fcvt_exception_fault_check(f_2, signed_form, trunc_form, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));

        if (fp_is_nan(tmp_default_result)) {
            FR[f_1].significand = INTEGER_INDEFINITE;
            FR[f_1].exponent = FP_INTEGER_EXP;
            FR[f_1].sign = FP_SIGN_POSITIVE;
        } else {
            tmp_res = fp_ieee_rnd_to_int(fp_reg_read(FR[f_2]), &tmp_fp_env);
            if (tmp_res.exponent)
                tmp_res.significand = fp_U64_rsh(
                    tmp_res.significand, (FP_INTEGER_EXP - tmp_res.exponent));
            if (signed_form && tmp_res.sign)
                tmp_res.significand = (~tmp_res.significand) + 1;

            FR[f_1].significand = tmp_res.significand;
            FR[f_1].exponent = FP_INTEGER_EXP;
            FR[f_1].sign = FP_SIGN_POSITIVE;
        }
    }
}
fp_update_fpsr(sf, tmp_fp_env);
fp_update_psr(f_1);
if (fp_raise_traps(tmp_fp_env))
    fp_exception_trap(fp_decode_trap(tmp_fp_env));
```
FP Exceptions: Invalid Operation (V)  Inexact (I)
   Denormal/Unnormal Operand (D)
   Software Assist (SWA) fault

Interruptions:  Illegal Operation fault  Floating-point Exception fault
   Disabled Floating-point Register fault  Floating-point Exception trap
fcvt.xf — Convert Signed Integer to Floating-point

Format: \[(qp) \text{fcvt.xf } f_1 = f_2\]

Description: The 64-bit significand of FR\(f_2\) is treated as a signed integer and its register file precision floating-point representation is placed in FR\(f_1\).

If FR\(f_2\) is a NaTVal, FR\(f_1\) is set to NaTVal instead of the computed result.

This operation is always exact and is unaffected by the rounding mode.

Operation:

\[
\text{if (PR[qp])} \{
\text{fp_check_target_register}\(f_1\)\);
\text{if (tmp_isrcode = fp_reg_disabled(}f_1, f_2, 0, 0))
\quad \text{disabled_fp_register_fault(tmp_isrcode, 0);}
\text{if (fp_is_natval(FR[f_2]))} \{
\quad \text{FR}[f_1] = \text{NATVAL;}
\text{else} \{
\quad \text{tmp_res = FR}[f_2];
\text{if (tmp_res.significand(63))} \{
\quad \quad \text{tmp_res.significand} = (\sim\text{tmp_res.significand}) + 1;
\quad \quad \text{tmp_res.sign} = 1;
\text{else}
\quad \quad \text{tmp_res.sign} = 0;
\text{tmp_res.exponent} = \text{FP.INTEGER.EXP};
\quad \text{tmp_res} = \text{fp_normalize} (\text{tmp_res});
\text{FR}[f_1].\text{significand} = \text{tmp_res.significand;}
\text{FR}[f_1].\text{exponent} = \text{tmp_res.exponent;}
\text{FR}[f_1].\text{sign} = \text{tmp_res.sign;}
\}
\quad \text{fp_update_psr}(f_1);\}
\}
\]

FP Exceptions: None

Interruptions: Illegal Operation fault Disabled Floating-point Register fault
fcvt.xuf — Convert Unsigned Integer to Floating-point

Format:  
(qp) fcvt.xuf pc sf f1 = f3  
pseudo-op of: (qp) fma pc sf f1 = f3, f1, f0

Description:  
FR f3 is multiplied with FR 1, rounded to the precision indicated by pc (and possibly FPSR sf pc and FPSR sf wre) using the rounding mode specified by FPSR sf rc, and placed in FR f1.

Note:  
Multiplying FR f3 with FR 1 (a 1.0) normalizes the canonical representation of an integer in the floating-point register file producing a normal floating-point value.
If FR f3 is a NaTVal, FR f1 is set to NaTVal instead of the computed result.

The mnemonic values for the opcode’s pc are given in Table 2-22 on page 3:50. The mnemonic values for sf are given in Table 2-23 on page 3:50. For the encodings and interpretation of the status field’s pc, wre, and rc, refer to Table 5-6 and Table 5-5 on page 1:80.

Operation:  
See “fma — Floating-point Multiply Add” on page 3:70.
**fetchadd — Fetch and Add Immediate**

**Format:**

- \((qp)\) fetchadd4.sem.ldhint \(r_1 = [r_3], inc_3\)
  four_byte_form \(M17\)

- \((qp)\) fetchadd8.sem.ldhint \(r_1 = [r_3], inc_3\)
  eight_byte_form \(M17\)

**Description:**

A value consisting of four or eight bytes is read from memory starting at the address specified by the value in GR \(r_3\). The value is zero extended and added to the sign-extended immediate value specified by \(inc_3\). The values that may be specified by \(inc_3\) are: -16, -8, -4, -1, 1, 4, 8, 16. The least significant four or eight bytes of the sum are then written to memory starting at the address specified by the value in GR \(r_3\). The zero-extended value read from memory is placed in GR \(r_1\) and the NaT bit corresponding to GR \(r_1\) is cleared.

The \(sem\) completer specifies the type of semaphore operation. These operations are described in Table 2-28. See Section 4.4.7, “Sequentiality Attribute and Ordering” on page 2:69 for details on memory ordering.

**Table 2-28. Fetch and Add Semaphore Types**

<table>
<thead>
<tr>
<th>sem Completer</th>
<th>Ordering Semantics</th>
<th>Semaphore Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>acq</td>
<td>Acquire</td>
<td>The memory read/write is made visible prior to all subsequent data memory accesses.</td>
</tr>
<tr>
<td>rel</td>
<td>Release</td>
<td>The memory read/write is made visible after all previous data memory accesses.</td>
</tr>
</tbody>
</table>

The memory read and write are guaranteed to be atomic for accesses to pages with cacheable, writeback memory attribute. For accesses to other memory types, atomicity is platform dependent. Details on memory attributes are described in Section 4.4, “Memory Attributes” on page 2:63.

If the address specified by the value in GR \(r_3\) is not naturally aligned to the size of the value being accessed in memory, an Unaligned Data Reference fault is taken independent of the state of the User Mask alignment checking bit, UM.ac (PSR.ac in the Processor Status Register).

Both read and write access privileges for the referenced page are required. The write access privilege check is performed whether or not the memory write is performed.

Only accesses to UCE pages or cacheable pages with write-back write policy are permitted. Accesses to NaTPages result in a Data NaT Page Consumption fault. Accesses to pages with other memory attributes cause an Unsupported Data Reference fault.

On a processor model that supports exported fetchadd, a fetchadd to a UCE page causes the fetch-and-add operation to be exported outside of the processor; if the platform does not support exported fetchadd, the operation is undefined. On a processor model that does not support exported fetchadd, a fetchadd to a UCE page causes an Unsupported Data Reference fault. See Section 4.4.9, “Effects of Memory Attributes on Memory Reference Instructions” on page 2:73.

The value of the \(ldhint\) completer specifies the locality of the memory access. The values of the \(ldhint\) completer are given in Table 2-34 on page 3:132. Locality hints do not affect program functionality and may be ignored by the implementation. See Section 4.4.6, “Memory Hierarchy Control and Consistency” on page 1:60 for details.
**fetchadd**

**Operation:**

```c
if (PR[qp]) {
    check_target_register(r);

    if (GR[r].nat)
        register_nat_consumption_fault(SEMAPHORE);

    size = four_byte_form ? 4 : 8;

    paddr = tlb_translate(GR[r], size, SEMAPHORE, PSR.cpl, &mattr, &tmp_unused);
    if (!ma_supports_fetchadd(mattr))
        unsupported_data_reference_fault(SEMAPHORE, GR[r]);

    if (sem == 'acq')
        val = mem_xchg_add(inc, paddr, size, UM.be, mattr, ACQUIRE, ldhint);
    else // 'rel'
        val = mem_xchg_add(inc, paddr, size, UM.be, mattr, RELEASE, ldhint);

    alat_inval_multiple_entries(paddr, size);

    GR[r] = zero_ext(val, size * 8);
    GR[r].nat = 0;
}
```

**Interruptions:**

- Illegal Operation fault
- Register NaT Consumption fault
- Unimplemented Data Address fault
- Data Nested TLB fault
- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault
- Data NaT Page Consumption fault
- Data Key Miss fault
- Data Key Permission fault
- Data Access Rights fault
- Data Dirty Bit fault
- Data Access Bit fault
- Data Debug fault
- Unaligned Data Reference fault
- Unsupported Data Reference fault
**flushrs — Flush Register Stack**

**Format:**

`flushrs`  

**Description:**

All stacked general registers in the dirty partition of the register stack are written to the backing store before execution continues. The dirty partition contains registers from previous procedure frames that have not yet been saved to the backing store. For a description of the register stack partitions, refer to Chapter 6, “Register Stack Engine” in Volume 2. A pending external interrupt can interrupt the RSE store loop when enabled.

After this instruction completes execution BSPSTORE is equal to BSP.

This instruction must be the first instruction in an instruction group and must either be in instruction slot 0 or in instruction slot 1 of a template having a stop after slot 0; otherwise, the results are undefined. This instruction cannot be predicated.

**Operation:**

```c
while (AR[BSPSTORE] != AR[BSP]) {
    rse_store(MANDATORY); // increments AR[BSPSTORE]
    deliver_unmasked_pending_external_interrupt();
}
```

**Interruptions:**

Unimplemented Data Address fault  
VHPT Data fault  
Data Nested TLB fault  
Data TLB fault  
Alternate Data TLB fault  
Data Page Not Present fault  
Data NaT Page Consumption fault  
Data Key Miss fault  
Data Key Permission fault  
Data Access Rights fault  
Data Dirty Bit fault  
Data Access Bit fault  
Data Debug fault
fma — Floating-point Multiply Add

Format:  
\[(qp) \text{fma.pc.sf } f_1 = f_3.f_4.f_2\]

Description:  
The product of \( f_3 \) and \( f_4 \) is computed to infinite precision and then \( f_2 \) is added to this product, again in infinite precision. The resulting value is then rounded to the precision indicated by \( pc \) (and possibly FPSR.sf.pc and FPSR.sf.wire) using the rounding mode specified by FPSR.sf.rc. The rounded result is placed in FR\( f_1 \).

If any of \( f_3, f_4, \) or \( f_2 \) is a NaTVal, FR\( f_1 \) is set to NaTVal instead of the computed result.

If \( f_2 \) is 00, an IEEE multiply operation is performed instead of a multiply and add. See “fmpy — Floating-point Multiply” on page 3:77.

The mnemonic values for the opcode’s \( pc \) are given in Table 2-22 on page 3:50. The mnemonic values for \( sf \) are given in Table 2-23 on page 3:50. For the encodings and interpretation of the status field’s \( pc, \) \( wre \), and \( rc \), refer to Table 5-6 and Table 5-5 on page 1:80.

Operation:  
\[
\text{if (PR[qp])} \\
\quad \text{fp_check_target_register}(f_1); \\
\quad \text{if (tmp_isrcode = fp_reg_disabled(f_1, f_2, f_3, f_4))} \\
\quad \quad \text{disabled_fp_register_fault(tmp_isrcode, 0);} \\
\quad \text{if (fp_is_natval(FR[f_3]) || fp_is_natval(FR[f_4]))} \\
\quad \quad \text{FR[f_1] = NATVAL; } \\
\quad \text{fp_update_psr(f_1);} \\
\quad \text{else} \\
\quad \quad \text{tmp_default_result = fma_exception_fault_check(f_2, f_3, f_4, pc, sf, &tmp_fp_env);} \\
\quad \quad \text{if (fp_raise_fault(tmp_fp_env))} \\
\quad \quad \quad \text{fp_exception_fault(fp_decode_fault(tmp_fp_env));} \\
\quad \quad \text{if (fp_is_nan_or_inf(tmp_default_result))} \\
\quad \quad \quad \text{FR[f_1] = tmp_default_result;} \\
\quad \quad \text{else} \\
\quad \quad \quad \text{tmp_res = fp_mul(fp_reg_read(FR[f_3]), fp_reg_read(FR[f_4]));} \\
\quad \quad \quad \text{if (f_2 != 0)} \\
\quad \quad \quad \quad \text{tmp_res = fp_add(tmp_res, fp_reg_read(FR[f_2]), tmp_fp_env);} \\
\quad \quad \quad \text{FR[f_1] = fp_ieee_round(tmp_res, &tmp_fp_env);} \\
\quad \quad \text{fp_update_fpsr(sf, tmp_fp_env);} \\
\quad \text{fp_update_psr(f_1);} \\
\quad \text{if (fp_raise_traps(tmp_fp_env))} \\
\quad \quad \text{fp_exception_trap(fp_decode_trap(tmp_fp_env));} \\
\}
\]

FP Exceptions:  
Invalid Operation (V)  Underflow (U)  Denormal/Unnormalized Operand (D)  Overflow (O)  Software Assist (SWA) fault  Inexact (I)  Software Assist (SWA) trap

Interruptions:  
Illegal Operation fault  Floating-point Exception fault  Disabled Floating-point Register fault  Floating-point Exception trap
fmax — Floating-point Maximum

Format: \((qp)\ fmax.sf \ f_i = f_2, f_3\)

Description: The operand with the larger value is placed in \(f_1\). If \(f_2\) equals \(f_3\), \(f_1\) gets \(f_3\).
If either \(f_2\) or \(f_3\) is a NaN, \(f_1\) gets \(f_3\).
If either \(f_2\) or \(f_3\) is a NaTVal, \(f_1\) is set to NaTVal instead of the computed result.
This operation does not propagate NaNs the same way as other arithmetic floating-point instructions. The Invalid Operation is signaled in the same manner as the \(fcmp.lt\) operation.
The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

Operation:

```plaintext
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
    } else {
        fminmax_exception_fault_check(f2, f3, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));
        tmp_bool_res = fp_less_than(fp_reg_read(FR[f3]),
                                     fp_reg_read(FR[f2]));
        fp_update_fpsr(sf, tmp_fp_env);
    }
    fp_update_psr(f1);
}
```

FP Exceptions: Invalid Operation (V)
Denormal/Unnormal Operand (D)
Software Assist (SWA) fault

Interruptions: Illegal Operation fault Floating-point Exception fault
Disabled Floating-point Register fault
fmerge — Floating-point Merge

Format:

\[
\begin{align*}
(qp) \ fmerge.ns & \quad f_1 = f_2, f_3 \\
(qp) \ fmerge.s & \quad f_1 = f_2, f_3 \\
(qp) \ fmerge.se & \quad f_1 = f_2, f_3
\end{align*}
\]

Description:
Sign, exponent and significand fields are extracted from FR\_f_2 and FR\_f_3, combined, and the result is placed in FR\_f_1.

For the neg\_sign\_form, the sign of FR\_f_2 is negated and concatenated with the exponent and the significand of FR\_f_3. This form can be used to negate a floating-point number by using the same register for FR\_f_2 and FR\_f_3.

For the sign\_form, the sign of FR\_f_2 is concatenated with the exponent and the significand of FR\_f_3.

For the sign\_exp\_form, the sign and exponent of FR\_f_2 is concatenated with the significand of FR\_f_3.

For all forms, if either FR\_f_2 or FR\_f_3 is a NaTVal, FR\_f_1 is set to NaTVal instead of the computed result.

Figure 2-8. Floating-point Merge Negative Sign Operation

Figure 2-9. Floating-point Merge Sign Operation

Figure 2-10. Floating-point Merge Sign and Exponent Operation
Operation: if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
    } else {
        FR[f1].significant = FR[f3].significant;
        if (neg_sign_form) {
            FR[f1].exponent = FR[f3].exponent;
            FR[f1].sign = !FR[f2].sign;
        } else if (sign_form) {
            FR[f1].exponent = FR[f3].exponent;
            FR[f1].sign = FR[f2].sign;
        } else { // sign_exp_form
            FR[f1].exponent = FR[f2].exponent;
            FR[f1].sign = FR[f2].sign;
        }
    }
    fp_update_psr(f1);
}

FP Exceptions: None

Interruptions: Illegal Operation fault Disabled Floating-point Register fault
**fmin — Floating-point Minimum**

**Format:**

\[(qp) \text{fmin}\_sf \ f_1 = f_2, f_3\]  

**Description:**

The operand with the smaller value is placed in \(f_1\). If \(f_2\) equals \(f_3\), \(f_1\) gets \(f_3\).

If either \(f_2\) or \(f_3\) is a NaN, \(f_1\) gets \(f_3\).

If either \(f_2\) or \(f_3\) is a NaTVal, \(f_1\) is set to NaTVal instead of the computed result.

This operation does not propagate NaNs the same way as other arithmetic floating-point instructions. The Invalid Operation is signaled in the same manner as the \(f\text{cmp}.lt\) operation.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

**Operation:**

\[
\begin{align*}
\text{if } \{\text{PR[qp]}\} & \{
\text{fp\_check\_target\_register}(f_1); \\
& \text{if } \{\text{tmp\_isrcode} = \text{fp\_reg\_disabled}(f_1, f_2, f_3, 0)\}
\text{disabled\_fp\_register\_fault}(\text{tmp\_isrcode}, 0); \\
& \text{if } \{\text{fp\_is\_natval}(\text{FR}[f_2]) || \text{fp\_is\_natval}(\text{FR}[f_3])\} \{ \\
& \text{FR}[f_1] = \text{NATVAL}; \\
& \} \text{ else } \{
\text{fminmax\_exception\_fault\_check}(f_2, f_3, sf, \&\text{tmp\_fp\_env}); \\
& \text{if } \{\text{fp\_raise\_fault}(\text{tmp\_fp\_env})\}
\text{fp\_exception\_fault}(\text{fp\_decode\_fault}(\text{tmp\_fp\_env})); \\
& \text{tmp\_bool\_res} = \text{fp\_less\_than}(\text{fp\_reg\_read}(\text{FR}[f_2]), \\
& \text{fp\_reg\_read}(\text{FR}[f_3])); \\
& \text{FR}[f_1] = \text{tmp\_bool\_res} ? \text{FR}[f_2] : \text{FR}[f_3]; \\
& \text{fp\_update\_fpsr}(sf, \text{tmp\_fp\_env}); \\
& \} \\
& \text{fp\_update\_psr}(f_1);
\}
\end{align*}
\]

**FP Exceptions:**

- Invalid Operation (V)
- Denormal/Unnormal Operand (D)
- Software Assist (SWA) fault

**Interruptions:**

- Illegal Operation fault
- Floating-point Exception fault
- Disabled Floating-point Register fault
**fmix — Floating-point Mix**

**Format:**

(qp) fmix.l \( f_1 = f_2, f_3 \)

(qp) fmix.r \( f_1 = f_2, f_3 \)

(qp) fmix.lr \( f_1 = f_2, f_3 \)

**mix_l_form** F9

**mix_r_form** F9

**mix_lr_form** F9

**Description:**

For the mix_l_form (mix_r_form), the left (right) single precision value in FR \( f_2 \) is concatenated with the left (right) single precision value in FR \( f_3 \). For the mix_lr_form, the left single precision value in FR \( f_2 \) is concatenated with the right single precision value in FR \( f_3 \).

For all forms, the exponent field of FR \( f_1 \) is set to the biased exponent for \( 2.0^{63} \) (0x1003E) and the sign field of FR \( f_1 \) is set to positive (0).

For all forms, if either FR \( f_2 \) or FR \( f_3 \) is a NaTVal, FR \( f_1 \) is set to NaTVal instead of the computed result.

**Figure 2-11. Floating-point Mix Left**

![Figure 2-11](image1)

**Figure 2-12. Floating-point Mix Right**

![Figure 2-12](image2)

**Figure 2-13. Floating-point Mix Left-Right**

![Figure 2-13](image3)
Operation: 
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
    } else {
        if (mix_l_form) {
            tmp_res_hi = FR[f2].significand{63:32};
            tmp_res_lo = FR[f3].significand{63:32};
        } else if (mix_r_form) {
            tmp_res_hi = FR[f2].significand{31:0};
            tmp_res_lo = FR[f3].significand{31:0};
        } else { // mix_lr_form
            tmp_res_hi = FR[f2].significand{63:32};
            tmp_res_lo = FR[f3].significand{31:0};
        }
        FR[f1].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;
    }
    fp_update_psr(f1);
}

FP Exceptions: None

Interruptions: Illegal Operation fault
Disabled Floating-point Register fault
fmpy — Floating-point Multiply

Format:  

\[(qp)\text{fmpy.pcsf} f_1 = f_3, f_4\]  

pseudo-op of: \[(qp)\text{fma.pcsf} f_1 = f_3, f_4, 0\]

Description:  
The product FR\(_{f_3}\) and FR\(_{f_4}\) is computed to infinite precision. The resulting value is then rounded to the precision indicated by pc (and possibly FPSR.sf.pc and FPSR.sf.wr) using the rounding mode specified by FPSR.sf.rc. The rounded result is placed in FR\(_{f_1}\).

If either FR\(_{f_3}\) or FR\(_{f_4}\) is a NaTVal, FR\(_{f_1}\) is set to NaTVal instead of the computed result.

The mnemonic values for the opcode’s pc are given in Table 2-22 on page 3:50. The mnemonic values for sf are given in Table 2-23 on page 3:50. For the encodings and interpretation of the status field’s pc, wr, and rc, refer to Table 5-6 and Table 5-5 on page 1:80.

Operation:  
See “fma — Floating-point Multiply Add” on page 3:70.
**fms — Floating-point Multiply Subtract**

**Format:**

\[(qp) \text{fms}.pc.sf f_1 = f_3, f_4, f_2\]

**Description:**

The product of \(f_3\) and \(f_4\) is computed to infinite precision and then \(f_2\) is subtracted from this product, again in infinite precision. The resulting value is then rounded to the precision indicated by \(pc\) (and possibly FPSR.sf.pc and FPSR.sf.wre) using the rounding mode specified by FPSR.sf.rc. The rounded result is placed in \(f_1\).

If any of \(f_3\), \(f_4\), or \(f_2\) is a NaTVal, a NaTVal is placed in \(f_1\) instead of the computed result.

If \(f_2\) is \(f_0\), an IEEE multiply operation is performed instead of a multiply and subtract. See “fmpy — Floating-point Multiply” on page 3:77.

The mnemonic values for the opcode’s \(pc\) are given in Table 2-22 on page 3:50. The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50. For the encodings and interpretation of the status field’s \(pc\), \(wre\), and \(rc\), refer to Table 5-6 and Table 5-5 on page 1:80.

**Operation:**

```c
if (PR[qp]) {
  fp_check_target_register(f_1);
  if (tmp_isrcode = fp_reg_disabled(f_1, f_2, f_3, f_4))
    disabled_fp_register_fault(tmp_isrcode, 0);

  if (fp_is_natval(FR[f_2]) || fp_is_natval(FR[f_3]) ||
      fp_is_natval(FR[f_4])) {
    FR[f_1] = NATVAL;
    fp_update_psr(f_1);
  } else {
    tmp_default_result = fms_fnma_exception_fault_check(f_2, f_3, f_4, pc, sf, &tmp_fp_env);
    if (fp_raise_fault(tmp_fp_env))
      fp_exception_fault(fp_decode_fault(tmp_fp_env));
    if (fp_is_nan_or_inf(tmp_default_result)) {
      FR[f_1] = tmp_default_result;
    } else {
      tmp_res = fp_mul(fp_reg_read(FR[f_3]), fp_reg_read(FR[f_4]));
      tmp_fr2 = fp_reg_read(FR[f_2]);
      tmp_fr2.sign = !tmp_fr2.sign;
      if (f_2 != 0)
        tmp_res = fp_add(tmp_res, tmp_fr2, tmp_fp_env);
      FR[f_1] = fp_ieee_round(tmp_res, &tmp_fp_env);
    }
  }
  fp_update_fpsr(sf, tmp_fp_env);
  fp_update_psr(f_1);
  if (fp_raise_traps(tmp_fp_env))
    fp_exception_trap(fp_decode_trap(tmp_fp_env));
}
```

**FP Exceptions:**

Invalid Operation (V) \hspace{1cm} Underflow (U)
Denormal/Unnormal Operand (D) \hspace{1cm} Overflow (O)
Software Assist (SWA) fault \hspace{1cm} Inexact (I)
Software Assist (SWA) trap

**Interruptions:**

Illegal Operation fault \hspace{1cm} Floating-point Exception fault
Disabled Floating-point Register fault \hspace{1cm} Floating-point Exception trap
fneg — Floating-point Negate

**Format:**

(qp) fneg $f_2 = f_3$

pseudo-op of:

(qp) fmerge.ns $f_1 = f_3, f_2$

**Description:**

The value in FR $f_3$ is negated and placed in FR $f_1$.

If FR $f_3$ is a NaTVal, FR $f_1$ is set to NaTVal instead of the computed result.

**Operation:**

See “fmerge — Floating-point Merge” on page 3:72.
fnegabs — Floating-point Negate Absolute Value

Format: \((qp) \\text{fnegabs} \ f_1 = f_3\)  
 pseudo-op of: \((qp) \ \text{fmerge.ns} \ f_1 = f_0, f_3\)

Description: The absolute value of the value in FR\(f_3\) is computed, negated, and placed in FR\(f_1\).

If FR\(f_3\) is a NaTVal, FR\(f_1\) is set to NaTVal instead of the computed result.

fnma — Floating-point Negative Multiply Add

Format: \((qp)\ fnma.pc.sf\ f_1 = f_3, f_4, f_2\)

Description: The product of \(f_3\) and \(f_4\) is computed to infinite precision, negated, and then \(f_2\) is added to this product, again in infinite precision. The resulting value is then rounded to the precision indicated by \(pc\) (and possibly FPSR.sf,pc and FPSR.sf,wre) using the rounding mode specified by FPSR.sf,rc. The rounded result is placed in \(f_1\).

If any of \(f_3\), \(f_4\), or \(f_2\) is a NaNVal, \(f_1\) is set to NaNVal instead of the computed result.

If \(f_3\) is \(f_0\), an IEEE multiply operation is performed, followed by negation of the product. See “fnmpy — Floating-point Negative Multiply” on page 3:82.

The mnemonic values for the opcode’s \(pc\) are given in Table 2-22 on page 3:50. The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50. For the encodings and interpretation of the status field’s \(pc\), \(wre\), and \(rc\), refer to Table 5-6 and Table 5-5 on page 1:80.

Operation:

\[
\text{if (PR[qp])} \{
\text{fp_check_target_register}(f_1);
\text{if (tmp_isrcode = fp_reg_disabled}(f_1, f_2, f_3, f_4))
\text{disabled_fp_register_fault(tmp_isrcode, 0);}\
\text{if (fp_is_nan_or_inf}(f_2)) || \text{fp_is_nan_or_inf}(f_3) || \text{fp_is_nan_or_inf}(f_4))
\text{FR}[f_1] = \text{NATVAL};
\text{fp_update_psr}(f_1);
\} \text{else} \{
\text{tmp_default_result} = \text{fms_fnma_exception_fault_check}(f_2, f_3, f_4, pc, sf, \&tmp_fp_env);
\text{if (fp_raise_fault}(tmp_fp_env))
\text{fp_exception_fault(fp_decode_fault}(tmp_fp_env));
\}
\text{if (fp_is_nan_or_inf}(tmp_default_result)) \{\text{FR}[f_1] = tmp_default_result;\}
\text{else} \{\text{tmp_res} = \text{fp_mul}(fp_reg_read}(f_3), \text{fp_reg_read}(f_4));
\text{tmp_res.sign} = !\text{tmp_res.sign};
\text{if (f_2} != 0)
\text{tmp_res} = \text{fp_add}(tmp_res, \text{fp_reg_read}(f_2), \text{tmp_fp_env});
\text{FR}[f_1] = \text{fp_ieee_round}(tmp_res, \&tmp_fp_env);
\}
\text{fp_update_fpsr}(sf, \text{tmp_fp_env});
\text{fp_update_psr}(f_1);
\text{if (fp_raise_traps}(tmp_fp_env))
\text{fp_exception_trap(fp_decode_trap}(tmp_fp_env));
\}
\]

FP Exceptions: Invalid Operation (V) Underflow (U)
Denormal/Unnormal Operand (D) Overflow (O)
Software Assist (SWA) fault Inexact (I)
Software Assist (SWA) trap

Interruptions: Disabled Floating-point Register fault Floating-point Exception trap
fnmpy — Floating-point Negative Multiply

**Format:**

\[(qp) \text{ fnmpy.pc.sf} f_1 = f_3, f_4\]  

**pseudo-op of:** \[(qp) \text{ fnma.pc.sf} f_1 = f_3, f_4, 0\]

**Description:**

The product \(FR_{f_3}\) and \(FR_{f_4}\) is computed to infinite precision and then negated. The resulting value is then rounded to the precision indicated by \(pc\) (and possibly \(FPSR.sf.pc\) and \(FPSR.sf.wre\)) using the rounding mode specified by \(FPSR.sf.rc\). The rounded result is placed in \(FR_{f_1}\).

If either \(FR_{f_3}\) or \(FR_{f_4}\) is a NaTVal, \(FR_{f_1}\) is set to NaTVal instead of the computed result.

The mnemonic values for the opcode’s \(pc\) are given in Table 2-22 on page 3:50. The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50. For the encodings and interpretation of the status field’s \(pc\), \(wre\), and \(rc\), refer to Table 5-6 and Table 5-5 on page 1:80.

**Operation:**

See “fnma — Floating-point Negative Multiply Add” on page 3:81.
fnorm — Floating-point Normalize

Format: \( (qp) \text{fnorm}.pc.sf f_1 = f_3 \)  

pseudo-op of: \((qp) \text{fma}.pc.sf f_1 = f_3, f_1, f_0\)

Description: FR \( f_3 \) is normalized and rounded to the precision indicated by \( pc \) (and possibly FPSR.\( sf.pc \) and FPSR.\( sf.wre \)) using the rounding mode specified by FPSR.\( sf.rc \), and placed in FR \( f_1 \).

If FR \( f_3 \) is a NaTVal, FR \( f_1 \) is set to NaTVal instead of the computed result.

The mnemonic values for the opcode’s \( pc \) are given in Table 2-22 on page 3:50. The mnemonic values for \( sf \) are given in Table 2-23 on page 3:50. For the encodings and interpretation of the status field’s \( pc, wre, \) and \( rc \), refer to Table 5-6 and Table 5-5 on page 1:80.

Operation: See “fma — Floating-point Multiply Add” on page 3:70.
for — Floating-point Logical Or

Format: \[(qp)\] for \(f_1 = f_2, f_3\)

Description: The bit-wise logical OR of the significand fields of FR\(f_2\) and FR\(f_3\) is computed. The resulting value is stored in the significand field of FR\(f_1\). The exponent field of FR\(f_1\) is set to the biased exponent for 2.063 (0x1003E) and the sign field of FR\(f_1\) is set to positive (0).

If either FR\(f_2\) or FR\(f_3\) is a NaTVal, FR\(f_1\) is set to NaTVal instead of the computed result.

Operation: if (PR[qp]) {
    fp_check_target_register(f_1);
    if (tmp_isrcode = fp_reg_disabled(f_1, f_2, f_3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (fp_is_natval(FR[f_2]) || fp_is_natval(FR[f_3])) {
        FR[f_1] = NATVAL;
    } else {
        FR[f_1].significand = FR[f_2].significand | FR[f_3].significand;
        FR[f_1].exponent = FP_INTEGER_EXP;
        FR[f_1].sign = FP_SIGN_POSITIVE;
    }

    fp_update_psr(f_1);
}

FP Exceptions: None

Interruptions: Illegal Operation fault Disabled Floating-point Register fault
fpabs — Floating-point Parallel Absolute Value

Format: \((qp) \text{ fpabs } f1 = f3\)  \hspace{1cm} \text{pseudo-op of: (qp) fpmerge.s } f1 = f0, f3

Description: The absolute values of the pair of single precision values in the significand field of FR \(f_3\) are computed and stored in the significand field of FR \(f_1\). The exponent field of FR \(f_1\) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of FR \(f_1\) is set to positive (0).

If FR \(f_3\) is a NaTVal, FR \(f_1\) is set to NaTVal instead of the computed result.

**fpack — Floating-point Pack**

**Format:**
\[(qp) \ fpack \ f_1 = f_2, f_3 \]

**Description:**
The register format numbers in FR \( f_2 \) and FR \( f_3 \) are converted to single precision memory format. These two single precision numbers are concatenated and stored in the significand field of FR \( f_1 \). The exponent field of FR \( f_1 \) is set to the biased exponent for \( 2.0^{63} \) (0x1003E) and the sign field of FR \( f_1 \) is set to positive (0).

If either FR \( f_2 \) or FR \( f_3 \) is a NaTVal, FR \( f_1 \) is set to NaTVal instead of the computed result.

**Figure 2-14. Floating-point Pack**

```
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f_2, f_3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f_2]) || fp_is_natval(FR[f_3]))) {
        FR[f_1] = NATVAL;
    } else {
        tmp_res_hi = fp_single(FR[f_2]);
        tmp_res_lo = fp_single(FR[f_3]);
        FR[f_1].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f_1].exponent = FP_INTEGER_EXP;
        FR[f_1].sign = FP_SIGN_POSITIVE;
    }
    fp_update_psr(f1);
}
```

**FP Exceptions:** None

**Interruptions:** Illegal Operation fault

Disabled Floating-point Register fault
fpamax — Floating-point Parallel Absolute Maximum

Format: \( (gp) \text{fpamax}\.sf\ f_1 = f_2, f_3 \)

Description: The paired single precision values in the significands of \(f_2\) and \(f_3\) are compared. The operands with the larger absolute value are returned in the significand field of \(f_1\).

If the magnitude of high (low) \(f_3\) is less than the magnitude of high (low) \(f_2\), high (low) \(f_1\) gets high (low) \(f_2\). Otherwise high (low) \(f_1\) gets high (low) \(f_3\).

If high (low) \(f_2\) or high (low) \(f_3\) is a NaN, and neither \(f_2\) or \(f_3\) is a NaTVal, high (low) \(f_1\) gets high (low) \(f_3\).

The exponent field of \(f_1\) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of \(f_1\) is set to positive (0).

If either \(f_2\) or \(f_3\) is a NaTVal, \(f_1\) is set to NaTVal instead of the computed result.

This operation does not propagate NaNs the same way as other arithmetic floating-point instructions. The Invalid Operation is signaled in the same manner as for the \text{fpcomp}\.lt operation.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

Operation:

```plaintext
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
    } else {
        fpminmax_exception_fault_check(f2, f3, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));

        tmp_fr2 = tmp_right = fp_reg_read_hi(f2);
        tmp_fr3 = tmp_left = fp_reg_read_hi(f3);
        tmp_right.sign = FP_SIGN_POSITIVE;
        tmp_left.sign = FP_SIGN_POSITIVE;
        tmp_bool_res = fp_less_than(tmp_left, tmp_right);
        tmp_res_hi = fp_single(tmp_bool_res ? tmp_fr2: tmp_fr3);

        tmp_fr2 = tmp_right = fp_reg_read_lo(f2);
        tmp_fr3 = tmp_left = fp_reg_read_lo(f3);
        tmp_right.sign = FP_SIGN_POSITIVE;
        tmp_left.sign = FP_SIGN_POSITIVE;
        tmp_bool_res = fp_less_than(tmp_left, tmp_right);
        tmp_res_lo = fp_single(tmp_bool_res ? tmp_fr2: tmp_fr3);

        FR[f1].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;

        fp_update_fpsr(sf, tmp_fp_env);
    }
    fp_update_psr(f1);
}
```

FP Exceptions: Invalid Operation (V)
Denormal/Unnormal Operand (D)
Software Assist (SWA) fault

Interruptions: Illegal Operation fault Floating-point Exception fault
Disabled Floating-point Register fault
fpamin — Floating-point Parallel Absolute Minimum

Format: (qp) fpamin.sf f₁ = f₂, f₃

Description: The paired single precision values in the significands of FR f₂ or FR f₃ are compared. The operands with the smaller absolute value is returned in the significand of FR f₁.

If the magnitude of high (low) FR f₂ is less than the magnitude of high (low) FR f₃, high (low) FR f₁ gets high (low) FR f₂. Otherwise high (low) FR f₁ gets high (low) FR f₃.

If high (low) FR f₂ or high (low) FR f₃ is a NaN, and neither FR f₂ or FR f₃ is a NaTVal, high (low) FR f₁ gets high (low) FR f₃.

The exponent field of FR f₁ is set to the biased exponent for $2.063 \times 10^{03}$ (0x1003E) and the sign field of FR f₁ is set to positive ($0$).

If either FR f₂ or FR f₃ is NaTVal, FR f₁ is set to NaTVal instead of the computed result.

This operation does not propagate NaNs the same way as other arithmetic floating-point instructions. The Invalid Operation is signaled in the same manner as for the fpcmp lt operation.

The mnemonic values for sf are given in Table 2-23 on page 3:50.

Operation:

```c
if (PR[qp]) {
    fp_check_target_register(f₁);
    if (tmp_isrcode = fp_reg_disabled(f₁, f₂, f₃, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (fp_is_natval(FR[f₂]) || fp_is_natval(FR[f₃])) {
        FR[f₁] = NATVAL;
    } else {
        fpminmax_exception_fault_check(f₂, f₃, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));

        tmp_fr2 = tmp_left = fp_reg_read_hi(f₂);
        tmp_fr3 = tmp_right = fp_reg_read_hi(f₃);
        tmp_left.sign = FP_SIGN_POSITIVE;
        tmp_right.sign = FP_SIGN_POSITIVE;
        tmp_bool_res = fp_less_than(tmp_left, tmp_right);
        tmp_res_hi = fp_single(tmp_bool_res ? tmp_fr2 : tmp_fr3);

        tmp_fr2 = tmp_left = fp_reg_read_lo(f₂);
        tmp_fr3 = tmp_right = fp_reg_read_lo(f₃);
        tmp_left.sign = FP_SIGN_POSITIVE;
        tmp_right.sign = FP_SIGN_POSITIVE;
        tmp_bool_res = fp_less_than(tmp_left, tmp_right);
        tmp_res_lo = fp_single(tmp_bool_res ? tmp_fr2 : tmp_fr3);

        FR[f₁].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f₁].exponent = FP_INTEGER_EXP;
        FR[f₁].sign = FP_SIGN_POSITIVE;

        fp_update_fpsr(sf, tmp_fp_env);
    }
    fp_update_psr(f₁);
}
```

FP Exceptions: Invalid Operation (V)
Denormal/Unnormal Operand (D)
Software Assist (SWA) fault

Interruptions: Illegal Operation fault Floating-point Exception fault
Disabled Floating-point Register fault
fpcmp — Floating-point Parallel Compare

Format:  
\((qp)\) fpcmp,frl.sf \(f_1 = f_2, f_3\)

Description:  
The two pairs of single precision source operands in the significand fields of FR \(f_2\) and FR \(f_3\) are compared for one of twelve relations specified by \(frl\). This produces a boolean result which is a mask of 32 1’s if the comparison condition is true, and a mask of 32 0’s otherwise. This result is written to a pair of 32-bit integers in the significand field of FR \(f_1\). The exponent field of FR \(f_3\) is set to the biased exponent for \(2.063\) (0x1003E) and the sign field of FR \(f_1\) is set to positive (0).

Table 2-29. Floating-point Parallel Comparison Results

<table>
<thead>
<tr>
<th>PR[qp]==0</th>
<th>PR[qp]==1</th>
</tr>
</thead>
<tbody>
<tr>
<td>result==false, No Source NaTVals</td>
<td>result==true, No Source NaTVals</td>
</tr>
<tr>
<td>unchanged</td>
<td>0...0</td>
</tr>
</tbody>
</table>

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

The relations are defined for each of the comparison types in Table 2-29. Of the twelve relations, not all are directly implemented in hardware. Some are actually pseudo-ops. For these, the assembler simply switches the source operand specifiers and/or switches the predicate type specifiers and uses an implemented relation.

If either FR \(f_2\) or FR \(f_3\) is a NaTVal, FR \(f_1\) is set to NaTVal instead of the computed result.

Table 2-30. Floating-point Parallel Comparison Relations

<table>
<thead>
<tr>
<th>(frl)</th>
<th>(frl) Completer Unabbreviated</th>
<th>Relation</th>
<th>Pseudo-op of</th>
<th>Quiet NaN as Operand Invalid</th>
</tr>
</thead>
<tbody>
<tr>
<td>eq</td>
<td>equal</td>
<td>(f_2 == f_3)</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>lt</td>
<td>less than</td>
<td>(f_2 &lt; f_3)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>le</td>
<td>less than or equal</td>
<td>(f_2 \leq f_3)</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>gt</td>
<td>greater than</td>
<td>(f_2 &gt; f_3)</td>
<td>(f_2 \leftrightarrow f_3)</td>
<td>Yes</td>
</tr>
<tr>
<td>ge</td>
<td>greater than or equal</td>
<td>(f_2 \geq f_3)</td>
<td>(f_2 \leftrightarrow f_3)</td>
<td>Yes</td>
</tr>
<tr>
<td>unord</td>
<td>unordered</td>
<td>(f_2 \neq f_3)</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>neq</td>
<td>not equal</td>
<td>(\neg (f_2 == f_3))</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>nlt</td>
<td>not less than</td>
<td>(\neg (f_2 &lt; f_3))</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>nle</td>
<td>not less than or equal</td>
<td>(\neg (f_2 \leq f_3))</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>ngl</td>
<td>not greater than</td>
<td>(\neg (f_2 &gt; f_3))</td>
<td>(f_2 \leftrightarrow f_3)</td>
<td>Yes</td>
</tr>
<tr>
<td>nge</td>
<td>not greater than or equal</td>
<td>(\neg (f_2 \geq f_3))</td>
<td>(f_2 \leftrightarrow f_3)</td>
<td>Yes</td>
</tr>
<tr>
<td>ord</td>
<td>ordered</td>
<td>(f_2 \neq f_3)</td>
<td>No</td>
<td></td>
</tr>
</tbody>
</table>

Operation:

```c
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
    } else {
        fpcmp_exception_fault_check(f2, f3, frl, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));
        tmp_fr2 = fp_reg_read_hi(f2);
    }
```
tmp_fr3 = fp_reg_read_hi(f3);

if  (frel == 'eq')  tmp_rel = fp_equal(tmp_fr2, tmp_fr3);
else if (frel == 'lt') tmp_rel = fp_less_than(tmp_fr2, tmp_fr3);
else if (frel == 'le') tmp_rel = fp_lesser_or_equal(tmp_fr2, tmp_fr3);
else if (frel == 'gt') tmp_rel = fp_less_than(tmp_fr3, tmp_fr2);
else if (frel == 'ge') tmp_rel = fp_lesser_or_equal(tmp_fr3, tmp_fr2);
else if (frel == 'unord') tmp_rel = fp_unordered(tmp_fr2, tmp_fr3);
else if (frel == 'neq') tmp_rel = !fp_equal(tmp_fr2, tmp_fr3);
else if (frel == 'nlt') tmp_rel = !fp_less_than(tmp_fr2, tmp_fr3);
else if (frel == 'nle') tmp_rel = !fp_lesser_or_equal(tmp_fr2, tmp_fr3);
else if (frel == 'ngt') tmp_rel = !fp_less_than(tmp_fr3, tmp_fr2);
else if (frel == 'nge') tmp_rel = !fp_lesser_or_equal(tmp_fr3, tmp_fr2);
else tmp_rel = !fp_unordered(tmp_fr2, tmp_fr3);  // 'ord'

tmp_res_hi = (tmp_rel ? 0xFFFFFFFF : 0x00000000);

fr_1 = fp_reg_read_lo(f2);
fr_2 = fp_reg_read_lo(f3);

if  (frel == 'eq')  tmp_rel = fp_equal(tmp_fr2, tmp_fr3);
else if (frel == 'lt') tmp_rel = fp_less_than(tmp_fr2, tmp_fr3);
else if (frel == 'le') tmp_rel = fp_lesser_or_equal(tmp_fr2, tmp_fr3);
else if (frel == 'gt') tmp_rel = fp_less_than(tmp_fr3, tmp_fr2);
else if (frel == 'ge') tmp_rel = fp_lesser_or_equal(tmp_fr3, tmp_fr2);
else if (frel == 'unord') tmp_rel = fp_unordered(tmp_fr2, tmp_fr3);
else if (frel == 'neq') tmp_rel = !fp_equal(tmp_fr2, tmp_fr3);
else if (frel == 'nlt') tmp_rel = !fp_less_than(tmp_fr2, tmp_fr3);
else if (frel == 'nle') tmp_rel = !fp_lesser_or_equal(tmp_fr2, tmp_fr3);
else if (frel == 'ngt') tmp_rel = !fp_less_than(tmp_fr3, tmp_fr2);
else if (frel == 'nge') tmp_rel = !fp_lesser_or_equal(tmp_fr3, tmp_fr2);
else tmp_rel = !fp_unordered(tmp_fr2, tmp_fr3);  // 'ord'

tmp_res_lo = (tmp_rel ? 0xFFFFFFFF : 0x00000000);

fr_1.significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
fr_1.exponent = FP_INTEGER_EXP;
fr_1.sign = FP_SIGN_POSITIVE;

fp_update_fpsr(sf, tmp_fp_env);

FP Exceptions: Invalid Operation (V)
Denormal/Unnormal Operand (D)
Software Assist (SWA) fault

Interruptions:  Illegal Operation fault  Floating-point Exception fault
Disabled Floating-point Register fault
fpcvt.fx — Convert Parallel Floating-point to Integer

Format:  
\[(qp) \text{ fpcvt.fx.sf} f_1 = f_2\]  
\[(qp) \text{ fpcvt.fx.trunc.sf} f_1 = f_2\]  
\[(qp) \text{ fpcvt.fxu.sf} f_1 = f_2\]  
\[(qp) \text{ fpcvt.fxu.trunc.sf} f_1 = f_2\]

Description: The pair of single precision values in the significand field of \(f_2\) is converted to a pair of 32-bit signed integers (signed_form) or unsigned integers (unsigned_form) using either the rounding mode specified in the FPSR.sf.rc, or using Round-to-Zero if the trunc_form of the instruction is used. The result is written as a pair of 32-bit integers into the significand field of \(f_1\). The exponent field of \(f_1\) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of \(f_1\) is set to positive (0). If the result of the conversion cannot be represented as a 32-bit integer, the 32-bit integer indefinite value 0x80000000 is used as the result, if the IEEE Invalid Operation Floating-point Exception fault is disabled.

If \(f_2\) is a NaTVal, \(f_1\) is set to NaTVal instead of the computed result.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

Operation:  
```c
if (PR[qp]) {  
    fp_check_target_register(f1);  
    if (tmp_isrcode = fp_reg_disabled(f1, f2, 0, 0))  
        disabled_fp_register_fault(tmp_isrcode, 0);  
    if (fp_is_natval(FR[f2])) {  
        FR[f1] = NATVAL;  
        fp_update_psr(f1);  
    } else {  
        tmp_default_result_pair = fpcvt_exception_fault_check(f2,  
            signed_form, trunc_form, sf, &tmp_fp_env);  
        if (fp_raise_fault(tmp_fp_env))  
            fp_exception_fault(fp_decode_fault(tmp_fp_env));  
        if (fp_is_nan(tmp_default_result_pair.hi)) {  
            tmp_res_hi = INTEGER_INDEFINITE_32_BIT;  
        } else {  
            tmp_res = fp_ieee_rnd_to_int_sp(fp_reg_read_hi(f2), HIGH,  
                &tmp_fp_env);  
            if (tmp_res.exponent)  
                tmp_res.significand = fp_U64_rsh(  
                    tmp_res.significand, (FP_INTEGER_EXP - tmp_res.exponent));  
            if (signed_form && tmp_res.sign)  
                tmp_res.significand = (~tmp_res.significand) + 1;  
            tmp_res_hi = tmp_res.significand{31:0};  
        }  
        if (fp_is_nan(tmp_default_result_pair.lo)) {  
            tmp_res_lo = INTEGER_INDEFINITE_32_BIT;  
        } else {  
            tmp_res = fp_ieee_rnd_to_int_sp(fp_reg_read_lo(f2), LOW,  
                &tmp_fp_env);  
            if (tmp_res.exponent)  
                tmp_res.significand = fp_U64_rsh(  
                    tmp_res.significand, (FP_INTEGER_EXP - tmp_res.exponent));  
            if (signed_form && tmp_res.sign)  
                tmp_res.significand = (~tmp_res.significand) + 1;  
            tmp_res_lo = tmp_res.significand{31:0};  
    }
```
fpcvt.fx

} } } 

FR[f_i].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
FR[f_i].exponent = FP_INTEGER_EXP;
FR[f_i].sign = FP_SIGN_POSITIVE;

fp_update_fpsr(sf, tmp_fp_env);
fp_update_psrf(f_i);
if (fp_raise_traps(tmp_fp_env))
    fp_exception_trap(fp_decode_trap(tmp_fp_env));

FP Exceptions: Invalid Operation (V) Inexact (I)
Denormal/Unnormal Operand (D) Software Assist (SWA) Fault

Interruptions: Illegal Operation fault Floating-point Exception fault
Disabled Floating-point Register fault Floating-point Exception trap
fpma — Floating-point Parallel Multiply Add

Format: \((fpma.sf f_1, f_3, f_4, f_2)\)

Description: The pair of products of the pairs of single precision values in the significand fields of \(FR\ f_3\) and \(FR\ f_4\) are computed to infinite precision and then the pair of single precision values in the significand field of \(FR\ f_2\) is added to these products, again in infinite precision. The resulting values are then rounded to single precision using the rounding mode specified by FPSR.sf.rc. The pair of rounded results are stored in the significand field of \(FR\ f_1\). The exponent field of \(FR\ f_1\) is set to the biased exponent for \(2.063\) (0x1003E) and the sign field of \(FR\ f_1\) is set to positive (0).

If any of \(FR\ f_3\), \(FR\ f_4\), or \(FR\ f_2\) is a NaTVal, \(FR\ f_1\) is set to NaTVal instead of the computed results.

Note: If \(f_2\) is 0 in the fpma instruction, just the IEEE multiply operation is performed. (See “fpmpy — Floating-point Parallel Multiply” on page 3:99.) \(FR\ f_1\), as an operand, is not a packed pair of 1.0 values, it is just the register file format’s 1.0 value.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.
The encodings and interpretation for the status field’s \(rc\) are given in Table 5-5 on page 1:80.

Operation:

\[
\text{if } (PR[qp]) \{ \quad \text{fp_check_target_register}(f_1); \\
\quad \text{if } (\text{tmp_isrcode} = \text{fp_reg_disabled}(f_1, f_3, f_4)) \quad \text{disabled_fp_register_fault(tmp_isrcode, 0)}; \\
\quad \text{if } (\text{fp_is_natval}(FR[f_2]))) \quad | \quad \text{fp_is_natval}(FR[f_3]))) \quad | \\
\quad \text{fp_is_natval}(FR[f_4])) \{ \\
\quad \quad \text{FR}[f_1] = \text{NATVAL}; \\
\quad \quad \text{fp_update_psr}(f_1); \\
\quad \} \quad \text{else } \{ \\
\quad \quad \text{tmp_default_result_pair} = \text{fpma_exception_fault_check}(f_2, \\
\quad \quad \quad f_3, f_4, sf, \&tmp_fp_env); \\
\quad \quad \text{if } (\text{fp_raise_fault}(tmp_fp_env)) \\
\quad \quad \quad \text{fp_exception_fault(fp_decode_fault(tmp_fp_env))}; \\
\quad \quad \text{if } (\text{fp_is_nan_or_inf}(\text{tmp_default_result_pair}.hi)) \{ \\
\quad \quad \quad \text{tmp_res_hi} = \text{fp_single}(\text{tmp_default_result_pair}.hi); \\
\quad \quad \} \quad \text{else } \{ \\
\quad \quad \quad \text{tmp_res} = \text{fp_mul}(\text{fp_reg_read_hi}(f_3), \text{fp_reg_read_hi}(f_4)); \\
\quad \quad \quad \text{if } (f_2 != 0) \\
\quad \quad \quad \text{tmp_res} = \text{fp_add}(\text{tmp_res}, \text{fp_reg_read_hi}(f_2), \text{tmp_fp_env}); \\
\quad \quad \quad \text{tmp_res_hi} = \text{fp_ieee_round_sp}(\text{tmp_res}, \text{HIGH}, \&\text{tmp_fp_env}); \\
\quad \quad \} \\
\quad \quad \text{if } (\text{fp_is_nan_or_inf}(\text{tmp_default_result_pair}.lo)) \{ \\
\quad \quad \quad \text{tmp_res_lo} = \text{fp_single}(\text{tmp_default_result_pair}.lo); \\
\quad \quad \} \quad \text{else } \{ \\
\quad \quad \quad \text{tmp_res} = \text{fp_mul}(\text{fp_reg_read_lo}(f_3), \text{fp_reg_read_lo}(f_4)); \\
\quad \quad \quad \text{if } (f_2 != 0) \\
\quad \quad \quad \text{tmp_res} = \text{fp_add}(\text{tmp_res}, \text{fp_reg_read_lo}(f_2), \text{tmp_fp_env}); \\
\quad \quad \quad \text{tmp_res_lo} = \text{fp_ieee_round_sp}(\text{tmp_res}, \text{LOW}, \&\text{tmp_fp_env}); \\
\quad \quad \} \\
\quad \} \\
\} \\
\} \\
\} \\
\text{FR}[f_1].\text{significand} = \text{fp_concatenate}(\text{tmp_res_hi}, \text{tmp_res_lo}); \\
\text{FR}[f_1].\text{exponent} = \text{FP_INTEGER_EXP}; \\
\text{FR}[f_1].\text{sign} = \text{FP_SIGN_POSITIVE}; \\
\text{fp_update_fpsr(sf, tmp_fp_env);} \\
\text{fp_update_psr(f_1);} \\
\text{if } (\text{fp_raise_traps}(tmp_fp_env)) \\
\text{fp_exception_trap(fp_decode_trap(tmp_fp_env));}
FP Exceptions: Invalid Operation (V)  Underflow (U)
Denormal/Unnormal Operand (D)  Overflow (O)
Software Assist (SWA) Fault  Inexact (I)
Software Assist (SWA) trap

Interruptions:  Illegal Operation fault  Floating-point Exception fault
Disabled Floating-point Register fault  Floating-point Exception trap
**fpmax — Floating-point Parallel Maximum**

**Format:**  
\((QP) \text{ fpmax.sf } f_1 = f_2, f_3\)

**Description:**  
The paired single precision values in the significands of FR\(_{f_2}\) or FR\(_{f_3}\) are compared. The operands with the larger value is returned in the significand of FR\(_{f_1}\).

If the value of high (low) FR\(_{f_2}\) is less than the value of high (low) FR\(_{f_3}\), high (low) FR\(_{f_1}\) gets high (low) FR\(_{f_2}\). Otherwise high (low) FR\(_{f_1}\) gets high (low) FR\(_{f_3}\).

If high (low) FR\(_{f_2}\) or high (low) FR\(_{f_3}\) is a NaN, high (low) FR\(_{f_1}\) gets high (low) FR\(_{f_3}\).

The exponent field of FR\(_{f_1}\) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of FR\(_{f_1}\) is set to positive (0).

If either FR\(_{f_2}\) or FR\(_{f_3}\) is NaTVal, FR\(_{f_1}\) is set to NaTVal instead of the computed result.

This operation does not propagate NaNs the same way as other arithmetic floating-point instructions. The Invalid Operation is signaled in the same manner as for the fpcmp.lt operation.

The mnemonic values for sf are given in Table 2-23 on page 3:50.

**Operation:**  
```c
if (PR[QP]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
    } else {
        fpminmax_exception_fault_check(f2, f3, sf, &tmp_fp_env);
        fp_exception_fault(fp_decode_fault(tmp_fp_env));
        tmp_fr2 = tmp_right = fp_reg_read_hi(f2);
        tmp_fr3 = tmp_left = fp_reg_read_hi(f3);
        tmp_bool_res = fp_less_than(tmp_left, tmp_right);
        tmp_res_hi = fp_single(tmp_bool_res ? tmp_fr2 : tmp_fr3);
        tmp_fr2 = tmp_right = fp_reg_read_lo(f2);
        tmp_fr3 = tmp_left = fp_reg_read_lo(f3);
        tmp_bool_res = fp_less_than(tmp_left, tmp_right);
        tmp_res_lo = fp_single(tmp_bool_res ? tmp_fr2 : tmp_fr3);
        FR[f1].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;
    }
    fp_update_fpsr(sf, tmp_fp_env);
}
```

**FP Exceptions:** Invalid Operation (V)  
Denormal/Unnormal Operand (D)  
Software Assist (SWA) fault

**Interruptions:**  
Illegal Operation fault  
Floating-point Exception fault  
Disabled Floating-point Register fault
fpmerge — Floating-point Parallel Merge

Format:

- \((qp)\) fpmerge.ns \(f_1 = f_2.f_3\)
- \((qp)\) fpmerge.s \(f_1 = f_2.f_3\)
- \((qp)\) fpmerge.se \(f_1 = f_2.f_3\)

Description:

For the neg_sign_form, the signs of the pair of single precision values in the significand field of \(f_2\) are negated and concatenated with the exponents and the significands of the pair of single precision values in the significand field of \(f_3\) and stored in the significand field of \(f_1\). This form can be used to negate a pair of single precision floating-point numbers by using the same register for \(f_2\) and \(f_3\).

For the sign_form, the signs of the pair of single precision values in the significand field of \(f_2\) are concatenated with the exponents and the significands of the pair of single precision values in the significand field of \(f_3\) and stored in \(f_1\).

For the sign_exp_form, the signs and exponents of the pair of single precision values in the significand field of \(f_2\) are concatenated with the pair of single precision significands in the significand field of \(f_3\) and stored in the significand field of \(f_1\).

For all forms, the exponent field of \(f_1\) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of \(f_1\) is set to positive (0).

For all forms, if either \(f_2\) or \(f_3\) is a NaN, \(f_1\) is set to NaN instead of the computed result.

Figure 2-15. Floating-point Parallel Merge Negative Sign Operation

Figure 2-16. Floating-point Parallel Merge Sign Operation

Figure 2-17. Floating-point Parallel Merge Sign and Exponent Operation
**Operation:**

```c
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3]))
        FR[f1] = NATVAL;
    else {
        if (neg_sign_form) {
            tmp_res_hi = (!FR[f2].significand{63} << 31)
                        | (FR[f3].significand{62:32});
            tmp_res_lo = (!FR[f2].significand{31} << 31)
                        | (FR[f3].significand{30:0});
        } else if (sign_form) {
            tmp_res_hi = (FR[f2].significand{63} << 31)
                        | (FR[f3].significand{62:32});
            tmp_res_lo = (FR[f2].significand{31} << 31)
                        | (FR[f3].significand{30:0});
        } else { // sign_exp_form
            tmp_res_hi = (FR[f2].significand{63:55} << 23)
                        | (FR[f3].significand{54:32});
            tmp_res_lo = (FR[f2].significand{31:23} << 23)
                        | (FR[f3].significand{22:0});
        }
        FR[f1].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;
    }
    fp_update_psr(f1);
}
```

**FP Exceptions:** None

**Interruptions:** Illegal Operation fault  Disabled Floating-point Register fault
fpmin — Floating-point Parallel Minimum

Format: \((qp)\) fpmin.sf \(f_1 = f_2, f_3\)

Description:
The paired single precision values in the significands of \(f_2\) or \(f_3\) are compared. The operands with the smaller value is returned in significand of \(f_1\).

If the value of high (low) \(f_2\) is less than the value of high (low) \(f_3\), high (low) \(f_1\) gets high (low) \(f_2\). Otherwise high (low) \(f_1\) gets high (low) \(f_3\).

If high (low) \(f_2\) or high (low) \(f_3\) is a NaN, high (low) \(f_1\) gets high (low) \(f_3\).

The exponent field of \(f_1\) is set to the biased exponent for \(2.063 \times 10^{-3}\) (0x1003E) and the sign field of \(f_1\) is set to positive (0).

If either \(f_2\) or \(f_3\) is a NaNVal, \(f_1\) is set to NaNVal instead of the computed result.

This operation does not propagate NaNs the same way as other arithmetic floating-point instructions. The Invalid Operation is signaled in the same manner as for the \(fpcmp.lt\) operation.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

Operation:
```c
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
    } else {
        fpminmax_exception_fault_check(f2, f3, sf, &tmp_fp_env);
        fp_exception_fault(fp_decode_fault(tmp_fp_env));
        tmp_fr2 = tmp_left = fp_reg_read_hi(f2);
        tmp_fr3 = tmp_right = fp_reg_read_hi(f3);
        tmp_bool_res = fp_less_than(tmp_left, tmp_right);
        tmp_res_hi = fp_single(tmp_bool_res ? tmp_fr2: tmp_fr3);
        tmp_fr2 = tmp_left = fp_reg_read_lo(f2);
        tmp_fr3 = tmp_right = fp_reg_read_lo(f3);
        tmp_bool_res = fp_less_than(tmp_left, tmp_right);
        tmp_res_lo = fp_single(tmp_bool_res ? tmp_fr2: tmp_fr3);
        FR[f1].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;
        fp_update_fpsr(sf, tmp_fp_env);
    }
    fp_update_psr(f1);
}
```

FP Exceptions:
Invalid Operation (V)
Denormal/Unnormal Operand (D)
Software Assist (SWA) fault

Interruptions:
Illegal Operation fault
Floating-point Exception fault
Disabled Floating-point Register fault
fpmpy — Floating-point Parallel Multiply

Format: \( (qp) \) fpmpy.sf \( f_1 = f_3, f_4 \)  
\( \) pseudo-op of: \( (qp) \) fpma.sf \( f_1 = f_3, f_4, f_0 \)

Description: The pair of products of the pairs of single precision values in the significand fields of FR \( f_3 \) and FR \( f_4 \) are computed to infinite precision. The resulting values are then rounded to single precision using the rounding mode specified by FPSR.sf.rc. The pair of rounded results are stored in the significand field of FR \( f_1 \). The exponent field of FR \( f_1 \) is set to the biased exponent for \( 2.0^{03} \) (0x1003E) and the sign field of FR \( f_1 \) is set to positive (0).

If either FR \( f_3 \), or FR \( f_4 \) is a NaTVal, FR \( f_1 \) is set to NaTVal instead of the computed results.

The mnemonic values for \( sf \) are given in Table 2-23 on page 3:50.
The encodings and interpretation for the status field’s \( rc \) are given in Table 5-5 on page 1:80.

fpms — Floating-point Parallel Multiply Subtract

Format:  \((qp)\) fpms.sf \(f_1 = f_3, f_4, f_2\)

Description: The pair of products of the pairs of single precision values in the significand fields of \(FR_f_3\) and \(FR_f_4\) are computed to infinite precision and then the pair of single precision values in the significand field of \(FR_f_2\) is subtracted from these products, again in infinite precision. The resulting values are then rounded to single precision using the rounding mode specified by FPSR.sf.rc. The pair of rounded results are stored in the significand field of \(FR_f_1\). The exponent field of \(FR_f_1\) is set to the biased exponent for \(2.0^{53}\) (0x1003E) and the sign field of \(FR_f_1\) is set to positive (0).

Note: If any of \(FR_f_3\), \(FR_f_4\), or \(FR_f_2\) is a NaNVal, \(FR_f_1\) is set to NaNVal instead of the computed results.

Mapping: If \(f_2\) is f0 in the fpms instruction, just the IEEE multiply operation is performed.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.
The encodings and interpretation for the status field’s \(rc\) are given in Table 5-5 on page 1:80.

Operation: if (PR[qp]) {
    fp_check_target_register(f_1);
    if (tmp_isrcode = fp_reg_disabled(f_1, f_3, f_4))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f_2]) || fp_is_natval(FR[f_3]) ||
        fp_is_natval(FR[f_4])) {
        FR[f_1] = NATVAL;
        fp_update_psr(f_1);
    } else {
        tmp_default_result_pair = fpms_fpnma_exception_fault_check(f_2, f_3, f_4, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            exception_fault(fp_decode_fault(tmp_fp_env));
        if (fp_is_nan_or_inf(tmp_default_result_pair.hi)) {
            tmp_hi = fp_single(tmp_default_result_pair.hi);
        } else {
            tmp_res = fp_mul(fp_reg_read_hi(f_3), fp_reg_read_hi(f_4));
            if (f_2 != 0) {
                tmp_sub = fp_reg_read_hi(f_2);
                tmp_sub.sign = !tmp_sub.sign;
                tmp_res = fp_add(tmp_res, tmp_sub, tmp_fp_env);
            }
            tmp_res_hi = fp_ieee_round_sp(tmp_res, HIGH, &tmp_fp_env);
        }
        if (fp_is_nan_or_inf(tmp_default_result_pair.lo)) {
            tmp_lo = fp_single(tmp_default_result_pair.lo);
        } else {
            tmp_res = fp_mul(fp_reg_read_lo(f_3), fp_reg_read_lo(f_4));
            if (f_2 != 0) {
                tmp_sub = fp_reg_read_lo(f_2);
                tmp_sub.sign = !tmp_sub.sign;
                tmp_res = fp_add(tmp_res, tmp_sub, tmp_fp_env);
            }
            tmp_res_lo = fp_ieee_round_sp(tmp_res, LOW, &tmp_fp_env);
        }
        FR[f_1].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f_1].exponent = FP_INTEGER_EXP;  
}
FR[f_j].sign = FP_SIGN_POSITIVE;

fp_update_fpsr(sf, tmp_fp_env);
fp_update_psr(f_j);
if (fp_raise_traps(tmp_fp_env))
   fp_exception_trap(fp_decode_trap(tmp_fp_env));
}

**FP Exceptions:**
- Invalid Operation (V)
- Denormal/Unnormal Operand (D)
- Software Assist (SWA) fault
- Overflow (O)
- Inexact (I)
- Software Assist (SWA) trap

**Interruptions:**
- Illegal Operation fault
- Disabled Floating-point Register fault
- Floating-point Exception fault
- Floating-point Exception trap
fpneg — Floating-point Parallel Negate

Format: \[(qp)\ \text{fpneg}\ f_1 = f_3\]  
pseudo-op of: \[(qp)\ \text{fpmerge.ns}\ f_1 = f_3.f_3\]

Description: The pair of single precision values in the significand field of FR\( f_3 \) are negated and stored in the significand field of FR\( f_1 \). The exponent field of FR\( f_1 \) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of FR\( f_1 \) is set to positive (0).

If FR\( f_3 \) is a NaTVal, FR\( f_1 \) is set to NaTVal instead of the computed result.

fpnegabs — Floating-point Parallel Negate Absolute Value

Format: \( (qp) \text{ fpnegabs } f_1 = f_3 \)

pseudo-op of: \( (qp) \text{ fpmerge.ns } f_1 = f_0, f_3 \)

Description: The absolute values of the pair of single precision values in the significand field of \( FR_f_3 \) are computed, negated and stored in the significand field of \( FR_f_1 \). The exponent field of \( FR_f_1 \) is set to the biased exponent for \( 2.0^{63} \) (0x1003E) and the sign field of \( FR_f_1 \) is set to positive (0).

If \( FR_f_3 \) is a NaTVal, \( FR_f_1 \) is set to NaTVal instead of the computed result.

fpnma — Floating-point Parallel Negative Multiply Add

Format:

\[(qp) \text{fpnma} sf f_1 = f_3, f_4, f_2\]

Description:

The pair of products of the pairs of single precision values in the significand fields of FR\(f_3\) and FR\(f_4\) are computed to infinite precision, negated, and then the pair of single precision values in the significand field of FR\(f_2\) are added to these (negated) products, again in infinite precision. The resulting values are then rounded to single precision using the rounding mode specified by FPSR.\(sf,rc\). The pair of rounded results are stored in the significand field of FR\(f_1\). The exponent field of FR\(f_1\) is set to the biased exponent for 2.0^{65} (0x1003E) and the sign field of FR\(f_1\) is set to positive (0).

If any of FR\(f_3\), FR\(f_4\), or FR\(f_2\) is a NaTVal, FR\(f_1\) is set to NaTVal instead of the computed result.

Note: If \(f_2\) is 0 in the fpnma instruction, just the IEEE multiply operation (with the product being negated before rounding) is performed.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

The encodings and interpretation for the status field’s \(rc\) are given in Table 5-5 on page 1:80.

Operation:

```c
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, f4))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f3]) || fp_is_natval(FR[f4]) ||
        fp_is_natval(FR[f2])) {
        FR[f1] = NATVAL;
        fp_update_psr(f1);
    } else {
        tmp_default_result_pair = fpms_fpnma_exception_fault_check(f2, f3, f4, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));
        if (fp_is_nan_or_inf(tmp_default_result_pair.hi)) {
            tmp_res_hi = fp_single(tmp_default_result_pair.hi);
            if (f2 != 0)
                tmp_res = fp_add(tmp_res, fp_reg_read_hi(f2), tmp_fp_env);
            tmp_res_hi = fp_ieee_round_sp(tmp_res, HIGH, &tmp_fp_env);
        }
        if (fp_is_nan_or_inf(tmp_default_result_pair.lo)) {
            tmp_res_lo = fp_single(tmp_default_result_pair.lo);
        } else {
            tmp_res = fp_mul(fp_reg_read_hi(f3), fp_reg_read_hi(f4));
            tmp_res.sign = !tmp_res.sign;
            if (f2 != 0)
                tmp_res = fp_add(tmp_res, fp_reg_read_hi(f2), tmp_fp_env);
            tmp_res_lo = fp_ieee_round_sp(tmp_res, LOW, &tmp_fp_env);
        }
        if (!FR[f1].significand)
            fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;
        fp_update_fpsr(sf, tmp_fp_env);
        fp_update_psr(f1);
    }
}
```
if (fp_raise_traps(tmp_fp_env))
    fp_exception_trap(fp_decode_trap(tmp_fp_env));
}

**FP Exceptions:**
- Invalid Operation (V)
- Denormal/Unnormal Operand (D)
- Software Assist (SWA) fault
- Underflow (U)
- Overflow (O)
- Inexact (I)
- Software Assist (SWA) trap

**Interruptions:**
- Illegal Operation fault
- Disabled Floating-point Register fault
- Floating-point Exception fault
- Floating-point Exception trap
fpnmpy — Floating-point Parallel Negative Multiply

**Format:**

\[(qp) \text{ fpnmpy.s} f_{1} = f_{3}, f_{4}\]

pseudo-op of: \[(qp) \text{ fpnma.s} f_{1} = f_{3}, f_{4}, 0\]

**Description:**

The pair of products of the pairs of single precision values in the significand fields of \(F_{R} f_{3}\) and \(F_{R} f_{4}\) are computed to infinite precision and then negated. The resulting values are then rounded to single precision using the rounding mode specified by \(\text{FPSR.s} \text{r} \text{c}\). The pair of rounded results are stored in the significand field of \(F_{R} f_{1}\). The exponent field of \(F_{R} f_{1}\) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of \(F_{R} f_{1}\) is set to positive (0).

If either \(F_{R} f_{3}\) or \(F_{R} f_{4}\) is a NaTVal, \(F_{R} f_{1}\) is set to NaTVal instead of the computed results.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

The encodings and interpretation for the status field’s \(rc\) are given in Table 5-5 on page 1:80.

**Operation:**

See “fpnma — Floating-point Parallel Negative Multiply Add” on page 3:104.
fprcpa — Floating-point Parallel Reciprocal Approximation

**Format:**

\[(qp)\, fprcpa.sf\, f_1, p_2 = f_2, f_3\]

**Description:**

If PR.\(qp\) is 0, PR.\(p_2\) is cleared and FR.\(f_1\) remains unchanged.

If PR.\(qp\) is 1, the following will occur:

- Each half of the significand of FR.\(f_1\) is either set to an approximation (with a relative error < \(2^{-8.886}\)) of the reciprocal of the corresponding half of FR.\(f_3\), or set to the IEEE-754 mandated response for the quotient FR.\(f_2\)/FR.\(f_3\) of the corresponding half — if that half of FR.\(f_2\) or of FR.\(f_3\) is in the set \{-Infinity, -0, +0, +Infinity, NaN\}.

- If either half of FR.\(f_1\) is set to the IEEE-754 mandated quotient, or is set to an approximation of the reciprocal which may cause the Newton-Raphson iterations to fail to produce the correct IEEE-754 divide result, then PR.\(p_2\) is set to 0, otherwise it is set to 1.

For correct IEEE divide results, when PR.\(p_2\) is cleared, user software is expected to compute the quotient (FR.\(f_2\)/FR.\(f_3\)) for each half (using the non-parallel \(frcpa\) instruction), and merge the results into FR.\(f_1\), keeping PR.\(p_2\) cleared.

- The exponent field of FR.\(f_1\) is set to the biased exponent for \(2^{63}\) (0x1003E) and the sign field of FR.\(f_1\) is set to positive (0).

- If either FR.\(f_2\) or FR.\(f_3\) is a NaTVal, FR.\(f_1\) is set to NaTVal instead of the computed result, and PR.\(p_2\) is cleared.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

**Operation:**

```c
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
        PR[p2] = 0;
    } else {
        tmp_default_result_pair = fprcpa_exception_fault_check(f2, f3, sf,
            &tmp_fp_env, &limits_check);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));
        if (fp_is_nan_or_inf(tmp_default_result_pair.hi) ||
            limits_check.hi_fr3) {
            tmp_res_hi = fp_single(tmp_default_result_pair.hi);
            tmp_pred_hi = 0;
        } else {
            num = fp_normalize(fp_reg_read_hi(f2));
            den = fp_normalize(fp_reg_read_hi(f3));
            if (fp_is_inf(num) && fp_is_finite(den)) {
                tmp_res = FP_INFINITY;
                tmp_res.sign = num.sign ^ den.sign;
                tmp_pred_hi = 0;
            } else if (fp_is_finite(num) && fp_is_inf(den)) {
                tmp_res = FP_ZERO;
                tmp_res.sign = num.sign ^ den.sign;
                tmp_pred_hi = 0;
            } else if (fp_is_zero(num) && fp_is_finite(den)) {
                tmp_res = FP_ZERO;
                tmp_res.sign = num.sign ^ den.sign;
                tmp_pred_hi = 0;
            } else if (fp_is_zero(num) && fp_is_zero(den)) {
                tmp_res = FP_ZERO;
                tmp_res.sign = num.sign ^ den.sign;
                tmp_pred_hi = 0;
```
} else {
    tmp_res = fp_ieee_recip(den);
    if (limits_check.hi_fr2_or_quot)
        tmp_pred_hi = 0;
    else
        tmp_pred_hi = 1;
}
    tmp_res_hi = fp_single(tmp_res);
}
if (fp_is_nan_or_inf(tmp_default_result_pair.lo) ||
    limits_check.lo_fr3) {
    tmp_res_lo = fp_single(tmp_default_result_pair.lo);
    tmp_pred_lo = 0;
} else {
    num = fp_normalize(fp_reg_read_lo(f 2));
    den = fp_normalize(fp_reg_read_lo(f 3));
    if (fp_is_inf(num) && fp_is_finite(den)) {
        tmp_res = FP_INFINITY;
        tmp_res.sign = num.sign ^ den.sign;
        tmp_pred_lo = 0;
    } else if (fp_is_finite(num) && fp_is_inf(den)) {
        tmp_res = FP_ZERO;
        tmp_res.sign = num.sign ^ den.sign;
        tmp_pred_lo = 0;
    } else if (fp_is_zero(num) && fp_is_finite(den)) {
        tmp_res = FP_ZERO;
        tmp_res.sign = num.sign ^ den.sign;
        tmp_pred_lo = 0;
    } else {
        tmp_res = fp_ieee_recip(den);
        if (limits_check.lo_fr2_or_quot)
            tmp_pred_lo = 0;
        else
            tmp_pred_lo = 1;
    }
    tmp_res_lo = fp_single(tmp_res);
}

FR[f_i].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
FR[f_i].exponent = FP_INTEGER_EXP;
FR[f_i].sign = FP_SIGN_POSITIVE;
PR[p 2] = tmp_pred_hi && tmp_pred_lo;

fp_update_fpsr(sf, tmp_fp_env);
}
else (f pupdate_psr(f_i);
} else {
    PR[p 2] = 0;
}

**FP Exceptions:** Invalid Operation (V)
Zero Divide (Z)
Denormal/Unnormal Operand (D)
Software Assist (SWA) fault

**Interruptions:** Illegal Operation fault Floating-point Exception fault
Disabled Floating-point Register fault
fprsqrta — Floating-point Parallel Reciprocal Square Root Approximation

Format: \((qp)\) fprsqrta.sf f₁, p₂ = f₃  

Description: If PR \(qp\) is 0, PR \(p₂\) is cleared and FR \(f₁\) remains unchanged.

If PR \(qp\) is 1, the following will occur:

- Each half of the significand of FR \(f₁\) is either set to an approximation (with a relative error < \(2^{-8.831}\)) of the reciprocal square root of the corresponding half of FR \(f₃\), or set to the IEEE-754 compliant response for the reciprocal square root of the corresponding half of FR \(f₃\) — if that half of FR \(f₃\) is in the set \{-Infinity, -Finite, -0, +0, +Infinity, NaN\}.

- If either half of FR \(f₁\) is set to the IEEE-754 mandated reciprocal square root, or is set to an approximation of the reciprocal square root which may cause the Newton-Raphson iterations to fail to produce the correct IEEE-754 square root result, then PR \(p₂\) is set to 0, otherwise it is set to 1.

For correct IEEE square root results, when PR \(p₂\) is cleared, user software is expected to compute the square root for each half (using the non-parallel frsqrta instruction), and merge the results in FR \(f₁\), keeping PR \(p₂\) cleared.

- The exponent field of FR \(f₁\) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of FR \(f₁\) is set to positive (0).

- If FR \(f₃\) is a NaTVal, FR \(f₁\) is set to NaTVal instead of the computed result, and PR \(p₂\) is cleared.

The mnemonic values for sf are given in Table 2-23 on page 3:50.

Operation: if (PR[qp]) {
    fp_check_target_register(f₁);
    if (tmp_isrcode = fp_reg_disabled(f₁, f₃, 0, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (fp_is_natval(FR[f₃])) {
        FR[f₁] = NATVAL;
        PR[p₂] = 0;
    } else {
        tmp_default_result_pair = fprsqrta_exception_fault_check(f₃, sf, &tmp_fp_env, &limits_check);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));

        if (fp_is_nan(tmp_default_result_pair.hi)) {
            tmp_res_hi = fp_single(tmp_default_result_pair.hi);
            tmp_pred_hi = 0;
        } else {
            tmp_fr3 = fp_normalize(fp_reg_read_hi(f₃));
            if (fp_is_zero(tmp_fr3)) {
                tmp_res = FP_INFINITY;
                tmp_res.sign = tmp_fr3.sign;
                tmp_pred_hi = 0;
            } else if (fp_is_pos_inf(tmp_fr3)) {
                tmp_res = FP_ZERO;
                tmp_pred_hi = 0;
            } else {
                tmp_res = fp_ieee_recip_sqrt(tmp_fr3);
                if (limits_check.hi)
                    tmp_pred_hi = 0;
                else
                    tmp_pred_hi = 1;
        }
    }
}
if (fp_is_nan(tmp_default_result_pair.lo)) {
    tmp_res_lo = fp_single(tmp_default_result_pair.lo);
    tmp_pred_lo = 0;
} else {
    tmp_fr3 = fp_normalize(fp_reg_read_lo(f 3));
    if (fp_is_zero(tmp_fr3)) {
        tmp_res = FP_INFINITY;
        tmp_res.sign = tmp_fr3.sign;
        tmp_pred_lo = 0;
    } else if (fp_is_pos_inf(tmp_fr3)) {
        tmp_res = FP_ZERO;
        tmp_pred_lo = 0;
    } else {
        tmp_res = fp_ieee_recip_sqrt(tmp_fr3);
        if (limits_check.lo)
            tmp_pred_lo = 0;
        else
            tmp_pred_lo = 1;
    }
    tmp_res_lo = fp_single(tmp_res);
}
FR[f 1].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
FR[f 1].exponent = FP_INTEGER_EXP;
FR[f 1].sign = FP_SIGN_POSITIVE;
PR[p 2] = tmp_pred_hi && tmp_pred_lo;
fp_update_fpsr(sf, tmp_fp_env);
} else {
    PR[p 2] = 0;
}

FP Exceptions: Invalid Operation (V)
Denormal/Unnormal Operand (D)
Software Assist (SWA) fault

Interruptions: Illegal Operation fault Floating-point Exception fault
Disabled Floating-point Register fault
frcpa — Floating-point Reciprocal Approximation

Format: \( (qp \text{ frcpa sf } f_2, p_2 = f_2, f_3) \)

Description: If PR\( qp \) is 0, PR\( p_2 \) is cleared and FR\( f_1 \) remains unchanged.

If PR\( qp \) is 1, the following will occur:

- FR\( f_1 \) is either set to an approximation (with a relative error < \( 2^{-8.886} \)) of the reciprocal of FR\( f_3 \), or to the IEEE-754 mandated quotient of FR\( f_2/FR f_3 \) — if either FR\( f_2 \) or FR\( f_3 \) is in the set \{-Infinity, -0, Pseudo-zero, +0, +Infinity, NaN, Unsupported\}.
- If FR\( f_1 \) is set to the approximation of the reciprocal of FR\( f_3 \), then PR\( p_2 \) is set to 1; otherwise, it is set to 0.
- If FR\( f_2 \) and FR\( f_3 \) are such that the approximation of FR\( f_3 \)'s reciprocal may cause the Newton-Raphson iterations to fail to produce the correct IEEE-754 result of FR\( f_2/FR f_3 \), then a Floating-point Exception fault for Software Assist occurs.
- System software is expected to compute the IEEE-754 quotient (FR\( f_2/FR f_3 \)), return the result in FR\( f_1 \), and set PR\( p_2 \) to 0.
- If either FR\( f_2 \) or FR\( f_3 \) is a NaTVal, FR\( f_1 \) is set to NaTVal instead of the computed result, and PR\( p_2 \) is cleared.

The mnemonic values for \( sf \) are given in Table 2-23 on page 3:50.

Operation:

```c
if (PR[qp]) {
    fp_check_target_register(fj);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
        PR[p2] = 0;
    } else {
        tmp_default_result = frcpa_exception_fault_check(f2, f3, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));
        if (fp_is_nan_or_inf(tmp_default_result)) {
            FR[f1] = tmp_default_result;
            PR[p2] = 0;
        } else {
            num = fp_normalize(fp_reg_read(FR[f2]));
            den = fp_normalize(fp_reg_read(FR[f3]));
            if (fp_is_inf(num) && fp_is_finite(den)) {
                FR[f1] = FP_INFINITY;
                FR[f1].sign = num.sign ^ den.sign;
                PR[p2] = 0;
            } else if (fp_is_finite(num) && fp_is_inf(den)) {
                FR[f1] = FP_ZERO;
                FR[f1].sign = num.sign ^ den.sign;
                PR[p2] = 0;
            } else if (fp_is_zero(num) && fp_is_finite(den)) {
                FR[f1] = FP_ZERO;
                FR[f1].sign = num.sign ^ den.sign;
                PR[p2] = 0;
            } else if (fp_is_zero(num) && fp_is_zero(den)) {
                FR[f1] = FP_INFINITY;
                FR[f1].sign = num.sign ^ den.sign;
                PR[p2] = 0;
            } else {
                FR[f1] = fp_ieee_recip(den);
                PR[p2] = 1;
            }
        }
    }
```
frcpa

void fp_update_fpsr(sfp, tmp_fp_env);
}
void fp_update_psr(f1);
} else {
PR[p2] = 0;
}
// fp_ieee_recip()

fp_ieee_recip(den) {

RECIP_TABLE[256] = {
    0x3fc, 0x3f4, 0x3e4, 0x3dd, 0x3d5, 0x3cd, 0x3c6,
    0x3be, 0x3b7, 0x3af, 0x3a1, 0x39d, 0x39f, 0x39b,
    0x384, 0x37d, 0x36f, 0x368, 0x361, 0x35b, 0x354,
    0x34d, 0x346, 0x339, 0x333, 0x32c, 0x326, 0x320,
    0x319, 0x313, 0x307, 0x300, 0x2fa, 0x2f4, 0x2ee,
    0x2e8, 0x2e2, 0x2dc, 0x2d1, 0x2cb, 0x2c5, 0x2bf,
    0x2ba, 0x2b4, 0x2af, 0x2a3, 0x29e, 0x299, 0x293,
    0x28e, 0x288, 0x27e, 0x279, 0x273, 0x26e, 0x269,
    0x264, 0x25f, 0x25a, 0x255, 0x250, 0x24f, 0x246,
    0x23c, 0x237, 0x22e, 0x229, 0x224, 0x21f, 0x21b,
    0x216, 0x211, 0x208, 0x204, 0x1ff, 0x1fb, 0x1f6,
    0x1f2, 0x1ed, 0x1e9, 0x1e5, 0x1ed, 0x1d8, 0x1d4,
    0x1cf, 0x1cb, 0x1c7, 0x1c3, 0x1bf, 0x1bb, 0x1b6,
    0x1ae, 0x1aa, 0x1a6, 0x1a2, 0x19e, 0x199, 0x193,
    0x18f, 0x18b, 0x17f, 0x17c, 0x17b, 0x174,
    0x171, 0x16d, 0x16b, 0x166, 0x162, 0x15d, 0x15b,
    0x15d, 0x150, 0x14d, 0x149, 0x146, 0x142, 0x13f,
    0x138, 0x134, 0x131, 0x12e, 0x12a, 0x127, 0x124,
    0x11d, 0x11a, 0x117, 0x113, 0x110, 0x10d, 0x10a,
    0x103, 0x100, 0x0f7, 0x0f4, 0x0f1, 0x0ee,
    0x0eb, 0x0e8, 0x0e5, 0x0e2, 0x0df, 0x0d9, 0x0d6,
    0x0d3, 0x0d0, 0xc0, 0xc8, 0xc5, 0xc2, 0xbf,
    0x0bc, 0x0b9, 0x0b7, 0x0b4, 0x0b1, 0xa9, 0xa6,
    0x0a5, 0x0a4, 0x0a1, 0x09e, 0x09c, 0x099, 0x096,
    0x091, 0x08e, 0x08c, 0x089, 0x087, 0x084, 0x07f,
    0x07c, 0x07a, 0x077, 0x075, 0x073, 0x070, 0x06e,
    0x069, 0x066, 0x064, 0x061, 0x05f, 0x059, 0x05a,
    0x05b, 0x057, 0x053, 0x04f, 0x04c, 0x04a, 0x048,
    0x043, 0x041, 0x03f, 0x03c, 0x03a, 0x038, 0x036,
    0x033, 0x031, 0x02f, 0x02d, 0x02b, 0x029, 0x026,
    0x024, 0x022, 0x020, 0x01e, 0x01c, 0x01a, 0x018,
    0x015, 0x013, 0x011, 0x00f, 0x00d, 0x00b, 0x009,
    0x007, 0x005, 0x003, 0x001,
};

tmp_index = den.significand(62:55);
tmp_res.significand = (1 << 63) | (RECIP_TABLE[tmp_index] << 53);
tmp_res.exponent = FP_REG_EXP_ONES - 2 - den.exponent;
tmp_res.sign = den.sign;
return (tmp_res);
}

**FP Exceptions:**
- Invalid Operation (V)
- Zero Divide (Z)
- Denormal/Unnormal Operand (D)
- Software Assist (SWA) fault

**Interruptions:**
- Illegal Operation fault
- Floating-point Exception fault
- Disabled Floating-point Register fault
frsqrta — Floating-point Reciprocal Square Root Approximation

Format: \((qp)\) frsqrta.sf \(f_1, p_2 = f_3\)

Description: If PR \(qp\) is 0, PR \(p_2\) is cleared and FR \(f_1\) remains unchanged.

If PR \(qp\) is 1, the following will occur:

- FR \(f_1\) is either set to an approximation (with a relative error < \(2^{-8.831}\)) of the reciprocal square root of FR \(f_3\), or set to the IEEE-754 mandated square root of FR \(f_3\) — if FR \(f_3\) is in the set \{-Infinity, -Finite, -0, Pseudo-zero, +0, +Infinity, NaN, Unsupported\}.
- If FR \(f_1\) is set to an approximation of the reciprocal square root of FR \(f_3\), then PR \(p_2\) is set to 1; otherwise, it is set to 0.
- If FR \(f_3\) is such the approximation of its reciprocal square root may cause the Newton-Raphson iterations to fail to produce the correct IEEE-754 square root result, then a Floating-point Exception fault for Software Assist occurs.

System software is expected to compute the IEEE-754 square root, return the result in FR \(f_1\), and set PR \(p_2\) to 0.

- If FR \(f_3\) is a NaTVal, FR \(f_1\) is set to NaTVal instead of the computed result, and PR \(p_2\) is cleared.

The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50.

Operation:

```c
if (PR[qp]) {
    fp_check_target_register(f_1);
    if (tmp_isrcode = fp_reg_disabled(f_1, f_3, 0, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f_3])) {
        FR[f_1] = NATVAL;
        PR[p_2] = 0;
    } else {
        tmp_default_result = frsqrta_exception_fault_check(f_3, sf, &tmp_fp_env);
        if (fp_raise_fault(tmp_fp_env))
            fp_exception_fault(fp_decode_fault(tmp_fp_env));
        if (fp_is_nan(tmp_default_result)) {
            FR[f_1] = tmp_default_result;
            PR[p_2] = 0;
        } else {
            tmp_fr3 = fp_normalize(fp_reg_read(FR[f_3]));
            if (fp_is_zero(tmp_fr3)) {
                FR[f_1] = tmp_fr3;
                PR[p_2] = 0;
            } else if (fp_is_pos_inf(tmp_fr3)) {
                FR[f_1] = tmp_fr3;
                PR[p_2] = 0;
            } else {
                FR[f_1] = fp_ieee_recip_sqrt(tmp_fr3);
                PR[p_2] = 1;
            }
        }
    }
    fp_update_fpsr(sf, tmp_fp_env);
    fp_update_psr(f_1);
} else {
    PR[p_2] = 0;
}
```
// fp_ieee_recip_sqrt()

fp_ieee_recip_sqrt(root) {
    RECIP_SQRT_TABLE[256] = {
        0x1a5, 0x1a0, 0x19a, 0x195, 0x18f, 0x18a, 0x185, 0x180,
        0x17a, 0x170, 0x16b, 0x166, 0x161, 0x15d, 0x158,
        0x153, 0x14e, 0x14a, 0x145, 0x140, 0x13c, 0x138, 0x133,
        0x12f, 0x12a, 0x126, 0x122, 0x11e, 0x11a, 0x115, 0x111,
        0x10d, 0x109, 0x105, 0x101, 0x0fd, 0x0fa, 0x0f6, 0x0f2,
        0x0ee, 0x0ea, 0x0e7, 0x0e3, 0x0df, 0x0dc, 0x0db, 0x0d5,
        0x0d1, 0x0ce, 0x0ca, 0x0c7, 0x0c3, 0x0c0, 0x0b6, 0x0b9,
        0x0b6, 0x0b3, 0x0b0, 0x0a6, 0x0a3, 0x0a0, 0x09d, 0x09a,
        0x097, 0x094, 0x091, 0x08e, 0x0b8, 0x088,
        0x085, 0x082, 0x07f, 0x07d, 0x07a, 0x077, 0x074, 0x071,
        0x06f, 0x06c, 0x069, 0x066, 0x064, 0x061, 0x05f, 0x05c,
        0x05a, 0x057, 0x054, 0x052, 0x04f, 0x04d, 0x04a, 0x048,
        0x045, 0x043, 0x041, 0x03e, 0x03c, 0x03a, 0x037, 0x035,
        0x033, 0x030, 0x02e, 0x02c, 0x029, 0x027, 0x025, 0x023,
        0x020, 0x01e, 0x01c, 0x01a, 0x018, 0x016, 0x014, 0x011,
        0x00f, 0x00d, 0x00b, 0x009, 0x007, 0x005, 0x003, 0x001,
        0x3fc, 0x3f4, 0x3ec, 0x3e5, 0x3dd, 0x3d5, 0x3ce, 0x3c7,
        0x3bf, 0x3b8, 0x3b1, 0x3aa, 0x3a3, 0x39c, 0x395, 0x38e,
        0x388, 0x381, 0x37a, 0x374, 0x36d, 0x367, 0x361, 0x35a,
        0x354, 0x34e, 0x348, 0x342, 0x33c, 0x336, 0x330, 0x32b,
        0x325, 0x31f, 0x31a, 0x314, 0x30f, 0x309, 0x304, 0x2fe,
        0x2f9, 0x2f4, 0x2ee, 0x2e9, 0x2e4, 0x2d6, 0x2da, 0x2d5,
        0x2d0, 0x2cb, 0x2ce, 0x2c1, 0x2bd, 0x2b8, 0x2b3, 0x2ae,
        0x2aa, 0x2a5, 0x2a1, 0x29c, 0x298, 0x293, 0x28f, 0x28a,
        0x286, 0x282, 0x27d, 0x279, 0x275, 0x271, 0x26d, 0x268,
        0x264, 0x260, 0x25c, 0x258, 0x254, 0x250, 0x24c, 0x249,
        0x245, 0x241, 0x23d, 0x239, 0x235, 0x232, 0x22e, 0x22a,
        0x227, 0x223, 0x220, 0x21c, 0x218, 0x215, 0x211, 0x20e,
        0x20a, 0x207, 0x204, 0x200, 0x1fd, 0x1f9, 0x1f6, 0x1f3,
        0x1f0, 0x1e8, 0x1e9, 0x1e6, 0x1e3, 0xfd, 0xfc, 0xf9,
        0xf18, 0x1d9, 0x1d6, 0x1d3, 0x1d0, 0x1c7, 0x1c4, 0x1c1,
        0x1be, 0x1bb, 0x1b8, 0x1b5, 0x1b2, 0x1af, 0x1ac, 0x1aa,
    };

    tmp_index = (root.exponent{0} << 7) | root.significand{62:56};
    tmp_res.significand = (1 << 63) | (RECIP_SQRT_TABLE[tmp_index] << 53);
    tmp_res.exponent = FP_REG_EXP_HALF -
        ((root.exponent - FP_REG_BIAS) >> 1);  
    tmp_res.sign = FP_SIGN_POSITIVE;
    return (tmp_res);
}

FP Exceptions:
- Invalid Operation (V)
- Denormal/Unnormal Operand (D)
- Software Assist (SWA) fault

Interruptions:
- Illegal Operation fault
- Floating-point Exception fault
- Disabled Floating-point Register fault
fselect — Floating-point Select

Format: \((qp)\) fselect \(f_1 = f_3, f_4, f_2\)

Description: The significand field of \(FR_{f_3}\) is logically AND-ed with the significand field of \(FR_{f_2}\) and the significand field of \(FR_{f_4}\) is logically AND-ed with the one’s complement of the significand field of \(FR_{f_2}\). The two results are logically OR-ed together. The result is placed in the significand field of \(FR_{f_1}\).

The exponent field of \(FR_{f_1}\) is set to the biased exponent for \(2.063\) (0x1003E). The sign bit field of \(FR_{f_1}\) is set to positive (0).

If any of \(FR_{f_3}\), \(FR_{f_4}\), or \(FR_{f_2}\) is a NaTVal, \(FR_{f_1}\) is set to NaTVal instead of the computed result.

Operation:

```c
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, f4))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3]) || fp_is_natval(FR[f4])) {
        FR[f1] = NATVAL;
    } else {
        FR[f1].significand = (FR[f3].significand & FR[f2].significand)
                         | (FR[f4].significand & ~FR[f2].significand);
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;
    }
    fp_update_psr(f1);
}
```

FP Exceptions: None

Interruptions: Illegal Operation fault Disabled Floating-point Register fault
**fsetc — Floating-point Set Controls**

**Format:** 

```plaintext
(qp) fsetc sf amask7, omask7
```

**Description:** 

The status field’s control bits are initialized to the value obtained by logically AND-ing the `sf0.controls` and `amask7` immediate field and logically OR-ing the `omask7` immediate field.

The mnemonic values for `sf` are given in Table 2-23 on page 3:50.

**Operation:** 

```plaintext
if (PR[qp]) {
    tmp_controls = (AR[FPSR].sf0.controls & amask7) | omask7;
    if (is_reserved_field(FSETC, sf, tmp_controls))
        reserved_register_field_fault();
    fp_set_sf_controls(sf, tmp_controls);
}
```

**FP Exceptions:** None

**Interruptions:** Reserved Register/Field fault
fsub — Floating-point Subtract

Format: \((qp) \ fsub.pc.sf \ f_1 = f_3, f_2\)  

pseudo-op of: \((qp) \ fms.pc.sf \ f_1 = f_3, f_1, f_2\)

Description: FR\(f_2\) is subtracted from FR\(f_3\) (computed to infinite precision), rounded to the precision indicated by \(pc\) (and possibly FPSR.\(sf.pc\) and FPSR.\(sf.wre\)) using the rounding mode specified by FPSR.\(sf.rc\), and placed in FR\(f_1\).

If either FR\(f_3\) or FR\(f_2\) is a NaTVal, FR\(f_1\) is set to NaTVal instead of the computed result.

The mnemonic values for the opcode’s \(pc\) are given in Table 2-22 on page 3:50. The mnemonic values for \(sf\) are given in Table 2-23 on page 3:50. For the encodings and interpretation of the status field’s \(pc\), \(wre\), and \(rc\), refer to Table 5-6 and Table 5-5 on page 1:80.

Operation: See “fms — Floating-point Multiply Subtract” on page 3:78.
**fswap — Floating-point Swap**

**Format:**

(qp) fswap f1 = f2, f3

(qp) fswap.nl f1 = f2, f3

(qp) fswap.nr f1 = f2, f3

**Description:**

For the swap_form, the left single precision value in FR\(f_2\) is concatenated with the right single precision value in FR\(f_3\). The concatenated pair is then swapped.

For the swap_nl_form, the left single precision value in FR\(f_2\) is concatenated with the right single precision value in FR\(f_3\). The concatenated pair is then swapped, and the left single precision value is negated.

For the swap_nr_form, the left single precision value in FR\(f_2\) is concatenated with the right single precision value in FR\(f_3\). The concatenated pair is then swapped, and the right single precision value is negated.

For all forms, the exponent field of FR\(f_1\) is set to the biased exponent for 2.0\(^{63}\) (0x1003E) and the sign field of FR\(f_1\) is set to positive (0).

For all forms, if either FR\(f_2\) or FR\(f_3\) is a NaTVal, FR\(f_1\) is set to NaTVal instead of the computed result.

**Figure 2-18. Floating-point Swap**

![Diagram of Floating-point Swap](image1)

**Figure 2-19. Floating-point Swap Negate Left**

![Diagram of Floating-point Swap Negate Left](image2)

**Figure 2-20. Floating-point Swap Negate Right**

![Diagram of Floating-point Swap Negate Right](image3)
Operation:

```c
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f1] = NATVAL;
    } else {
        if (swap_form) {
            tmp_res_hi = FR[f3].significand{31:0};
            tmp_res_lo = FR[f3].significand{63:32};
        } else if (swap_nl_form) {
            tmp_res_hi = (!FR[f3].significand{31} << 31)
                | (FR[f3].significand{30:0});
            tmp_res_lo = FR[f3].significand{63:32};
        } else { // swap_nr_form
            tmp_res_hi = FR[f3].significand{31:0};
            tmp_res_lo = (!FR[f3].significand{63} << 31)
                | (FR[f3].significand{62:32});
        }
        FR[f1].significand = fp_concatenate(tmp_res_hi, tmp_res_lo);
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;
    }
    fp_update_psr(f1);
}
```

**FP Exceptions:** None

**Interruptions:** Illegal Operation fault, Disabled Floating-point Register fault
fsxt — Floating-point Sign Extend

Format:

\[(qp)\] \( fsxt.l\ f_1 = f_2, f_3 \) \hspace{0.5cm} \text{sxt\_l\_form \ F9} \n
\[(qp)\] \( fsxt.r\ f_1 = f_2, f_3 \) \hspace{0.5cm} \text{sxt\_r\_form \ F9} \n
Description:
For the sxt\_l\_form (sxt\_r\_form), the sign of the left (right) single precision value in FR\( f_2 \) is extended to 32-bits and is concatenated with the left (right) single precision value in FR\( f_3 \).

For all forms, the exponent field of FR\( f_1 \) is set to the biased exponent for \( 2.0^{63} \) (0x1003E) and the sign field of FR\( f_1 \) is set to positive (0).

For all forms, if either FR\( f_2 \) or FR\( f_3 \) is a NaTVal, FR\( f_1 \) is set to NaTVal instead of the computed result.

Operation:

\[
\text{if } (\text{PR[qp]}) \{ \\
\quad \text{fp\_check\_target\_register}(f_1); \\
\quad \text{if } (\text{tmp\_isrcode} = \text{fp\_reg\_disabled}(f_1, f_2, f_3, 0)) \\
\quad\quad \text{disabled\_fp\_register\_fault(tmp\_isrcode, 0);} \\
\quad \text{if } (\text{fp\_is\_natval}(\text{FR}[f_2]) || \text{fp\_is\_natval}(\text{FR}[f_3])) \{ \\
\quad\quad \text{FR}[f_1] = \text{NATVAL}; \\
\quad\quad \text{else } \{ \\
\quad\quad\quad \text{if } (\text{sxt\_l\_form}) \{ \\
\quad\quad\quad\quad \text{tmp\_res\_hi} = (\text{FR}[f_2].\text{significand}(63) ? 0xFFFFFFFF : 0x00000000); \\
\quad\quad\quad\quad \text{tmp\_res\_lo} = \text{FR}[f_3].\text{significand}(63:32); \\
\quad\quad\quad\quad \} \text{ else } \{ \\
\quad\quad\quad\quad \text{tmp\_res\_hi} = (\text{FR}[f_2].\text{significand}(31) ? 0xFFFFFFFF : 0x00000000); \\
\quad\quad\quad\quad \text{tmp\_res\_lo} = \text{FR}[f_3].\text{significand}(31:0); \\
\quad\quad\quad\} \\
\quad\quad \text{FR}[f_1].\text{significand} = \text{fp\_concatenate(tmp\_res\_hi, tmp\_res\_lo);} \\
\quad\quad \text{FR}[f_1].\text{exponent} = \text{FP\_INTEGER\_EXP}; \\
\quad\quad \text{FR}[f_1].\text{sign} = \text{FP\_SIGN\_POSITIVE}; \\
\quad\quad \} \\
\quad \} \\
\quad \text{fp\_update\_psr}(f_1); \\
\}\n
FP Exceptions: None

Interruptions: Illegal Operation fault \hspace{1cm} Disabled Floating-point Register fault
fwb — Flush Write Buffers

Format: \((qp)\) fwb

Description: The processor is instructed to expedite flushing of any pending stores held in write or coalescing buffers. Since this operation is a hint, the processor may or may not take any action and actually flush any outstanding stores. The processor gives no indication when flushing of any prior stores is completed. An fwb instruction does not ensure ordering of stores, since later stores may be flushed before prior stores.

To ensure prior coalesced stores are made visible before later stores, software must issue a release operation between stores (see Table 4-14 on page 2:70 for a list of release operations).

This instruction can be used to help ensure stores held in write or coalescing buffers are not delayed for long periods or to expedite high priority stores out of the processors.

Operation: \(\text{if (PR[qp]) } \{
\text{mem_flush_pending_stores();}
\})\)

Interruptions: None
fxor — Floating-point Exclusive Or

Format:  \((qp)\ fxor f_1 = f_2 \oplus f_3\)

Description:  The bit-wise logical exclusive-OR of the significand fields of \(f_2\) and \(f_3\) is computed. The resulting value is stored in the significand field of \(f_1\). The exponent field of \(f_1\) is set to the biased exponent for \(2.063\) (0x1003E) and the sign field of \(f_1\) is set to positive (0).

If either of \(f_2\) or \(f_3\) is a NaTVal, \(f_1\) is set to NaTVal instead of the computed result.

Operation:

```
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, f3, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (fp_is_natval(FR[f2]) || fp_is_natval(FR[f3])) {
        FR[f2] = NATVAL;
    } else {
        FR[f1].significand = FR[f2].significand \(^\oplus\) FR[f3].significand;
        FR[f1].exponent = FP_INTEGER_EXP;
        FR[f1].sign = FP_SIGN_POSITIVE;
    }

    fp_update_psr(f1);
}
```

FP Exceptions: None

Interruptions:  Illegal Operation fault  Disabled Floating-point Register fault
getf — Get Floating-point Value or Exponent or Significand

Format:

\[
\begin{align*}
(qp) \ text{getf.s} & \quad r_1 = f_2 \\
(qp) \ text{getf.d} & \quad r_1 = f_2 \\
(qp) \ text{getf.exp} & \quad r_1 = f_2 \\
(qp) \ text{getf.sig} & \quad r_1 = f_2
\end{align*}
\]

Description: In the single and double forms, the value in FR \( f_2 \) is converted into a single precision (single_form) or double precision (double_form) memory representation and placed in GR \( r_1 \), as shown in Figure 5-4 on page 1:82 and Figure 5-5 on page 1:83, respectively. In the single_form, the most-significant 32 bits of GR \( r_1 \) are set to 0.

In the exponent_form, the exponent field of FR \( f_2 \) is copied to bits 16:0 of GR \( r_1 \) and the sign bit of the value in FR \( f_2 \) is copied to bit 17 of GR \( r_1 \). The most-significant 46-bits of GR \( r_1 \) are set to zero.

Figure 2-23. Function of getf.exp

![Diagram of getf.exp]

In the significand_form, the significand field of the value in FR \( f_2 \) is copied to GR \( r_1 \)

Figure 2-24. Function of getf.sig

![Diagram of getf.sig]

For all forms, if FR \( f_2 \) contains a NaTVal, then the NaT bit corresponding to GR \( r_1 \) is set to 1.

Operation:

\[
\begin{align*}
&\text{if (PR[qp])} \\
&\quad \text{check_target_register}(r_1); \\
&\quad \text{if (tmp_isrcode = fp_reg_disabled(f_2, 0, 0, 0))} \\
&\quad\quad \text{disabled_fp_register_fault(tmp_isrcode, 0);} \\
&\quad \text{if (single_form)} \\
&\quad\quad \text{GR}[r_1][31:0] = \text{fp_fr_to_mem_format}(FR[f_2], 4, 0); \\
&\quad\quad\text{GR}[r_1][63:32] = 0; \\
&\quad\text{else if (double_form)} \\
&\quad\quad \text{GR}[r_1] = \text{fp_fr_to_mem_format}(FR[f_2], 8, 0); \\
&\quad\text{else if (exponent_form)} \\
&\quad\quad \text{GR}[r_1][63:18] = 0; \\
&\quad\quad \text{GR}[r_1][16:0] = FR[f_2].\text{exponent}; \\
&\quad\quad \text{GR}[r_1][17] = FR[f_2].\text{sign}; \\
&\quad\text{else // significand_form} \\
&\quad\quad \text{GR}[r_1] = FR[f_2].\text{significand};
\end{align*}
\]
if (fp_is_natval(FR[f2]))
    GR[r2].nat = 1;
else
    GR[r2].nat = 0;
}

**Interuptions:**  Illegal Operation fault

Disabled Floating-point Register fault
hint — Performance Hint

Format:

- \((qp)\) hint \((imm_{21})\)  
- \((qp)\) hint.i \((imm_{21})\)  
- \((qp)\) hint.b \((imm_{21})\)  
- \((qp)\) hint.m \((imm_{21})\)  
- \((qp)\) hint.f \((imm_{21})\)  
- \((qp)\) hint.x \((imm_{62})\)

Description: Provides a performance hint to the processor about the program being executed. It has no effect on architectural machine state, and operates as a \textit{nop} instruction except for its performance effects.

The immediate, \(imm_{21}\) or \(imm_{62}\), specifies the hint. For the \(x\_unit\_form\), the L slot of the bundle contains the upper 41 bits of \(imm_{62}\).

This instruction has five forms, each of which can be executed only on a particular execution unit type. The pseudo-op can be used if the unit type to execute on is unimportant.

Table 2-31. Hint Immediates

<table>
<thead>
<tr>
<th>(imm_{21}) or (imm_{62})</th>
<th>Mnemonic</th>
<th>Hint</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>@pause</td>
<td>Indicates to the processor that the currently executing stream is waiting, spinning, or doing low priority tasks. This hint can be used by the processor to allocate more resources or time to another executing stream on the same processor.</td>
</tr>
<tr>
<td>0x01-0x3f</td>
<td></td>
<td>These values are available for future architected extensions and will execute as a \textit{nop} on all current processors. Use of these values may cause unexpected performance issues on future processors and should not be used.</td>
</tr>
</tbody>
</table>

Operation:

```c
if (PR[qp]) {
    if (x_unit_form)
        hint = imm_{62};
    else // i_unit_form || b_unit_form || m_unit_form || f_unit_form
        hint = imm_{21};

    if (is_supported_hint(hint))
        execute_hint(hint);
}
```

Interruptions: None
invala — Invalidate ALAT

Format:  

```
(qp) invala

(qp) invala.e r_f

(qp) invala.e f_f
```

Description:  The selected entry or entries in the ALAT are invalidated.

In the complete_form, all ALAT entries are invalidated. In the entry_form, the ALAT is queried using the general register specifier \( r_f \) (gr_form), or the floating-point register specifier \( f_f \) (fr_form), and if any ALAT entry matches, it is invalidated.

Operation:  

```
if (PR[qp]) {
    if (complete_form)
        alat_inval();
    else { // entry_form
        if (gr_form)
            alat_inval_single_entry(GENERAL, r_f);
        else // fr_form
            alat_inval_single_entry(FLOAT, f_f);
    }
}
```

Interruptions:  None
**itc — Insert Translation Cache**

**Format:**

\[
\begin{align*}
&q \textit{itc.i} \, r_2 \quad \text{instruction_form} \quad M41 \\
&q \textit{itc.d} \, r_2 \quad \text{data_form} \quad M41
\end{align*}
\]

**Description:** An entry is inserted into the instruction or data translation cache. GR \(r_2\) specifies the physical address portion of the translation. ITIR specifies the protection key, page size and additional information. The virtual address is specified by the IFA register and the region register is selected by IFA\{63:61\}. The processor determines which entry to replace based on an implementation-specific replacement algorithm.

The visibility of the `itc` instruction to externally generated purges (ptc.q, ptc.ga) must occur before subsequent memory operations. From a software perspective, this is similar to acquire semantics. Serialization is still required to observe the side-effects of a translation being present.

`itc` must be the last instruction in an instruction group; otherwise, its behavior (including its ordering semantics) is undefined.

The TLB is first purged of any overlapping entries as specified by Table 4-1 on page 2:43.

This instruction can only be executed at the most privileged level, and when PSR.ic is zero.

To ensure forward progress, software must ensure that PSR.ic remains 0 until `rfi-ing` to the instruction that requires the translation.

**Operation:**

\[
\begin{align*}
\text{if} \quad & (\text{PR}[qp]) \quad \{ \\
& \text{if} \quad (!\text{followed_by_stop()}) \\
& \quad \text{undefined_behavior();} \\
& \text{if} \quad (\text{PSR.ic}) \quad \text{illegal_operation_fault();} \\
& \text{if} \quad (\text{PSR.cpl} \neq 0) \quad \text{privileged_operation_fault(0);} \\
& \text{if} \quad (\text{GR}[r_2].\text{nat}) \quad \text{register_nat_consumption_fault(0);} \\
\} \\
\text{tmp_size} &= \text{CR[ITIR].ps;} \\
\text{tmp_va} &= \text{CR[IFA]}\{60:0\}; \\
\text{tmp_rid} &= \text{RR[CR[IFA]}\{63:61\}]\{.rid; \\
\text{tmp_va} &= \text{align_to_size_boundary(tmp_va, tmp_size);} \\
& \text{if} \quad (\text{is_reserved_field(TLB_TYPE, GR[r_2], CR[ITIR])}) \\
& \quad \text{reserved_register_field_fault();} \\
& \text{if} \quad (\text{unimplemented_virtual_address(CR[IFA])}) \\
& \quad \text{unimplemented_data_address_fault(0);} \\
& \text{if} \quad \text{(instruction_form)} \{ \\
& \quad \text{tlb_must_purge_itc_entries(tmp_rid, tmp_va, tmp_size);} \\
& \quad \text{tlb_may_purge_dtc_entries(tmp_rid, tmp_va, tmp_size);} \\
& \quad \text{slot} = \text{tlb_replacement_algorithm(ITC_TYPE);} \\
& \quad \text{tlb_insert_inst(slot, GR[r_2], CR[ITIR], CR[IFA], tmp_rid, TC);} \\
& \} \quad \text{else} \quad \{ \text{// data_form} \\
& \quad \text{tlb_must_purge_dtc_entries(tmp_rid, tmp_va, tmp_size);} \\
& \quad \text{tlb_may_purge_itc_entries(tmp_rid, tmp_va, tmp_size);} \\
& \quad \text{slot} = \text{tlb_replacement_algorithm(DTC_TYPE);} \\
& \quad \text{tlb_insert_data(slot, GR[r_2], CR[ITIR], CR[IFA], tmp_rid, TC);} \\
& \}
\end{align*}
\]
**Interrupts:**
- Machine Check abort
- Illegal Operation fault
- Privileged Operation fault
- Register NaT Consumption fault
- Reserved Register/Field fault
- Unimplemented Data Address fault

**Serialization:** For the instruction_form, software must issue an instruction serialization operation before a dependent instruction fetch access. For the data_form, software must issue a data serialization operation before issuing a data access or non-access reference dependent on the new translation.
itr — Insert Translation Register

Format:  

\[
\begin{align*}
(qp) \text{itr} & : \text{itr}[r_3] = r_2, & \text{instruction form} & : M42 \\
(qp) \text{itr.d} & : \text{dtr}[r_3] = r_2, & \text{data form} & : M42
\end{align*}
\]

Description:  

A translation is inserted into the instruction or data translation register specified by the contents of GR \(r_3\). GR \(r_2\) specifies the physical address portion of the translation. ITIR specifies the protection key, page size and additional information. The virtual address is specified by the IFA register and the region register is selected by IFA\{63:61\}.

As described in Table 4-1, “Purge Behavior of TLB Instructions” on page 243, the TLB is first purged of any entries that overlap with the newly inserted translation. The translation previously contained in the TR slot specified by GR \(r_3\) is not necessarily purged from the processor's TLBs and may remain as a TC entry. To ensure that the previous TR translation is purged, software must use explicit ptr instructions before inserting the new TR entry.

This instruction can only be executed at the most privileged level, and when PSR.ic is zero.

Operation:  

\[
\begin{align*}
\text{if} \ (\text{PR}[qp]) \ {\{}
\text{if} \ (\text{PSR.ic}) \\
\text{illegal_operation_fault();}
\text{if} \ (\text{PSR.cpl} != 0) \\
\text{privileged_operation_fault();}
\text{if} \ (\text{GR}[r_3].nat || \text{GR}[r_2].nat) \\
\text{register_nat_consumption_fault();}
\end{align*}
\]

\[
\begin{align*}
\text{slot} & = \text{GR}[r_3]\{7:0\}; \\
\text{tmp_size} & = \text{CR}[ITIR].ps; \\
\text{tmp_va} & = \text{CR}[IFA]\{60:0\}; \\
\text{tmp_rid} & = \text{RR}[\text{CR}[IFA]\{63:61\}].rid; \\
\text{tmp_va} & = \text{align_to_size_boundary(tmp_va, tmp_size);}
\end{align*}
\]

\[
\begin{align*}
\text{tmp_tr_type} & = \text{instruction_form ? ITR_TYPE : DTR_TYPE;}
\text{if} \ (\text{is_reserved_reg(tmp_tr_type, slot})) \\
\text{reserved_register_field_fault();}
\text{if} \ (\text{is_reserved_field(TLB_TYPE, GR[r_3], CR[ITIR]))} \\
\text{reserved_register_field_fault();}
\text{if} \ (\text{unimplemented_virtual_address(CR[IFA]))} \\
\text{unimplemented_data_address_fault();}
\text{if} \ (\text{instruction_form}) \ {\{}
\text{tlb_must_purge_itc_entries(tmp_rid, tmp_va, tmp_size);}
\text{tlb_may_purge_dtc_entries(tmp_rid, tmp_va, tmp_size);}
\text{tlb_insert_inst(slot, GR[r_2], CR[ITIR], CR[IFA], tmp_rid, TR);}
\text{\}} \ \text{else} \ {\{}
\text{tlb_must_purge_dtc_entries(tmp_rid, tmp_va, tmp_size);}
\text{tlb_may_purge_itc_entries(tmp_rid, tmp_va, tmp_size);}
\text{tlb_insert_data(slot, GR[r_2], CR[ITIR], CR[IFA], tmp_rid, TR);}
\text{\}}
\end{align*}
\]

Interruptions:  

Machine Check abort  
Reserved Register/Field fault  
Illegal Operation fault  
Unimplemented Data Address fault  
Privileged Operation fault  
Register NaT Consumption fault
Serialization: For the instruction_form, software must issue an instruction serialization operation before a dependent instruction fetch access. For the data_form, software must issue a data serialization operation before issuing a data access or non-access reference dependent on the new translation.

Notes: The processor may use invalid translation registers for translation cache entries. Performance can be improved on some processor models by ensuring translation registers are allocated beginning at translation register zero and continuing contiguously upwards.
ld — Load

Format:

\[
\begin{align*}
(qp) \ ldz.ldtype.ldhint \ r_j &= [r_3] \\
(qp) \ ldz.ldtype.ldhint \ r_j &= [r_3], r_2 \\
(qp) \ ldz.ldtype.ldhint \ r_j &= [r_3], imm_9 \\
(qp) \ ld16. ldhint \ r_1, ar.csд &= [r_3] \\
(qp) \ ld16.acq. ldhint \ r_1, ar.csд &= [r_3] \\
(qp) \ ld8.fill. ldhint \ r_1 &= [r_3], r_2 \\
(qp) \ ld8.fill. ldhint \ r_1 &= [r_3], imm_9
\end{align*}
\]

Description:

A value consisting of \( sz \) bytes is read from memory starting at the address specified by the value in GR \( r_3 \). The value is then zero extended and placed in GR \( r_1 \). The values of the \( sz \) completer are given in Table 2-32. The NaT bit corresponding to GR \( r_1 \) is cleared, except as described below for speculative loads. The \( ldtype \) completer specifies special load operations, which are described in Table 2-33.

For the sixteen_byte_form, two 8-byte values are loaded as a single, 16-byte memory read. The value at the lowest address is placed in GR \( r_1 \), and the value at the highest address is placed in the Compare and Store Data application register (AR[CSД]). The only load types supported for this sixteen_byte_form are none and acq.

For the fill_form, an 8-byte value is loaded, and a bit in the UNAT application register is copied into the target register NaT bit. This instruction is used for reloading a spilled register/NaT pair. See Section 4.4.4, “Control Speculation” on page 1:51 for details.

In the base update forms, the value in GR \( r_3 \) is added to either a signed immediate value (imm_9) or a value from GR \( r_2 \), and the result is placed back in GR \( r_3 \). This base register update is done after the load, and does not affect the load address. In the reg_base_update_form, if the NaT bit corresponding to GR \( r_2 \) is set, then the NaT bit corresponding to GR \( r_3 \) is set and no fault is raised. Base register update is not supported for the ld16 instruction.

Table 2-32. \( sz \) Completers

<table>
<thead>
<tr>
<th>( sz ) Completer</th>
<th>Bytes Accessed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 byte</td>
</tr>
<tr>
<td>2</td>
<td>2 bytes</td>
</tr>
<tr>
<td>4</td>
<td>4 bytes</td>
</tr>
<tr>
<td>8</td>
<td>8 bytes</td>
</tr>
</tbody>
</table>

Table 2-33. Load Types

<table>
<thead>
<tr>
<th>( ldtype ) Completer</th>
<th>Interpretation</th>
<th>Special Load Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Normal load</td>
<td></td>
</tr>
<tr>
<td>s</td>
<td>Speculative load</td>
<td>Certain exceptions may be deferred rather than generating a fault. Deferral causes the target register’s NaT bit to be set. The NaT bit is later used to detect deferral.</td>
</tr>
<tr>
<td>a</td>
<td>Advanced load</td>
<td>An entry is added to the ALAT. This allows later instructions to check for colliding stores. If the referenced data page has a non-speculative attribute, the target register and NaT bit is cleared, and the processor ensures that no ALAT entry exists for the target register. The absence of an ALAT entry is later used to detect deferral or collision.</td>
</tr>
</tbody>
</table>
For more details on ordered, biased, speculative, advanced and check loads see Section 4.4.4, “Control Speculation” on page 1:51 and Section 4.4.5, “Data Speculation” on page 1:55. For more details on ordered loads see Section 4.4.7, “Memory Access Ordering” on page 1:63. See Section 4.4.6, “Memory Hierarchy Control and Consistency” on page 1:60 for details on biased loads. Details on memory attributes are described in Section 4.4, “Memory Attributes” on page 2:63.

For the non-speculative load types, if NaT bit associated with GR \( r_3 \) is 1, a Register NaT Consumption fault is taken. For speculative and speculative advanced loads, no fault is raised, and the exception is deferred. For the base-update calculation, if the NaT bit associated with GR \( r_2 \) is 1, the NaT bit associated with GR \( r_3 \) is set to 1 and no fault is raised.

The value of the \( ldhint \) completer specifies the locality of the memory access. The values of the \( ldhint \) completer are given in Table 2-34. A prefetch hint is implied in the base update forms. The address specified by the value in GR \( r_3 \) after the base update acts as a hint to prefetch the indicated cache line. This prefetch uses the locality hints specified by \( ldhint \). Prefetch and locality hints do not affect program functionality and may be ignored by the implementation. See Section 4.4.6, “Memory Hierarchy Control and Consistency” on page 1:60 for details.

### Table 2-34. Load Hints

<table>
<thead>
<tr>
<th>( ldhint ) Completer</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Temporal locality, level 1</td>
</tr>
<tr>
<td>nt1</td>
<td>No temporal locality, level 1</td>
</tr>
<tr>
<td>nta</td>
<td>No temporal locality, all levels</td>
</tr>
</tbody>
</table>
In the no_base_update form, the value in GR\textit{r3} is not modified and no prefetch hint is implied. For the base update forms, specifying the same register address in \textit{r1} and \textit{r3} will cause an Illegal Operation fault.

Hardware support for \texttt{ld16} instructions that reference a page that is neither a cacheable page with write-back policy nor a NaTPage is optional. On processor models that do not support such \texttt{ld16} accesses, an Unsupported Data Reference fault is raised when an unsupported reference is attempted.

**Operation:**

```c
if (PR[qp]) {
    size = fill_form ? 8 : (sixteen_byte_form ? 16 : sz);
    speculative = (ldtype == 's' || ldtype == 'sa');
    advanced = (ldtype == 'a' || ldtype == 'sa');
    check_clear = (ldtype == 'c.clr' || ldtype == 'c.clr.acq');
    check_no_clear = (ldtype == 'c.nc');
    check = check_clear || check_no_clear;
    check_target_register(r3);
    if (reg_base_update_form || imm_base_update_form) {
        illegal_operation_fault();
        check_target_register(r3);
    }
    if (reg_base_update_form) {
        tmp_r2 = GR[r2];
        tmp_r2nat = GR[r2].nat;
    }
    if (!speculative && GR[r3].nat) // fault on NaT address
        register_nat_consumption_fault(itype);
    if (check && alat_cmp(GENERAL, r1)) { // no load on ld.c & ALAT hit
        if (check_clear) // remove entry on ld.c.clr or ld.c.clr.acq
            alat_inval_single_entry(GENERAL, r1);
    }
}
```

```c
if (!defer) {
    if (size == 16) {
        mem_read_pair(&val, &val_ar, paddr, size, UM.be, mattr, otype, ldhint);
    }
    else {
        val = mem_read(paddr, size, UM.be, mattr, otype, ldhint);
    }
}
```
if (check_clear || advanced) // remove any old ALAT entry
    alat_inval_single_entry(GENERAL, r1);
if (defer) {
    if (speculative) {
        GR[r1] = natd_gr_read(paddr, size, UM.be, mattr, otype,
            bias | ldhint);
        GR[r1].nat = 1;
    } else {
        GR[r1] = 0; // ld.a to sequential memory
        GR[r1].nat = 0;
    }
} else { // execute load normally
    if (fill_form) { // fill NaT on ld8.fill
        bit_pos = GR[r3]{8:3};
        GR[r1] = val;
        GR[r1].nat = AR[UNAT]{bit_pos};
    } else { // clear NaT on other types
        if (size == 16) {
            GR[r1] = val;
            AR[CSD] = val_ar;
        } else {
            GR[r1] = zero_ext(val, size * 8);
        }
        GR[r1].nat = 0;
    }
    if ((check_no_clear || advanced) && ma_is_speculative(mattr))
        // add entry to ALAT
        alat_write(GENERAL, r1, paddr, size);
}
if (imm_base_update_form) { // update base register
    GR[r3] = GR[r3] + sign_ext(imm9, 9);
    GR[r3].nat = GR[r3].nat;
} else if (reg_base_update_form) {
    GR[r3] = GR[r3] + tmp_r2;
    GR[r3].nat = GR[r3].nat | tmp_r2nat;
}
if ((reg_base_update_form || imm_base_update_form) && !GR[r3].nat)
    mem_implicit_prefetch(GR[r3], ldhint | bias, itype);

**Interruptions:**

- Illegal Operation fault
- Register NaT Consumption fault
- Unimplemented Data Address fault
- Data Nested TLB fault
- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault
- Data NaT Page Consumption fault
- Data Key Miss fault
- Data Key Permission fault
- Data Access Rights fault
- Data Access Bit fault
- Data Debug fault
- Unaligned Data Reference fault
- Unsupported Data Reference fault
Idf — Floating-point Load

Format:

- `(ap) ldffsz fldtype ldhint f1 = [r3]`  
  - no_base_update_form M6
- `(ap) ldffsz fldtype ldhint f1 = [r3], r2`  
  - reg_base_update_form M7
- `(ap) ldffsz fldtype ldhint f1 = [r3], imm9`  
  - imm_base_update_form M8
- `(ap) ldffs.fldtype ldhint f1 = [r3]`  
  - integer_form, no_base_update_form M6
- `(ap) ldffs.fldtype ldhint f1 = [r3], r2`  
  - integer_form, reg_base_update_form M7
- `(ap) ldffs.fldtype ldhint f1 = [r3], imm9`  
  - integer_form, imm_base_update_form M8
- `(ap) ldff.fill ldhint f1 = [r3]`  
  - fill_form, no_base_update_form M6
- `(ap) ldff.fill ldhint f1 = [r3], r2`  
  - fill_form, reg_base_update_form M7
- `(ap) ldff.fill ldhint f1 = [r3], imm9`  
  - fill_form, imm_base_update_form M8

Description: A value consisting of `fsz` bytes is read from memory starting at the address specified by the value in GR `r3`. The value is then converted into the floating-point register format and placed in FR `f1`. See Section 5.1, “Data Types and Formats” on page 1:75 for details on conversion to floating-point register format. The values of the `fsz` completer are given in Table 2-35. The `fldtype` completer specifies special load operations, which are described in Table 2-36.

For the integer_form, an 8-byte value is loaded and placed in the significand field of FR `f1` without conversion. The exponent field of FR `f1` is set to the biased exponent for 2.0(13) (0x1003E) and the sign field of FR `f1` is set to positive (0).

For the fill_form, a 16-byte value is loaded, and the appropriate fields are placed in FR `f1` without conversion. This instruction is used for reloading a spilled register. See Section 4.4.4, “Control Speculation” on page 1:51 for details.

In the base update forms, the value in GR `r3` is added to either a signed immediate value (imm9) or a value from GR `r2`, and the result is placed back in GR `r3`. This base register update is done after the load, and does not affect the load address. In the reg_base_update_form, if the NaT bit corresponding to GR `r2` is set, then the NaT bit corresponding to GR `r3` is set and no fault is raised.

Table 2-35. `fsz` Completers

<table>
<thead>
<tr>
<th><code>fsz</code> Completer</th>
<th>Bytes Accessed</th>
<th>Memory Format</th>
</tr>
</thead>
<tbody>
<tr>
<td>s</td>
<td>4 bytes</td>
<td>Single precision</td>
</tr>
<tr>
<td>d</td>
<td>8 bytes</td>
<td>Double precision</td>
</tr>
<tr>
<td>e</td>
<td>10 bytes</td>
<td>Extended precision</td>
</tr>
</tbody>
</table>

Table 2-36. FP Load Types

<table>
<thead>
<tr>
<th><code>fldtype</code> Completer</th>
<th>Interpretation</th>
<th>Special Load Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Normal load</td>
<td>Certain exceptions may be deferred rather than generating a fault. Deferral causes NaTVal to be placed in the target register. The NaTVal value is later used to detect deferral.</td>
</tr>
<tr>
<td>s</td>
<td>Speculative load</td>
<td>An entry is added to the ALAT. This allows later instructions to check for colliding stores. If the referenced data page has a non-speculative attribute, no ALAT entry is added to the ALAT and the target register is set as follows: for the integer_form, the exponent is set to 0x1003E and the sign and significand are set to zero; for all other forms, the sign, exponent and significand are set to zero. The absence of an ALAT entry is later used to detect deferral or collision.</td>
</tr>
<tr>
<td>a</td>
<td>Advanced load</td>
<td>An entry is added to the ALAT, and certain exceptions may be deferred. Deferral causes NaTVal to be placed in the target register, and the processor ensures that no ALAT entry exists for the target register. The absence of an ALAT entry is later used to detect deferral or collision.</td>
</tr>
<tr>
<td>sa</td>
<td>Speculative Advanced load</td>
<td>An entry is added to the ALAT, and certain exceptions may be deferred. Deferral causes NaTVal to be placed in the target register, and the processor ensures that no ALAT entry exists for the target register. The absence of an ALAT entry is later used to detect deferral or collision.</td>
</tr>
</tbody>
</table>
For more details on speculative, advanced and check loads see Section 4.4.4, “Control Specification” on page 1:51 and Section 4.4.5, “Data Specification” on page 1:55. Details on memory attributes are described in Section 4.4, “Memory Attributes” on page 2:63.

For the non-speculative load types, if NaT bit associated with GR \( r_3 \) is 1, a Register NaT Consumption fault is taken. For speculative and speculative advanced loads, no fault is raised, and the exception is deferred. For the base-update calculation, if the NaT bit associated with GR \( r_2 \) is 1, the NaT bit associated with GR \( r_3 \) is set to 1 and no fault is raised.

The value of the \( \text{ldhint} \) modifier specifies the locality of the memory access. The mnemonic values of \( \text{ldhint} \) are given in Table 2-34 on page 3:132. A prefetch hint is implied in the base update forms. The address specified by the value in GR \( r_3 \) after the base update acts as a hint to prefetch the indicated cache line. This prefetch uses the locality hints specified by \( \text{ldhint} \). Prefetch and locality hints do not affect program functionality and may be ignored by the implementation. See Section 4.4.6, “Memory Hierarchy Control and Consistency” on page 1:60 for details.

In the no_base_update form, the value in GR \( r_3 \) is not modified and no prefetch hint is implied.

The PSR.mfl and PSR.mfh bits are updated to reflect the modification of FR \( f_j \).

Hardware support for \( \text{ldfe} \) (10-byte) instructions that reference a page that is neither a cacheable page with write-back policy nor a NaTPage is optional. On processor models that do not support such \( \text{ldfe} \) accesses, an Unsupported Data Reference fault is raised when an unsupported reference is attempted. The fault is delivered only on the normal, advanced, and check load flavors. Control-speculative flavors of \( \text{ldfe} \) always defer the Unsupported Data Reference fault.

### Operation:

```c
if (PR[qp]) {
    size = (fill_form ? 16 : (integer_form ? 8 : fsz));
    speculative = (fldtype == 's' || fldtype == 'sa');
    advanced = (fldtype == 'a' || fldtype == 'sa');
    check_clear = (fldtype == 'c.clr' );
    check_no_clear = (fldtype == 'c.nc');
    check = check_clear || check_no_clear;

    itype = READ;
    if (speculative) itype |= SPEC;
    if (advanced) itype |= ADVANCE;
    if (size == 10) itype |=UNCACHE_OPT;

    if (reg_base_update_form || imm_base_update_form)
        check_target_register(r3);
```
fp_check_target_register(f1);
if (tmp_isrcode = fp_reg_disabled(f1, 0, 0, 0))
  disabled_fp_register_fault(tmp_isrcode, itype);

if (!speculative && GR[r3].nat) // fault on NaT address
  register_nat_consumption_fault(itype);

defer = speculative && (GR[r3].nat || PSR.ed);// defer exception if spec

if (check && alat_cmp(FLOAT, f1)) { // no load on ldf.c & ALAT hit
  if (!defer) { // remove entry on ldf.c.clr
    alat_inval_single_entry(FLOAT, f1);
  } else {
    if (!defer) {
      paddr = tlb_translate(GR[r3], size, itype, PSR.cpl, &mattr, &defer);
      spontaneous_deferral(paddr, size, UM.be, mattr, UNORDERED, ldhint, &defer);
      if (!defer)
        val = mem_read(paddr, size, UM.be, mattr, UNORDERED, ldhint);
    } if (check_clear || advanced) { // remove any old ALAT entry
      alat_inval_single_entry(FLOAT, f1);
    } if (speculative && defer) {
      FR[f1] = NATVAL;
    } else if (advanced && !speculative && defer) {
      FR[f1] = (integer_form ? FP_INT_ZERO : FP_ZERO);
    } else {
      // execute load normally
      FR[f1] = fp_mem_to_fr_format(val, size, integer_form);
      if (!defer)
        val = mem_read(paddr, size, UM.be, mattr, UNORDERED, ldhint);
    } if (check_clear || advanced && ma_is_speculative(mattr)) // add entry to ALAT
      alat_write(FLOAT, f1, paddr, size);
  }
}

if (imm_base_update_form) { // update base register
  GR[r3] = GR[r3] + sign_ext(imm9, 9);
  GR[r3].nat = GR[r3].nat;
} else if (reg_base_update_form) {
  GR[r3] = GR[r3] + GR[r2];
  GR[r3].nat = GR[r3].nat || GR[r2].nat;
}

if ((reg_base_update_form || imm_base_update_form) && !GR[r3].nat)
  mem_implicit_prefetch(GR[r3], ldhint, itype);

fp_update_psr(f1);

Interruptions:
Illegal Operation fault
Disabled Floating-point Register fault
Register NaT Consumption fault
Unimplemented Data Address fault
Data Nested TLB fault
Alternate Data TLB fault
VHPT Data fault
Data TLB fault
Data Page Not Present fault
Data NaT Page Consumption fault
Data Key Miss fault
Data Key Permission fault
Data Access Rights fault
Data Access Bit fault
Data Debug fault
Unaligned Data Reference fault
Unsupported Data Reference fault
ldfp — Floating-point Load Pair

Format:

(qp) ldfps, fldtype, ldhint f1, f2 = [r3] single_form, no_base_update_form M11
(qp) ldfps, fldtype, ldhint f1, f2 = [r3], 8 single_form, base_update_form M12
(qp) ldfpd, fldtype, ldhint f1, f2 = [r3] double_form, no_base_update_form M11
(qp) ldfpd, fldtype, ldhint f1, f2 = [r3], 16 double_form, base_update_form M12
(qp) ldfp8, fldtype, ldhint f1, f2 = [r3] integer_form, no_base_update_form M11
(qp) ldfp8, fldtype, ldhint f1, f2 = [r3], 16 integer_form, base_update_form M12

Description: Eight (single_form) or sixteen (double_form/integer_form) bytes are read from memory starting at the address specified by the value in GR r3. The value read is treated as a contiguous pair of floating-point numbers for the single_form/double_form and as integer/Parallel FP data for the integer_form. Each number is converted into the floating-point register format. The value at the lowest address is placed in FR f1, and the value at the highest address is placed in FR f2. See Section 5.1, “Data Types and Formats” on page 1:75 for details on conversion to floating-point register format. The fldtype completer specifies special load operations, which are described in Table 2-36 on page 3:135.

For more details on speculative, advanced and check loads see Section 4.4.4, “Control Speculation” on page 1:51 and Section 4.4.5, “Data Speculation” on page 1:55.

For the non-speculative load types, if NaT bit associated with GR r3 is 1, a Register NaT Consumption fault is taken. For speculative and speculative advanced loads, no fault is raised, and the exception is deferred.

In the base_update_form, the value in GR r3 is added to an implied immediate value (equal to double the data size) and the result is placed back in GR r3. This base register update is done after the load, and does not affect the load address.

The value of the ldhint modifier specifies the locality of the memory access. The mnemonic values of ldhint are given in Table 2-34 on page 3:132. A prefetch hint is implied in the base update form. The address specified by the value in GR r3 after the base update acts as a hint to prefetch the indicated cache line. This prefetch uses the locality hints specified by ldhint. Prefetch and locality hints do not affect program functionality and may be ignored by the implementation. See Section 4.4.6, “Memory Hierarchy Control and Consistency” on page 1:60 for details.

In the no_base_update form, the value in GR r3 is not modified and no prefetch hint is implied.

The PSR.mfl and PSR.mfh bits are updated to reflect the modification of FR f1 and FR f2.

There is a restriction on the choice of target registers. Register specifiers f1 and f2 must specify one odd-numbered physical FR and one even-numbered physical FR. Specifying two odd or two even registers will cause an Illegal Operation fault to be raised. The restriction is on physical register numbers after register rotation. This means that if f1 and f2 both specify static registers or both specify rotating registers, then f1 and f2 must be odd/even or even/odd. If f1 and f2 specify one static and one rotating register, the restriction depends on CFM.rrb.fr. If CFM.rrb.fr is even, the restriction is the same; f1 and f2 must be odd/even or even/odd. If CFM.rrb.fr is odd, then f1 and f2 must be even/even or odd/odd. Specifying one static and one rotating register should only be done when CFM.rrb.fr will have a predictable value (such as 0).
Operation:
if (PR[qp]) {
    size = single_form ? 8 : 16;
    speculative = (fldtype == 's' || fldtype == 'sa');
    advanced = (fldtype == 'a' || fldtype == 'sa');
    check_clear = (fldtype == 'c.clr');
    check_no_clear = (fldtype == 'c.nc');
    check = check_clear || check_no_clear;
    itype = READ;
    if (speculative) itype |= SPEC;
    if (advanced) itype |= ADVANCE;
    if (fp_req_bank_conflict(f1, f2))
        illegal_operation_fault();
    if (base_update_form)
        check_target_register(r3);
    fp_check_target_register(f1);
    fp_check_target_register(f2);
    if (tmp_isrcode = fp_reg_disabled(f1, f2, 0, 0))
        disabled_fp_register_fault(tmp_isrcode, itype);
    if (!speculative && GR[r3].nat) // fault on NaT address
        register_nat_consumption_fault(itype);
    defer = speculative && (GR[r3].nat || PSR.ed); // defer exception if spec
    if (check && alat_cmp(FLOAT, f1)) { // no load on ldfp.c & ALAT hit
        if (check_clear) // remove entry on ldfp.c.clr
            alat_inval_single_entry(FLOAT, f1);
    } else {
        if (!defer) {
            paddr = tlb_translate(GR[r3], size, itype, PSR.cpl, &mattr,
                                 &defer);
            spontaneous_deferral(paddr, size, UM.be, mattr, UNORDERED,
                                 ldhint, &defer);
            if (!defer)
                mem_read_pair(&f1_val, &f2_val, paddr, size, UM.be,
                              mattr, UNORDERED, ldhint);
        }
    }
    if (check_clear || advanced) // remove any old ALAT entry
        alat_inval_single_entry(FLOAT, f1);
    if (speculative && defer) {
        FR[f1] = NATVAL;
        FR[f2] = NATVAL;
    } else if (advanced && !speculative && defer) {
        FR[f1] = (integer_form ? FP_INT_ZERO : FP_ZERO);
        FR[f2] = (integer_form ? FP_INT_ZERO : FP_ZERO);
    } else {
        // execute load normally
        FR[f1] = fp_mem_to_fr_format(f1_val, size/2, integer_form);
        FR[f2] = fp_mem_to_fr_format(f2_val, size/2, integer_form);
        if ((check_no_clear || advanced) && ma_is_speculative(mattr))
            // add entry to ALAT
            alat_write(FLOAT, f1, paddr, size);
    }
}
if (base_update_form) { // update base register
    GR[r3] = GR[r3] + size;
\begin{verbatim}
GR[r3].nat = GR[r3].nat;
if (!GR[r3].nat)
    mem_implicit_prefetch(GR[r3], ldhint, itype);

fp_update_psr(f1);
fp_update_psr(f2);
\end{verbatim}

**Interruptions:**
- Illegal Operation fault
- Disabled Floating-point Register fault
- Register NaT Consumption fault
- Unimplemented Data Address fault
- Data Nested TLB fault
- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault
- Data NaT Page Consumption fault
- Data Key Miss fault
- Data Key Permission fault
- Data Access Rights fault
- Data Access Bit fault
- Data Debug fault
- Unaligned Data Reference fault
Ifetch — Line Prefetch

Format:

\[(ap) \text{Ifetch.} lftype.lfhint [r_3] \quad \text{no_base_update_form} \quad \text{M13}\]
\[(ap) \text{Ifetch.} lftype.lfhint [r_3], r_2 \quad \text{reg_base_update_form} \quad \text{M14}\]
\[(ap) \text{Ifetch.} lftype.lfhint [r_3], \text{imm}_9 \quad \text{imm_base_update_form} \quad \text{M15}\]
\[(ap) \text{Ifetch.} \text{excl.} lftype.lfhint [r_3] \quad \text{no_base_update_form, exclusive_form} \quad \text{M13}\]
\[(ap) \text{Ifetch.} \text{excl.} lftype.lfhint [r_3], r_2 \quad \text{reg_base_update_form, exclusive_form} \quad \text{M14}\]
\[(ap) \text{Ifetch.} \text{excl.} lftype.lfhint [r_3], \text{imm}_9 \quad \text{imm_base_update_form, exclusive_form} \quad \text{M15}\]

Description:
The line containing the address specified by the value in GR \(r_3\) is moved to the highest level of the data memory hierarchy. The value of the \(lfhint\) modifier specifies the locality of the memory access; see Section 4.4, “Memory Access Instructions” on page 1:48 for details. The mnemonic values of \(lfhint\) are given in Table 2-38.

The behavior of the memory read is also determined by the memory attribute associated with the accessed page. See Chapter 4, “Addressing and Protection” in Volume 2. Line size is implementation dependent but must be a power of two greater than or equal to 32 bytes. In the exclusive form, the cache line is allowed to be marked in an exclusive state. This qualifier is used when the program expects soon to modify a location in that line. If the memory attribute for the page containing the line is not cacheable, then no reference is made.

The completer, \(lftype\), specifies whether or not the instruction raises faults normally associated with a regular load. Table 2-37 defines these two options.

Table 2-37. \(lftype\) Mnemonic Values

<table>
<thead>
<tr>
<th>(lftype) Mnemonic</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Ignore faults</td>
</tr>
<tr>
<td>fault</td>
<td>Raise faults</td>
</tr>
</tbody>
</table>

In the base update forms, after being used to address memory, the value in GR \(r_3\) is incremented by either the sign-extended value in \(\text{imm}_9\) (in the \(\text{imm_base_update_form}\)) or the value in GR \(r_2\) (in the \(\text{reg_base_update_form}\)). In the \(\text{reg_base_update_form}\), if the NaT bit corresponding to GR \(r_2\) is set, then the NaT bit corresponding to GR \(r_3\) is set – no fault is raised.

In the \(\text{reg_base_update_form}\) and the \(\text{imm_base_update_form}\), if the NaT bit corresponding to GR \(r_3\) is clear, then the address specified by the value in GR \(r_3\) after the post-increment acts as a hint to implicitly prefetch the indicated cache line. This implicit prefetch uses the locality hints specified by \(lfhint\). The implicit prefetch does not affect program functionality, does not raise any faults, and may be ignored by the implementation.

In the \(\text{no_base_update_form}\), the value in GR \(r_3\) is not modified and no implicit prefetch hint is implied.

If the NaT bit corresponding to GR \(r_3\) is set then the state of memory is not affected. In the \(\text{reg_base_update_form}\) and \(\text{imm_base_update_form}\), the post increment of GR \(r_3\) is performed and prefetch is hinted as described above.

\(\text{Ifetch}\) instructions, like hardware prefetches, are not orderable operations, i.e., they have no order with respect to prior or subsequent memory operations.
A faulting \texttt{lfetch} to an unimplemented address results in an Unimplemented Data Address fault. A non-faulting \texttt{lfetch} to an unimplemented address does not take the fault and will not issue a prefetch request, but, if specified, will perform a register post-increment.

Both the non-faulting and the faulting forms of \texttt{lfetch} can be used speculatively. The purpose of raising faults on the faulting form is to allow the operating system to resolve problems with the address to the extent that it can do so relatively quickly. If problems with the address cannot be resolved quickly, the OS simply returns to the program, and forces the data prefetch to be skipped over.

Specifically, if a faulting \texttt{lfetch} takes any of the listed faults (other than Illegal Operation fault), the operating system must handle this fault to the extent that it can do so relatively quickly and invisibly to the interrupted program. If the fault cannot be handled quickly or cannot be handled invisibly (e.g., if handling the fault would involve terminating the program), the OS must return to the interrupted program, skipping over the data prefetch. This can easily be done by setting the IPSR.ed bit to 1 before executing an \texttt{rfi} to go back to the process, which will allow the \texttt{lfetch.fault} to perform its base register post-increment (if specified), but will suppress any prefetch request and hence any prefetch-related fault. Note that the OS can easily identify that a faulting \texttt{lfetch} was the cause of the fault by observing that ISR.na is 1, and ISR.code\{3:0\} is 4. The one exception to this is the Illegal Operation fault, which can be caused by an \texttt{lfetch.fault} if base register post-increment is specified, and the base register is outside of the current stack frame, or is GR0. Since this one fault is not related to the prefetch aspect of \texttt{lfetch.fault}, but rather to the base update portion, Illegal Operation faults on \texttt{lfetch.fault} should be handled the same as for any other instruction.

**Operation:**

```c
if (PR[qp]) {
    itype = READ|NON_ACCESS;
    itype |= (lftype == 'fault') ? LFETCH_FAULT : LFETCH;

    if (reg_base_update_form || imm_base_update_form)
        check_target_register(r3);

    if (lftype == 'fault') { // faulting form
        if (GR[r3].nat && !PSR.ed) // fault on NaT address
            register_nat_consumption_fault(itype);
    }

    excl_hint = (exclusive_form) ? EXCLUSIVE : 0;

    if (!GR[r3].nat && !PSR.ed) // faulting form already faulted if r3 is nat
        paddr = tlb_translate(GR[r3], 1, itype, PSR.cpl, &mattr, &defer);
        if (!defer)
            mem_promote(paddr, mattr, lfhint | excl_hint);
    }

    if (imm_base_update_form) {
        GR[r3] = GR[r3] + sign_ext(imm9, 9);
        GR[r3].nat = GR[r3].nat;
    } else if (reg_base_update_form) {
```

<table>
<thead>
<tr>
<th>\textit{lfhint Mnemonic}</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Temporal locality, level 1</td>
</tr>
<tr>
<td>nt1</td>
<td>No temporal locality, level 1</td>
</tr>
<tr>
<td>nt2</td>
<td>No temporal locality, level 2</td>
</tr>
<tr>
<td>nta</td>
<td>No temporal locality, all levels</td>
</tr>
</tbody>
</table>
GR[r_3] = GR[r_3] + GR[r_2];
GR[r_3].nat = GR[r_2].nat || GR[r_3].nat;
}

if ((reg_base_update_form || imm_base_update_form) && !GR[r_3].nat)
    mem_implicit_prefetch(GR[r_3], lfhint | excl_hint, itype);

Interruptions:
Illegal Operation fault
Register NaT Consumption fault
Unimplemented Data Address fault
Data Nested TLB fault
Alternate Data TLB fault
VHPT Data fault
Data TLB fault
Data Page Not Present fault
Data NaT Page Consumption fault
Data Key Miss fault
Data Key Permission fault
Data Access Rights fault
Data Access Bit fault
Data Debug fault
loadrs — Load Register Stack

**Format:** loadrs

**Description:** This instruction ensures that a specified number of bytes (registers values and/or NaT collections) below the current BSP have been loaded from the backing store into the stacked general registers. The loaded registers are placed into the dirty partition of the register stack. All other stacked general registers are marked as invalid, without being saved to the backing store.

The number of bytes to be loaded is specified in a sub-field of the RSC application register (RSC.loadrs). Backing store addresses are always 8-byte aligned, and therefore the low order 3 bits of the loadrs field (RSC.loadrs[2:0]) are ignored. This instruction can be used to invalidate all stacked registers outside the current frame, by setting RSC.loadrs to zero.

This instruction will fault with an Illegal Operation fault under any of the following conditions:

- the RSE is not in enforced lazy mode (RSC.mode is non-zero).
- CFM.sof and RSC.loadrs are both non-zero.
- an attempt is made to load up more registers than are available in the physical stacked register file.

This instruction must be the first instruction in an instruction group and must either be in instruction slot 0 or in instruction slot 1 of a template having a stop after slot 0; otherwise, the results are undefined. This instruction cannot be predicated.

**Operation:**

```c
if (AR[RSC].mode != 0)
    illegal_operation_fault();
if ((CFM.sof != 0) && (AR[RSC].loadrs != 0))
    illegal_operation_fault();

rse_ensure_regs_loaded(AR[RSC].loadrs); // can raise faults listed below
AR[RNAT] = undefined();
```

**Interruptions:**

- Illegal Operation fault
- Unimplemented Data Address fault
- Data Nested TLB fault
- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault
- Data NaT Page Consumption fault
- Data Key Miss fault
- Data Key Permission fault
- Data Access Rights fault
- Data Access Bit fault
- Data Debug fault
mf — Memory Fence

Format:  

(\text{qp}) \text{ mf} \quad \text{ordering_form} \quad \text{M24} \\
(\text{qp}) \text{ mf.a} \quad \text{acceptance_form} \quad \text{M24}

Description:  
This instruction forces ordering between prior and subsequent memory accesses. The ordering_form ensures all prior data memory accesses are made visible prior to any subsequent data memory accesses being made visible. It does not ensure prior data memory references have been accepted by the external platform, nor that prior data memory references are visible.

The acceptance_form prevents any subsequent data memory accesses by the processor from initiating transactions to the external platform until:

- all prior loads to sequential pages have returned data, and
- all prior stores to sequential pages have been accepted by the external platform.

The definition of “acceptance” is platform dependent. The acceptance_form is typically used to ensure the processor has “waited” until a memory-mapped I/O transaction has been “accepted”, before initiating additional external transactions. The acceptance_form does not ensure ordering, or acceptance to memory areas other than sequential pages.

Operation:  

\[
\text{if } (\text{PR[qp]})\{ \\
\quad \text{if } (\text{acceptance_form}) \\
\quad \quad \text{acceptance_fence();} \\
\quad \text{else } // \text{ordering_form} \\
\quad \quad \text{ordering_fence();} \\
\}\]

Interruptions:  
None
mix — Mix

Format:

\[(qp) \text{ mix1.1 } r_1 = r_2, r_3 \quad \text{one_byte_form, left_form} \]
\[(qp) \text{ mix2.1 } r_1 = r_2, r_3 \quad \text{two_byte_form, left_form} \]
\[(qp) \text{ mix4.1 } r_1 = r_2, r_3 \quad \text{four_byte_form, left_form} \]
\[(qp) \text{ mix1.r } r_1 = r_2, r_3 \quad \text{one_byte_form, right_form} \]
\[(qp) \text{ mix2.r } r_1 = r_2, r_3 \quad \text{two_byte_form, right_form} \]
\[(qp) \text{ mix4.r } r_1 = r_2, r_3 \quad \text{four_byte_form, right_form} \]

Description: The data elements of GR \( r_2 \) and \( r_3 \) are mixed as shown in Figure 2-25, and the result placed in GR \( r_1 \). The data elements in the source registers are grouped in pairs, and one element from each pair is selected for the result. In the left_form, the result is formed from the leftmost elements from each of the pairs. In the right_form, the result is formed from the rightmost elements. Elements are selected alternately from the two source registers.
Figure 2-25. Mix Example
Operation: if (PR[qp]) {
    check_target_register(r);
    if (one_byte_form) { // one-byte elements
        x[0] = GR[r][7:0]; y[0] = GR[r][7:0];
        x[1] = GR[r][15:8]; y[1] = GR[r][15:8];
        x[5] = GR[r][47:40]; y[5] = GR[r][47:40];
        x[7] = GR[r][63:56]; y[7] = GR[r][63:56];
        if (left_form)
            GR[r] = concatenate8(x[7], y[7], x[5], y[5],
                                  x[3], y[3], x[1], y[1]);
        else // right_form
            GR[r] = concatenate8(x[6], y[6], x[4], y[4],
                                  x[2], y[2], x[0], y[0]);
    } else if (two_byte_form) { // two-byte elements
        x[0] = GR[r][15:0]; y[0] = GR[r][15:0];
        x[1] = GR[r][31:16]; y[1] = GR[r][31:16];
        if (left_form)
            GR[r] = concatenate4(x[3], y[3], x[1], y[1]);
        else // right_form
            GR[r] = concatenate4(x[2], y[2], x[0], y[0]);
    } else { // four-byte elements
        x[0] = GR[r][31:0]; y[0] = GR[r][31:0];
        if (left_form)
            GR[r] = concatenate2(x[1], y[1]);
        else // right_form
            GR[r] = concatenate2(x[0], y[0]);
    } // end of right form
    GR[r].nat = GR[r2].nat || GR[r3].nat;
}

Interruptions: Illegal Operation fault
mov — Move Application Register

**Description:**
The source operand is copied to the destination register.

In the from_form, the application register specified by `ar3` is copied into GR `r1` and the corresponding NaT bit is cleared.

In the to_form, the value in GR `r2` (in the register_form), or the sign-extended value in `imm8` (in the immediate_form), is placed in AR `ar3`. In the register_form if the NaT bit corresponding to GR `r2` is set, then a Register NaT Consumption fault is raised.

Only a subset of the application registers can be accessed by each execution unit (M or I). Table 3-3 on page 1:23 indicates which application registers may be accessed from which execution unit type. An access to an application register from the wrong unit type causes an Illegal Operation fault.

This instruction has multiple forms with the pseudo operation eliminating the need for specifying the execution unit. Accesses of the ARs are always implicitly serialized. While implicitly serialized, read-after-write and write-after-write dependency violations must be avoided (e.g., setting CCV, followed by `cmpxchg` in the same instruction group, or simultaneous writes to the UNAT register by `ld.fill` and `mov` to UNAT).
Operation:
if (PR[qp]) {
    tmp_type = (i_form ? AR_I_TYPE : AR_M_TYPE);
    if (is_reserved_reg(tmp_type, ar3))
        illegal_operation_fault();

    if (from_form) {
        check_target_register(r1);
        if (((ar3 == BSPSTORE) || (ar3 == RNAT)) && (AR[RSC].mode != 0))
            illegal_operation_fault();

        if (ar3 == ITC & PSR.si & PSR.cpl != 0)
            privileged_register_fault();

        GR[r1] = (is_ignored_reg(ar3)) ? 0 : AR[ar3];
        GR[r1].nat = 0;
    } else { // to_form
        tmp_val = (register_form) ? GR[r2] : sign_ext(imm8, 8);

        if (register_form & GR[r2].nat)
            register_nat Consumption_fault(0);

        if (is_read_only_register(AR_TYPE, ar3)
            (((ar3 == BSPSTORE) || (ar3 == RNAT)) && (AR[RSC].mode != 0)))
            illegal_operation_fault();

        if (is_reserved_field(AR_TYPE, ar3, tmp_val))
            reserved_register_field_fault();

        if (!(is_kernel_reg(ar3) || ar3 == ITC) && (PSR.cpl != 0))
            privileged_register_fault();

        if (!is_ignored_reg(ar3)) {
            tmp_val = ignored_field_mask(AR_TYPE, ar3, tmp_val);
            // check for illegal promotion
            if (ar3 == RSC && tmp_val[3:2] u< PSR.cpl)
                tmp_val[3:2] = PSR.cpl;
            AR[ar3] = tmp_val;

            if (ar3 == BSPSTORE) {
                AR[BSP] = rse_update_internal_stack_pointers(tmp_val);
                AR[RNAT] = undefined();
            }
        }
    }
}

Interruptions:  Illegal Operation fault
                Reserved Register/Field fault
                Register NaT Consumption fault
                Privileged Register fault
**mov — Move Branch Register**

**Format:**

\[
\begin{align*}
(qp) \text{ mov } r_1 = b_2 & \quad \text{from_form} \quad 122 \\
(qp) \text{ mov } b_1 = r_2 & \quad \text{pseudo-op} \\
(qp) \text{ mov } mwh.ih \ b_1 = r_2, \ tag_{13} & \quad \text{to_form} \quad 121 \\
(qp) \text{ mov } ret.mwh.ih \ b_1 = r_2, \ tag_{13} & \quad \text{return_form}, \text{to_form} \quad 121
\end{align*}
\]

**Description:**

The source operand is copied to the destination register.

In the from_form, the branch register specified by \( b_2 \) is copied into \( GR_r_1 \). The NaT bit corresponding to \( GR_r_1 \) is cleared.

In the to_form, the value in \( GR_r_2 \) is copied into \( BR_b_1 \). If the NaT bit corresponding to \( GR_r_2 \) is 1, then a Register NaT Consumption fault is taken.

A set of hints can also be provided when moving to a branch register. These hints are very similar to those provided on the \( brp \) instruction, and provide prediction information about a future branch which may use the value being moved into \( BR_b_1 \). The return_form is used to provide the hint that this value will be used in a return-type branch.

The values for the \( mwh \) whether hint completer are given in Table 2-39. For a description of the \( ih \) hint completer see the Branch Prediction instruction and Table 2-13 on page 3:28.

**Table 2-39. Move to BR Whether Hints**

<table>
<thead>
<tr>
<th>mwh Completer</th>
<th>Move to BR Whether Hint</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Ignore all hints</td>
</tr>
<tr>
<td>sptk</td>
<td>Static Taken</td>
</tr>
<tr>
<td>dptk</td>
<td>Dynamic</td>
</tr>
</tbody>
</table>

A pseudo-op is provided for copying a general register into a branch register when there is no hint information to be specified. This is encoded with a value of 0 for \( tag_{13} \) and values corresponding to \( none \) for the hint completers.

**Operation:**

```
if (PR[qp]) {
    if (from_form) {
        check_target_register(r_1);
        GR[r_1] = BR[b_2];
        GR[r_1].nat = 0;
    } else { // to_form
        tmp_tag = IP + sign_ext((timm_9 << 4), 13);
        if (GR[r_2].nat)
            register_nat_consumption_fault(0);
        BR[b_1] = GR[r_2];
        branch_predict(mwh, ih, return_form, GR[r_2], tmp_tag);
    }
}
```

**Interruptions:**

- Illegal Operation fault
- Register NaT Consumption fault
mov cr

mov — Move Control Register

Format:

\[(qp) \text{mov} \quad r_1 = cr_3 \quad \text{from\_form} \quad M33\]
\[(qp) \text{mov} \quad cr_3 = r_2 \quad \text{to\_form} \quad M32\]

Description:
The source operand is copied to the destination register.

For the from\_form, the control register specified by \(cr_3\) is read and the value copied into GR \(r_1\).

For the to\_form, GR \(r_2\) is read and the value copied into CR \(cr_3\).

Control registers can only be accessed at the most privileged level. Reading or writing an interruption control register (CR16-CR25), when the PSR.ic bit is one, will result in an Illegal Operation fault.

Operation:

\[
\text{if } \{ PR[qp] \}\{
    \text{if } \{ \text{is\_reserved\_reg(CR\_TYPE, cr_3)} \}
    \text{if } \{ \text{is\_read\_only\_reg(CR\_TYPE, cr_3)} \}
    \text{if } \{ \text{PSR.ic & is\_interruption\_cr(cr_3)} \}
    \text{illegal\_operation\_fault();}
\}
\]

\[
\text{if } \{ \text{from\_form} \}
    \text{check\_target\_register(r_1);}
\text{if } \{ \text{PSR.cpl != 0} \}
    \text{privileged\_operation\_fault(0);}
\text{if } \{ \text{from\_form} \} \{
    \text{if } \{ \text{cr_3 == IVR} \}
        \text{check\_interrupt\_request();}
    \text{if } \{ \text{cr_3 == ITIR} \}
        GR[r_1] = \text{impl\_itir\_cwi\_mask(CR[ITIR]);}
    \text{else}
        GR[r_1] = CR[cr_3];
    \}
\text{else } \{ \text{// to\_form}
    \text{if } \{ \text{GR[r_2].nat} \}
        \text{register\_nat\_consumption\_fault(0);}
    \text{if } \{ \text{is\_reserved\_field(CR\_TYPE, cr_3, GR[r_2])} \}
        \text{reserved\_register\_field\_fault();}
    \text{if } \{ \text{cr_3 == EOI} \}
        \text{end\_of\_interrupt();}
    \text{tmp\_val = ignored\_field\_mask(CR\_TYPE, cr_3, GR[r_2]);}
    \text{CR[cr_3] = tmp\_val;}
    \text{if } \{ \text{cr_3 == IIPA} \}
        \text{last\_IP = tmp\_val;}
\}
\}
\]

Interuptions:

<table>
<thead>
<tr>
<th>Illegal Operation fault</th>
<th>Register NaT Consumption fault</th>
</tr>
</thead>
<tbody>
<tr>
<td>Privileged Operation fault</td>
<td>Reserved Register/Field fault</td>
</tr>
</tbody>
</table>

Serialization:

Reads of control registers reflect the results of all prior instruction groups and interruptions.

In general, writes to control registers do not immediately affect subsequent instructions. Software must issue a serialize operation before a dependent instruction uses a modified resource.

Control register writes are not implicitly synchronized with a corresponding control register read and requires data serialization.
**mov — Move Floating-point Register**

**Format:**

\[(qp)\] mov \(f_1 = f_3\)  

 pseudo-op of: \[(qp)\] fmerge.s \(f_1 = f_3, f_3\)

**Description:**

The value of FR \(f_3\) is copied to FR \(f_1\).

**Operation:**

See “fmerge — Floating-point Merge” on page 3:72.
**mov — Move General Register**

**Format:**

\[
(qp) \text{ mov } r_j = r_3
\]

pseudo-op of: \((qp) \text{ adds } r_j = 0, r_3\)

**Description:**
The value of GR \(r_3\) is copied to GR \(r_j\).

**Operation:**
See “add — Add” on page 3:11.
mov — Move Immediate

Format: \((qp) \text{ mov } r_1 = \text{imm}_{22}\)

Description: The immediate value, \(\text{imm}_{22}\), is sign extended to 64 bits and placed in GR \(r_1\).

Operation: See “add — Add” on page 3:11.
mov — Move Indirect Register

Format:

\[
(qp) \text{ mov } r_1 = \text{ireg}[r_3] \quad \text{from}_\text{form} \quad \text{M43}
\]

\[
(qp) \text{ mov } \text{ireg}[r_3] = r_2 \quad \text{to}_\text{form} \quad \text{M42}
\]

Description: The source operand is copied to the destination register.

For move from indirect register, GR \( r_2 \) is read and the value used as an index into the register file specified by \( \text{ireg} \) (see Table 2-40 below). The indexed register is read and its value is copied into GR \( r_1 \).

For move to indirect register, GR \( r_3 \) is read and the value used as an index into the register file specified by \( \text{ireg} \). GR \( r_2 \) is read and its value copied into the indexed register.

Table 2-40. Indirect Register File Mnemonics

<table>
<thead>
<tr>
<th>( \text{ireg} )</th>
<th>Register File</th>
</tr>
</thead>
<tbody>
<tr>
<td>cpuid</td>
<td>Processor Identification Register</td>
</tr>
<tr>
<td>dbrr</td>
<td>Data Breakpoint Register</td>
</tr>
<tr>
<td>ibrr</td>
<td>Instruction Breakpoint Register</td>
</tr>
<tr>
<td>pkrr</td>
<td>Protection Key Register</td>
</tr>
<tr>
<td>pmc</td>
<td>Performance Monitor Configuration Register</td>
</tr>
<tr>
<td>pmd</td>
<td>Performance Monitor Data Register</td>
</tr>
<tr>
<td>rr</td>
<td>Region Register</td>
</tr>
</tbody>
</table>

For all register files other than the region registers, bits \{7:0\} of GR \( r_3 \) are used as the index. For region registers, bits \{63:61\} are used. The remainder of the bits are ignored.

Instruction and data breakpoint, performance monitor configuration, protection key, and region registers can only be accessed at the most privileged level. Performance monitor data registers can only be written at the most privileged level.

The CPU identification registers can only be read. There is no to_form of this instruction.

For move to protection key register, the processor ensures uniqueness of protection keys by checking new valid protection keys against all protection key registers. If any matching keys are found, duplicate protection keys are invalidated.

Apart from the PMC and PMD register files, access of a non-existent register results in a Reserved Register/Field fault. All accesses to the implementation-dependent portion of PMC and PMD register files result in implementation dependent behavior but do not fault.

Modifying a region register or a protection key register which is being used to translate:

- the executing instruction stream when PSR.it == 1, or
- the data space for an eager RSE reference when PSR.rt == 1

is an undefined operation.
Operation: if (PR[gp]) {
    if (ireg == RR_TYPE)
        tmp_index = GR[r3]{63:61};
    else // all other register types
        tmp_index = GR[r3]{7:0};

    if (from_form) {
        check_target_register(r1);
        if (PSR.cpl != 0 && (!ireg == PMD_TYPE || ireg == CPUID_TYPE))
            privileged_operation_fault(0);
        if (GR[r3].nat)
            register_nat_consumption_fault(0);
        if (is_reserved_reg(ireg, tmp_index))
            reserved_register_field_fault();
    } else { // to_form
        if (PSR.cpl != 0)
            privileged_operation_fault(0);
        if (GR[r2].nat || GR[r3].nat)
            register_nat_consumption_fault(0);

        if (is_reserved_reg(ireg, tmp_index) || is_reserved_field(ireg, tmp_index, GR[r2]))
            reserved_register_field_fault();
        if (ireg == PKR_TYPE && GR[r2]{0} == 1) { // writing valid prot key
            if ((tmp_slot = tlb_search_pkr(GR[r2]{31:8})) != NOT_FOUND)
                PKR[tmp_slot].v = 0; // clear valid bit of matching key reg
        }
        tmp_val = ignored_field_mask(ireg, tmp_index, GR[r2]);
        switch (ireg) {
            case CPUID_TYPE: GR[r1] = CPUID[tmp_index]; break;
            case DBR_TYPE: GR[r1] = DBR[tmp_index]; break;
            case IBR_TYPE: GR[r1] = IBR[tmp_index]; break;
            case PKR_TYPE: GR[r1] = PKR[tmp_index]; break;
            case PMC_TYPE: GR[r1] = pmc_read(tmp_index); break;
            case RR_TYPE: GR[r1] = RR[tmp_index]; break;
            case PMD_TYPE: pmd_write(tmp_index, tmp_val); break;
            case RR_TYPE: RR[tmp_index] = tmp_val; break;
        }
    }
}
**Interruptions:**
- Illegal Operation fault
- Privileged Operation fault
- Register NaT Consumption fault
- Reserved Register/Field fault

**Serialization:**
- For move to data breakpoint registers, software must issue a data serialize operation before issuing a memory reference dependent on the modified register.

- For move to instruction breakpoint registers, software must issue an instruction serialize operation before fetching an instruction dependent on the modified register.

- For move to protection key, region, performance monitor configuration, and performance monitor data registers, software must issue an instruction or data serialize operation to ensure the changes are observed before issuing any dependent instruction.

- To obtain improved accuracy, software can issue an instruction or data serialize operation before reading the performance monitors.
mov — Move Instruction Pointer

Format: \((qp)\) mov \(r_j = ip\)

Description: The Instruction Pointer (IP) for the bundle containing this instruction is copied into GR \(r_j\).

Operation:

\[
\text{if } (PR[qp]) \{
\text{check_target_register}(r_j);
\text{GR}[r_j] = \text{IP};
\text{GR}[r_j].\text{nat} = 0;
\}
\]

Interruptions: Illegal Operation fault
mov pr

**mov — Move Predicates**

**Format:**

\[
\begin{align*}
(qp) \text{mov } r_1 &= \text{pr} & \text{from\_form} & \text{I25} \\
(qp) \text{mov pr} &= r_2, \text{mask}_{17} & \text{to\_form} & \text{I23} \\
(qp) \text{mov pr.rot} &= \text{imm}_{44} & \text{to\_rotate\_form} & \text{I24}
\end{align*}
\]

**Description:**

The source operand is copied to the destination register.

For moving the predicates to a GR, PR i is copied to bit position i within GR r1.

For moving to the predicates, the source can either be a general register, or an immediate value. In the to_form, the source operand is GR r2 and only those predicates specified by the immediate value mask\(_{17}\) are written. The value mask\(_{17}\) is encoded in the instruction in an imm\(_{16}\) field such that: \(imm_{16} = mask_{17} \gg 1\). Predicate register 0 is always one. The mask\(_{17}\) value is sign extended. The most significant bit of mask\(_{17}\), therefore, is the mask bit for all of the rotating predicates. If there is a deferred exception for GR r2 (the NaT bit is 1), a Register NaT Consumption fault is taken.

In the to_rotate_form, only the 48 rotating predicates can be written. The source operand is taken from the imm\(_{44}\) operand (which is encoded in the instruction in an imm\(_{28}\) field, such that: \(imm_{28} = imm_{44} \gg 16\)). The low 16-bits correspond to the static predicates. The immediate is sign extended to set the top 21 predicates. Bit position i in the source operand is copied to PR i.

This instruction operates as if the predicate rotation base in the Current Frame Marker (CFM.rrb.pr) were zero.

**Operation:**

\[
\begin{align*}
\text{if } (\text{PR[qp]}) \{ \\
\text{if } (\text{from\_form}) \{ \\
\text{check\_target\_register}(r_1); \\
GR[r_1] &= 1; \quad \text{// PR[0] is always 1} \\
& \quad \text{for } (i = 1; i \leq 63; i++) \{ \\
& \quad \quad \text{GR}[r_1][i] = \text{PR[pr\_phys\_to\_virt(i)]}; \\
& \quad \} \\
& \quad \text{GR}[r_1].nat = 0; \\
\} \quad \text{else if } (\text{to\_form}) \{ \\
& \quad \text{if } (\text{GR[r_2]}.nat) \\
& \quad \quad \text{register\_nat\_consumption\_fault}(0); \\
& \quad \quad \text{tmp\_src} = \text{sign\_ext}(\text{mask}_{17}, 17); \\
& \quad \quad \text{for } (i = 1; i \leq 63; i++) \{ \\
& \quad \quad \quad \text{if } (\text{tmp\_src}(i)) \\
& \quad \quad \quad \quad \text{PR[pr\_phys\_to\_virt(i)]} = \text{GR}[r_2][i]; \\
& \quad \} \\
& \quad \text{else} \{ \quad \text{// to\_rotate\_form} \\
& \quad \quad \text{tmp\_src} = \text{sign\_ext}(\text{imm}_{44}, 44); \\
& \quad \quad \text{for } (i = 16; i \leq 63; i++) \{ \\
& \quad \quad \quad \text{PR[pr\_phys\_to\_virt(i)]} = \text{tmp\_src}(i); \\
& \quad \} \\
& \} \\
\} \quad \text{else} \{
& \quad \text{if } (\text{GR[r_2]}.nat) \\
& \quad \quad \text{register\_nat\_consumption\_fault}(0); \\
& \quad \quad \text{tmp\_src} = \text{sign\_ext}(\text{imm}_{44}, 44); \\
& \quad \quad \text{for } (i = 16; i \leq 63; i++) \{ \\
& \quad \quad \quad \text{PR[pr\_phys\_to\_virt(i)]} = \text{tmp\_src}(i); \\
& \quad \} \\
& \}
\end{align*}
\]

**Interruptions:**

- Illegal Operation fault
- Register NaT Consumption fault
mov — Move Processor Status Register

Format:  

\[(qp) \text{ mov } r_1 = \text{psr} \]  
\[(qp) \text{ mov } \text{psr} = r_2 \]

Description:  

The source operand is copied to the destination register. See Section 3.3.2, “Processor Status Register (PSR)” on page 2:18.

For move from processor status register, PSR bits \{36:35\} and \{31:0\} are read, and copied into GR \(r_1\). All other bits of the PSR read as zero.

For move to processor status register, GR \(r_2\) is read, bits \{31:0\} copied into PSR\{31:0\} and bits \{45:32\} are ignored. All bits of GR \(r_2\) corresponding to reserved fields of the PSR must be 0 or a Reserved Register/Field fault will result.

Moves to and from the PSR can only be performed at the most privileged level.

The contents of the interruption resources (that are overwritten when the PSR.ic bit is 1) are undefined if an interruption occurs between the enabling of the PSR.ic bit and a subsequent instruction serialize operation.

Operation:  

\[
\text{if (PR[qp]) } \{
\quad \text{if (from_form)}
\quad \quad \text{check_target_register}(r_1);
\quad \quad \text{if (PSR.cpl} = 0)
\quad \quad \quad \text{privileged_operation_fault}(0);
\quad \quad \text{if (from_form)} \{
\quad \quad \quad \text{tmp_val} = \text{zero_ext}(\text{PSR}\{31:0\}, 32); \quad \quad \quad \quad \text{// read lower 32 bits}
\quad \quad \quad \text{tmp_val} |\text{=} \text{PSR}\{36:35\} \ll 35; \quad \quad \quad \quad \text{// read mc and it bits}
\quad \quad \quad \text{GR}[r_1] = \text{tmp_val}; \quad \quad \quad \quad \text{// other bits read as zero}
\quad \quad \quad \text{GR}[r_1].\text{nat} = 0;
\quad \quad \text{else } \quad \quad \quad \text{// to_form}
\quad \quad \quad \text{if (GR}[r_2].\text{nat})
\quad \quad \quad \quad \text{register_nat_consumption_fault}(0);
\quad \quad \quad \quad \text{if (is_reserved_field(PSR\_TYPE, PSR\_MOVPART, GR}[r_2]))
\quad \quad \quad \quad \quad \text{reserved_register_field_fault();}
\quad \quad \quad \text{PSR}\{31:0\} = \text{GR}[r_2]\{31:0\};
\quad \quad \}\}
\}
\]

Interruptions:  

Illegal Operation fault  
Register NaT Consumption fault  
Privileged Operation fault  
Reserved Register/Field fault

Serialization:  

Software must issue an instruction or data serialize operation before issuing instructions dependent upon the altered PSR bits. Unlike with the \text{rsm} instruction, the PSR.i bit is not treated specially when cleared.
**mov — Move User Mask**

**Format:**

\[(qp) \text{mov } r_j = \text{psr.um} \quad \text{from_form} \quad \text{M36}\]

\[(qp) \text{mov } \text{psr.um} = r_2 \quad \text{to_form} \quad \text{M35}\]

**Description:**
The source operand is copied to the destination register.

For move from user mask, PSR{5:0} is read, zero-extend, and copied into GR \(r_j\).

For move to user mask, PSR{5:0} is written by bits \{5:0\} of GR \(r_2\). PSR.up can only be modified if the secure performance monitor bit (PSR.sp) is zero. Otherwise PSR.up is not modified.

Writing a non-zero value into any other parts of the PSR results in a Reserved Register/Field fault.

**Operation:**

\[
\text{if } (PR[qp]) \{
\text{if } (\text{from_form}) \{
\text{check_target_register}(r_j);\\
\text{GR}[r_j] = \text{zero_ext}(\text{PSR}{5:0}, 6);\\
\text{GR}[r_j].nat = 0;\\
\} \quad \text{else} \quad \text{// to_form}
\text{if } (\text{GR}[r_2].nat)\\
\text{register_nat_consumption_fault}(0);\\
\text{if } (\text{is_reserved_field}(\text{PSR\_TYPE}, \text{PSR\_UM}, \text{GR}[r_2]))\\
\text{reserved_register_field_fault}();\]

\[
\text{PSR}[1:0] = \text{GR}[r_2][1:0];\\
\text{if } (\text{PSR.sp} == 0) \quad \text{// unsecured perf monitor}\\
\text{PSR}[2] = \text{GR}[r_2][2];\\
\text{PSR}[5:3] = \text{GR}[r_2][5:3];\]
\]

**Interruptions:**

Illegal Operation fault
Reserved Register/Field fault
Register NaT Consumption fault

**Serialization:**
All user mask modifications are observed by the next instruction group.
movl — Move Long Immediate

**Format:**

\[(qp) \text{ movl } r1 = \text{imm}64\]  

**Description:**
The immediate value \[\text{imm}64\] is copied to GR \(r1\). The L slot of the bundle contains 41 bits of \[\text{imm}64\].

**Operation:**

\[
\text{if } (\text{PR}[qp]) \{ \\
\text{check\_target\_register}(r1); \\
\text{GR}[r1] = \text{imm}64; \\
\text{GR}[r1].\text{nat} = 0; \\
\} \\
\]

**Interruptions:**
Illegal Operation fault
mux — Mux

Format:  
\[(qp) \ \text{mux1} \ r_1 = r_2, \ mbtype_4\]  
\[(qp) \ \text{mux2} \ r_1 = r_2, \ mbtype_8\]

Description:  
A permutation is performed on the packed elements in a single source register, GR \(r_2\), and the result is placed in GR \(r_1\). For 8-bit elements, only some of all possible permutations can be specified. The five possible permutations are given in Table 2-41 and shown in Figure 2-26.

Table 2-41. Mux Permutations for 8-bit Elements

<table>
<thead>
<tr>
<th>mbtype_4</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>@rev</td>
<td>Reverse the order of the bytes</td>
</tr>
<tr>
<td>@mix</td>
<td>Perform a Mix operation on the two halves of GR (r_2)</td>
</tr>
<tr>
<td>@shuf</td>
<td>Perform a Shuffle operation on the two halves of GR (r_2)</td>
</tr>
<tr>
<td>@alt</td>
<td>Perform an Alternate operation on the two halves of GR (r_2)</td>
</tr>
<tr>
<td>@brcst</td>
<td>Perform a Broadcast operation on the least significand byte of GR (r_2)</td>
</tr>
</tbody>
</table>

Figure 2-26. Mux1 Operation (8-bit elements)
For 16-bit elements, all possible permutations, with and without repetitions can be specified. They are expressed with an 8-bit \textit{mhtype} field, which encodes the indices of the four 16-bit data elements. The indexed 16-bit elements of GR \( r_2 \) are copied to corresponding 16-bit positions in the target register GR \( r_1 \). The indices are encoded in little-endian order. (The 8 bits of \textit{mhtype}[7:0] are grouped in pairs of bits and named \textit{mhtype}[3], \textit{mhtype}[2], \textit{mhtype}[1], \textit{mhtype}[0] in the Operation section).

**Figure 2-27. Mux2 Examples (16-bit elements)**

![Diagram showing 16-bit data elements and target register operations]

```
Operation:
if (PR[qp]) {
  check_target_register(r1);
  if (one_byte_form) {
    x[0] = GR[r2]{7:0};
    x[1] = GR[r2]{15:8};
    x[3] = GR[r2]{31:24};
    x[5] = GR[r2]{47:40};
    x[7] = GR[r2]{63:56};
    switch (mbtype) {
      case '@rev':
        GR[r1] = concatenate8(x[0], x[1], x[2], x[3], x[4], x[5], x[6], x[7]);
        break;
      case '@mix':
        GR[r1] = concatenate8(x[7], x[3], x[5], x[1], x[6], x[2], x[4], x[0]);
        break;
      case '@shuf':
        GR[r1] = concatenate8(x[7], x[3], x[6], x[2], x[5], x[1], x[4], x[0]);
    }
  }
}
```
break;

case '@alt':
    GR[r_1] = concatenate8(x[7], x[5], x[3], x[1],
    x[6], x[4], x[2], x[0]);
    break;

case '@brcst':
    GR[r_1] = concatenate8(x[0], x[0], x[0], x[0],
    x[0], x[0], x[0], x[0]);
    break;
}
} else { // two_byte_form
    x[0] = GR[r_2]{15:0};
    x[1] = GR[r_2]{31:16};
    x[2] = GR[r_2]{47:32};
    x[3] = GR[r_2]{63:48};

    res[0] = x[mhtype8{1:0}] ;
    res[1] = x[mhtype8{3:2}] ;
    res[2] = x[mhtype8{5:4}] ;
    res[3] = x[mhtype8{7:6}] ;

    GR[r_1] = concatenate4(res[3], res[2], res[1], res[0]);
}
GR[r_1].nat = GR[r_2].nat;

**Interruptions:** Illegal Operation fault
**nop — No Operation**

**Format:**

- `(qp) nop imm21`  
  - pseudo-op
- `(qp) nop.i imm21`  
  - i_unit_form I18
- `(qp) nop.b imm21`  
  - b_unit_form B9
- `(qp) nop.m imm21`  
  - m_unit_form M48
- `(qp) nop.f imm21`  
  - f_unit_form F16
- `(qp) nop.x imm62`  
  - x_unit_form X5

**Description:**  
No operation is done.

The immediate, `imm21` or `imm62`, can be used by software as a marker in program code. It is ignored by hardware.

For the `x_unit_form`, the L slot of the bundle contains the upper 41 bits of `imm62`.

A `nop.i` instruction may be encoded in an MLI-template bundle, in which case the L slot of the bundle is ignored.

This instruction has five forms, each of which can be executed only on a particular execution unit type. The pseudo-op can be used if the unit type to execute on is unimportant.

**Operation:**

```c
if (PR[qp]) {
    ; // no operation
}
```

**Interruptions:**  
None
or — Logical Or

Format: 

\[
(qp) \text{ or } r_1 = r_2, r_3 \\
(qp) \text{ or } r_1 = \text{imm}_8, r_3
\]

register_form \hspace{1cm} \text{A1} \\
imm8_form \hspace{1cm} \text{A3}

Description: The two source operands are logically ORed and the result placed in GR \( r_1 \). In the register form the first operand is \( GR \ r_2 \); in the immediate form the first operand is taken from the \( \text{imm}_8 \) encoding field.

Operation:

\[
\text{if } (\text{PR} [qp]) \{
\text{check_target_register}(r_1);
\text{tmp}_\text{src} = (\text{register_form} \ ? \ GR[r_2] : \text{sign}\_\text{ext}(\text{imm}_8, \ 8));
\text{tmp}_\text{nat} = (\text{register_form} \ ? \ GR[r_2].\text{nat} : 0);
\text{GR}[r_1] = \text{tmp}_\text{src} \text{ or } \text{GR}[r_3];
\text{GR}[r_1].\text{nat} = \text{tmp}_\text{nat} \text{ or } \text{GR}[r_3].\text{nat};
\}
\]

Interruptions: Illegal Operation fault
pack — Pack

Format:

- \((qp)\) pack2.sss \(r_1 = r_2, r_3\)
- \((qp)\) pack2.uss \(r_1 = r_2, r_3\)
- \((qp)\) pack4.sss \(r_1 = r_2, r_3\)

Description:

32-bit or 16-bit elements from GR \(r_2\) and GR \(r_3\) are converted into 16-bit or 8-bit elements respectively, and the results are placed GR \(r_1\). The source elements are treated as signed values. If a source element cannot be represented in the result element, then saturation clipping is performed. The saturation can either be signed or unsigned. If an element is larger than the upper limit value, the result is the upper limit value. If it is smaller than the lower limit value, the result is the lower limit value. The saturation limits are given in Table 2-42.

Table 2-42. Pack Saturation Limits

<table>
<thead>
<tr>
<th>Size</th>
<th>Source Element Width</th>
<th>Result Element Width</th>
<th>Saturation</th>
<th>Upper Limit</th>
<th>Lower Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>16 bit</td>
<td>8 bit</td>
<td>signed signed</td>
<td>0x7f</td>
<td>0x80</td>
</tr>
<tr>
<td>2</td>
<td>16 bit</td>
<td>8 bit</td>
<td>unsigned</td>
<td>0xff</td>
<td>0x00</td>
</tr>
<tr>
<td>4</td>
<td>32 bit</td>
<td>16 bit</td>
<td>signed signed</td>
<td>0x7fff</td>
<td>0x8000</td>
</tr>
</tbody>
</table>

Figure 2-28. Pack Operation
Operation: if (PR[qp]) {
  check_target_register(r1);
  if (two_byte_form) {
    if (signed_saturation_form) {
      max = sign_ext(0x7f, 8);
      min = sign_ext(0x80, 8);
    } else { // unsigned_saturation_form
      max = 0xff;
      min = 0x00;
    }
    temp[0] = sign_ext(GR[r2]{15:0}, 16);
    temp[1] = sign_ext(GR[r2]{31:16}, 16);
    temp[2] = sign_ext(GR[r2]{47:32}, 16);
    temp[3] = sign_ext(GR[r2]{63:48}, 16);
    temp[4] = sign_ext(GR[r3]{15:0}, 16);
    temp[5] = sign_ext(GR[r3]{31:16}, 16);
    temp[6] = sign_ext(GR[r3]{47:32}, 16);
    temp[7] = sign_ext(GR[r3]{63:48}, 16);
    for (i = 0; i < 8; i++) {
      if (temp[i] > max)
        temp[i] = max;
      if (temp[i] < min)
        temp[i] = min;
    }
    GR[r1] = concatenate8(temp[7], temp[6], temp[5], temp[4],
                           temp[3], temp[2], temp[1], temp[0]);
  } else { // four_byte_form
    max = sign_ext(0x7fff, 16); // signed_saturation_form
    min = sign_ext(0x8000, 16);
    temp[0] = sign_ext(GR[r2]{31:0}, 32);
    temp[1] = sign_ext(GR[r2]{63:32}, 32);
    temp[2] = sign_ext(GR[r3]{31:0}, 32);
    temp[3] = sign_ext(GR[r3]{63:32}, 32);
    for (i = 0; i < 4; i++) {
      if (temp[i] > max)
        temp[i] = max;
      if (temp[i] < min)
        temp[i] = min;
    }
    GR[r1] = concatenate4(temp[3], temp[2], temp[1], temp[0]);
  }
  GR[r1].nat = GR[r2].nat || GR[r3].nat;
}

Interruptions: Illegal Operation fault
padd — Parallel Add

Format: 

\[(qp) \text{ padd1 } r_1 = r_2, r_3\] one_byte_form, modulo_form A9
\[(qp) \text{ padd1.sss } r_1 = r_2, r_3\] one_byte_form, sss_saturation_form A9
\[(qp) \text{ padd1.uus } r_1 = r_2, r_3\] one_byte_form, uus_saturation_form A9
\[(qp) \text{ padd1.uuu } r_1 = r_2, r_3\] one_byte_form, uuu_saturation_form A9
\[(qp) \text{ padd2 } r_1 = r_2, r_3\] two_byte_form, modulo_form A9
\[(qp) \text{ padd2.sss } r_1 = r_2, r_3\] two_byte_form, sss_saturation_form A9
\[(qp) \text{ padd2.uus } r_1 = r_2, r_3\] two_byte_form, uus_saturation_form A9
\[(qp) \text{ padd2.uuu } r_1 = r_2, r_3\] two_byte_form, uuu_saturation_form A9
\[(qp) \text{ padd4 } r_1 = r_2, r_3\] four_byte_form, modulo_form A9

Description: The sets of elements from the two source operands are added, and the results placed in GR \(r_1\).

If a sum of two elements cannot be represented in the result element and a saturation completer is specified, then saturation clipping is performed. The saturation can either be signed or unsigned, as given in Table 2-43. If the sum of two elements is larger than the upper limit value, the result is the upper limit value. If it is smaller than the lower limit value, the result is the lower limit value. The saturation limits are given in Table 2-44.

Table 2-43. Parallel Add Saturation Completers

<table>
<thead>
<tr>
<th>Completer</th>
<th>Result (r_1) Treated as</th>
<th>Source (r_2) Treated as</th>
<th>Source (r_3) Treated as</th>
</tr>
</thead>
<tbody>
<tr>
<td>sss</td>
<td>signed</td>
<td>signed</td>
<td>signed</td>
</tr>
<tr>
<td>uus</td>
<td>unsigned</td>
<td>unsigned</td>
<td>signed</td>
</tr>
<tr>
<td>uuu</td>
<td>unsigned</td>
<td>unsigned</td>
<td>unsigned</td>
</tr>
</tbody>
</table>

Table 2-44. Parallel Add Saturation Limits

<table>
<thead>
<tr>
<th>Size</th>
<th>Element Width</th>
<th>Result (r_1) signed</th>
<th>Result (r_1) unsigned</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Upper Limit</td>
<td>Lower Limit</td>
</tr>
<tr>
<td>1</td>
<td>8 bit</td>
<td>0x7f</td>
<td>0x80</td>
</tr>
<tr>
<td>2</td>
<td>16 bit</td>
<td>0x7fff</td>
<td>0x8000</td>
</tr>
</tbody>
</table>

Figure 2-29. Parallel Add Examples
Operation: if (PR[qp]) {
    check_target_register(r1);
    if (one_byte_form) { // one-byte elements
        x[0] = GR[r2][7:0]; y[0] = GR[r3][7:0];
        x[1] = GR[r2][15:8]; y[1] = GR[r3][15:8];
        x[5] = GR[r2][47:40]; y[5] = GR[r3][47:40];
        x[7] = GR[r2][63:56]; y[7] = GR[r3][63:56];
        if (sss_saturation_form) {
            max = sign_ext(0x7f, 8);
            min = sign_ext(0x80, 8);
            for (i = 0; i < 8; i++) {
                temp[i] = sign_ext(x[i], 8) + sign_ext(y[i], 8);
            }
        } else if (uus_saturation_form) {
            max = 0xff;
            min = 0x00;
            for (i = 0; i < 8; i++) {
                temp[i] = zero_ext(x[i], 8) + sign_ext(y[i], 8);
            }
        } else if (uuu_saturation_form) {
            max = 0xff;
            min = 0x00;
            for (i = 0; i < 8; i++) {
                temp[i] = zero_ext(x[i], 8) + zero_ext(y[i], 8);
            }
        } else { // modulo_form
            for (i = 0; i < 8; i++) {
                temp[i] = zero_ext(x[i], 8) + zero_ext(y[i], 8);
            }
        }
        if (sss_saturation_form || uus_saturation_form || uuu_saturation_form) {
            for (i = 0; i < 8; i++) {
                if (temp[i] > max)
                    temp[i] = max;
                if (temp[i] < min)
                    temp[i] = min;
            }
        }
        GR[r1] = concatenate8(temp[7], temp[6], temp[5], temp[4],
                              temp[3], temp[2], temp[1], temp[0]);
    } else if (two_byte_form) { // 2-byte elements
        x[0] = GR[r2][15:0]; y[0] = GR[r3][15:0];
        x[1] = GR[r2][31:16]; y[1] = GR[r3][31:16];
        if (sss_saturation_form) {
            max = sign_ext(0x7fff, 16);
            min = sign_ext(0x8000, 16);
        }
for (i = 0; i < 4; i++) {
    temp[i] = sign_ext(x[i], 16) + sign_ext(y[i], 16);
}
} else if (uus_saturation_form) {
    max = 0xffff;
    min = 0x0000;
    for (i = 0; i < 4; i++) {
        temp[i] = zero_ext(x[i], 16) + sign_ext(y[i], 16);
    }
} else if (uuu_saturation_form) {
    max = 0xffff;
    min = 0x0000;
    for (i = 0; i < 4; i++) {
        temp[i] = zero_ext(x[i], 16) + zero_ext(y[i], 16);
    }
} else { // modulo_form
    for (i = 0; i < 4; i++) {
        temp[i] = zero_ext(x[i], 16) + zero_ext(y[i], 16);
    }
}

if (sss_saturation_form || uus_saturation_form || uuu_saturation_form) {
    for (i = 0; i < 4; i++) {
        if (temp[i] > max)
            temp[i] = max;
        if (temp[i] < min)
            temp[i] = min;
    }
}
GR[r1] = concatenate4(temp[3], temp[2], temp[1], temp[0]);
} else { // four-byte elements
    x[0] = GR[r2]{31:0};  y[0] = GR[r3]{31:0};
    for (i = 0; i < 2; i++) { // modulo_form
        temp[i] = zero_ext(x[i], 32) + zero_ext(y[i], 32);
    }
    GR[r1] = concatenate2(temp[1], temp[0]);
}
GR[r1].nat = GR[r2].nat || GR[r3].nat;

**Interruptions:** Illegal Operation fault
pavg — Parallel Average

Format:

\[(qp) \text{pavg1 } r_1 = r_2, r_3\]
\[(qp) \text{pavg1.raz } r_1 = r_2, r_3\]
\[(qp) \text{pavg2 } r_1 = r_2, r_3\]
\[(qp) \text{pavg2.raz } r_1 = r_2, r_3\]

Description: The unsigned data elements of GR \(r_2\) are added to the unsigned data elements of GR \(r_3\). The results of the add are then each independently shifted to the right by one bit position. The high-order bits of each element are filled with the carry bits of the sums. To prevent cumulative round-off errors, an averaging is performed. The unsigned results are placed in GR \(r_1\).

The averaging operation works as follows. In the normal_form, the low-order bit of each result is set to 1 if at least one of the two least significant bits of the corresponding sum is 1. In the raz_form, the average rounds away from zero by adding 1 to each of the sums.

Figure 2-30. Parallel Average Example
Operation:

```c
if (PR[qp]) {
    check_target_register(r1);
    if (one_byte_form) {
        x[0] = GR[r2]{7:0}; y[0] = GR[r3]{7:0};
        if (raz_form) {
            for (i = 0; i < 8; i++) {
                temp[i] = zero_ext(x[i], 8) + zero_ext(y[i], 8) + 1;
                res[i] = shift_right_unsigned(temp[i], 1);
            }
        } else { // normal form
            for (i = 0; i < 8; i++) {
                temp[i] = zero_ext(x[i], 8) + zero_ext(y[i], 8);
                res[i] = shift_right_unsigned(temp[i], 1) | (temp[i][0]);
            }
        }
        GR[r1] = concatenate8(res[7], res[6], res[5], res[4],
                               res[3], res[2], res[1], res[0]);
    } else { // two_byte_form
        x[0] = GR[r2]{15:0}; y[0] = GR[r3]{15:0};
        if (raz_form) {
            for (i = 0; i < 4; i++) {
                temp[i] = zero_ext(x[i], 8) + zero_ext(y[i], 8) + 1;
                res[i] = shift_right_unsigned(temp[i], 1);
            }
        } else { // normal form
            for (i = 0; i < 4; i++) {
                temp[i] = zero_ext(x[i], 8) + zero_ext(y[i], 8);
                res[i] = shift_right_unsigned(temp[i], 1) | (temp[i][0]);
            }
        }
        GR[r1] = concatenate8(res[7], res[6], res[5], res[4],
                               res[3], res[2], res[1], res[0]);
    }
}
```

Figure 2-31. Parallel Average with Round Away from Zero Example
for (i = 0; i < 4; i++) {
    temp[i] = zero_ext(x[i], 16) + zero_ext(y[i], 16) + 1;
    res[i] = shift_right_unsigned(temp[i], 1);
}
} else { // normal form
    for (i = 0; i < 4; i++) {
        temp[i] = zero_ext(x[i], 16) + zero_ext(y[i], 16);
        res[i] = shift_right_unsigned(temp[i], 1) | (temp[i][0]);
    }
    GR[r1] = concatenate4(res[3], res[2], res[1], res[0]);
    GR[r1].nat = GR[r2].nat || GR[r3].nat;
}

**Interruptions:** Illegal Operation fault
pavgsub — Parallel Average Subtract

**Format:**

- \((qp)\) pavgsub1  \(r_1 = r_2, r_3\)
- \((qp)\) pavgsub2  \(r_1 = r_2, r_3\)

**Description:**
The unsigned data elements of \(GR_{r_3}\) are subtracted from the unsigned data elements of \(GR_{r_2}\). The results of the subtraction are then each independently shifted to the right by one bit position. The high-order bits of each element are filled with the borrow bits of the subtraction (the complements of the ALU carries). To prevent cumulative round-off errors, an averaging is performed. The low-order bit of each result is set to 1 if at least one of the two least significant bits of the corresponding difference is 1. The signed results are placed in \(GR_{r_1}\).

**Operation:**

```c
if (PR[qp]) {
    check_target_register(r_1);
    if (one_byte_form) {
        x[0] = GR[r_2]{7:0};  y[0] = GR[r_3]{7:0};
        for (i = 0; i < 8; i++) {
            temp[i] = zero_ext(x[i], 8) - zero_ext(y[i], 8);
            res[i] = (temp[i]{8:0} u>> 1) | (temp[i]{0});
        }
        GR[r_1] = concatenate8(res[7], res[6], res[5], res[4],
                               res[3], res[2], res[1], res[0]);
    } else { // two_byte_form
        x[0] = GR[r_2]{15:0};  y[0] = GR[r_3]{15:0};
```
x[1] = GR[r_2](31:16);  y[1] = GR[r_3](31:16);

x[2] = GR[r_2](47:32);  y[2] = GR[r_3](47:32);

x[3] = GR[r_2](63:48);  y[3] = GR[r_3](63:48);

for (i = 0; i < 4; i++) {
  temp[i] = zero_ext(x[i], 16) - zero_ext(y[i], 16);
  res[i] = (temp[i] u>> 1) | (temp[i]0);
}

GR[r_1] = concatenate4(res[3], res[2], res[1], res[0]);

}  

GR[r_1].nat = GR[r_2].nat || GR[r_3].nat;

**Interruptions:**  Illegal Operation fault
pcmp — Parallel Compare

Format:
- \((gp)\) pcmp1.prel \(r_1 = r_2, r_3\)
- \((gp)\) pcmp2.prel \(r_1 = r_2, r_3\)
- \((gp)\) pcmp4.prel \(r_1 = r_2, r_3\)

Description: The two source operands are compared for one of the two relations shown in Table 2-45. If the comparison condition is true for corresponding data elements of \(GR_{r_2}\) and \(GR_{r_3}\), then the corresponding data element in \(GR_{r_1}\) is set to all ones. If the comparison condition is false, then the corresponding data element in \(GR_{r_1}\) is set to all zeros. For the ‘>’ relation, both operands are interpreted as signed.

Table 2-45. Pcmp Relations

<table>
<thead>
<tr>
<th>prel</th>
<th>Compare Relation ((r_2 \text{ prel} r_3))</th>
</tr>
</thead>
<tbody>
<tr>
<td>eq</td>
<td>(r_2 == r_3)</td>
</tr>
<tr>
<td>gt</td>
<td>(r_2 &gt; r_3) (signed)</td>
</tr>
</tbody>
</table>

Figure 2-33. Parallel Compare Example
Operation: if (PR[gp]) {
    check_target_register(r);

    if (one_byte_form) {
        // one-byte elements
        x[0] = GR[r2]{7:0}; y[0] = GR[r3]{7:0};
        for (i = 0; i < 8; i++) {
            if (prel == 'eq')
                tmp_rel = x[i] == y[i];
            else // 'gt'
                tmp_rel = greater_signed(sign_ext(x[i], 8),
                                         sign_ext(y[i], 8));

            if (tmp_rel)
                res[i] = 0xff;
            else
                res[i] = 0x00;
        }
        GR[r1] = concatenate8(res[7], res[6], res[5], res[4],
                              res[3], res[2], res[1], res[0]);
    }
    else if (two_byte_form) {
        // two-byte elements
        x[0] = GR[r2]{15:0}; y[0] = GR[r3]{15:0};
        for (i = 0; i < 4; i++) {
            if (prel == 'eq')
                tmp_rel = x[i] == y[i];
            else // 'gt'
                tmp_rel = greater_signed(sign_ext(x[i], 16),
                                         sign_ext(y[i], 16));

            if (tmp_rel)
                res[i] = 0xffff;
            else
                res[i] = 0x0000;
        }
        GR[r1] = concatenate4(res[3], res[2], res[1], res[0]);
    }
    else {
        // four-byte elements
        x[0] = GR[r2]{31:0}; y[0] = GR[r3]{31:0};
        for (i = 0; i < 2; i++) {
            if (prel == 'eq')
                tmp_rel = x[i] == y[i];
            else // 'gt'
                tmp_rel = greater_signed(sign_ext(x[i], 32),
                                         sign_ext(y[i], 32));

            if (tmp_rel)
                res[i] = 0xffffffff;
            else
                res[i] = 0x00000000;
        }
        GR[r1] = concatenate2(res[1], res[0]);
    }
    GR[r1].nat = GR[r2].nat || GR[r3].nat;
}

Interruptions: Illegal Operation fault
pmax — Parallel Maximum

Format:  
(qp) pmax1.u  \( r_1 = r_2, r_3 \)  
(qp) pmax2  \( r_1 = r_2, r_3 \)  

Description:  The maximum of the two source operands is placed in the result register. In the one_byte_form, each unsigned 8-bit element of \( r_2 \) is compared with the corresponding unsigned 8-bit element of \( r_3 \) and the greater of the two is placed in the corresponding 8-bit element of \( r_1 \). In the two_byte_form, each signed 16-bit element of \( r_2 \) is compared with the corresponding signed 16-bit element of \( r_3 \) and the greater of the two is placed in the corresponding 16-bit element of \( r_1 \).

Operation:  
```
if (PR[qp]) {
    check_target_register(r1);
    if (one_byte_form) { // one-byte elements
        x[0] = GR[r2]{7:0}; y[0] = GR[r3]{7:0};
        for (i = 0; i < 8; i++) {
            res[i] = (zero_ext(x[i],8) < zero_ext(y[i],8)) ? y[i] : x[i];
        }
        GR[r1] = concatenate8(res[7], res[6], res[5], res[4],
                             res[3], res[2], res[1], res[0]);
    } else { // two-byte elements
        x[0] = GR[r2]{15:0}; y[0] = GR[r3]{15:0};
        for (i = 0; i < 4; i++) {
            res[i] = (sign_ext(x[i],16) < sign_ext(y[i],16)) ? y[i] : x[i];
        }
        GR[r1] = concatenate4(res[3], res[2], res[1], res[0]);
    }
    GR[r1].nat = GR[r2].nat || GR[r3].nat;
}
```

Interruptions:  Illegal Operation fault
pmin — Parallel Minimum

Format:

\[(qp) \ pmin1.u \ r_1 = r_2, r_3\]  \hspace{1cm} one_byte_form  \hspace{1cm} I2
\[(qp) \ pmin2 \ r_1 = r_2, r_3\]  \hspace{1cm} two_byte_form  \hspace{1cm} I2

Description: The minimum of the two source operands is placed in the result register. In the one_byte_form, each unsigned 8-bit element of GR \(r_2\) is compared with the corresponding unsigned 8-bit element of GR \(r_3\) and the smaller of the two is placed in the corresponding 8-bit element of GR \(r_1\). In the two_byte_form, each signed 16-bit element of GR \(r_2\) is compared with the corresponding signed 16-bit element of GR \(r_3\) and the smaller of the two is placed in the corresponding 16-bit element of GR \(r_1\).

Operation:

if (PR[qp]) {
    check_target_register(r1);
    if (one_byte_form) { // one-byte elements
        x[0] = GR[r2]{7:0}; y[0] = GR[r3]{7:0};
        for (i = 0; i < 8; i++) {
            res[i] = (zero_ext(x[i],8) < zero_ext(y[i],8)) ? x[i] : y[i];
        }
        GR[r1] = concatenate8(res[7], res[6], res[5], res[4],
                               res[3], res[2], res[1], res[0]);
    } else { // two-byte elements
        x[0] = GR[r2]{15:0}; y[0] = GR[r3]{15:0};
        for (i = 0; i < 4; i++) {
            res[i] = (sign_ext(x[i],16) < sign_ext(y[i],16)) ? x[i] : y[i];
        }
        GR[r1] = concatenate4(res[3], res[2], res[1], res[0]);
    }
    GR[r1].nat = GR[r2].nat || GR[r3].nat;
}

Interruptions: Illegal Operation fault
pmpy — Parallel Multiply

**Format:**

\[(qp) \; \text{pmpy}2.r \; r_1 = r_2, r_3\]  
\[(qp) \; \text{pmpy}2.l \; r_1 = r_2, r_3\]

**Description:** Two signed 16-bit data elements of GR \( r_2 \) are multiplied by the corresponding two signed 16-bit data elements of GR \( r_3 \) as shown in Figure 2-36. The two 32-bit results are placed in GR \( r_1 \).

**Figure 2-36. Parallel Multiply Operation**

```
if (PR[qp]) {
    check_target_register(r_1);
    if (right_form) {
        GR[r_1]{31:0} = sign_ext(GR[r_2]{15:0}, 16) * sign_ext(GR[r_3]{15:0}, 16);
        GR[r_1]{63:32} = sign_ext(GR[r_2]{47:32}, 16) * sign_ext(GR[r_3]{47:32}, 16);
    } else { // left_form
        GR[r_1]{31:0} = sign_ext(GR[r_2]{31:16}, 16) * sign_ext(GR[r_3]{31:16}, 16);
        GR[r_1]{63:32} = sign_ext(GR[r_2]{63:48}, 16) * sign_ext(GR[r_3]{63:48}, 16);
    }
    GR[r_1].nat = GR[r_2].nat || GR[r_3].nat;
}
```

**Interruptions:** Illegal Operation fault
pmpyshr — Parallel Multiply and Shift Right

Format:  

\[(qp)\ pmpyshr2\ r_1 = r_2, r_3, count_2\]  
\[(qp)\ pmpyshr2.u\ r_1 = r_2, r_3, count_2\]

signed_form  I1  
unsigned_form  I1

Description:  
The four 16-bit data elements of GR \(r_2\) are multiplied by the corresponding four 16-bit data elements of GR \(r_3\) as shown in Figure 2-37. This multiplication can either be signed (pmpyshr2), or unsigned (pmpyshr2.u). Each product is then shifted to the right \(count_2\) bits, and the least-significant 16-bits of each shifted product form 4 16-bit results, which are placed in GR \(r_1\). A \(count_2\) of 0 gives the 16 low bits of the results, a \(count_2\) of 16 gives the 16 high bits of the results. The allowed values for \(count_2\) are given in Table 2-46.

Table 2-46. PMPYSHR Shift Options

<table>
<thead>
<tr>
<th>(count_2)</th>
<th>Selected Bit Field from Each 32-bit Product</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>15:0</td>
</tr>
<tr>
<td>7</td>
<td>22:7</td>
</tr>
<tr>
<td>15</td>
<td>30:15</td>
</tr>
<tr>
<td>16</td>
<td>31:16</td>
</tr>
</tbody>
</table>

Figure 2-37. Parallel Multiply and Shift Right Operation

[Diagram showing the operation of pmpyshr2]
Operation: if (PR[qp]) {
    check_target_register(r_j);
    x[0] = GR[r_2]{15:0};    y[0] = GR[r_3]{15:0};
    for (i = 0; i < 4; i++) {
        if (unsigned_form) // unsigned multiplication
            temp[i] = zero_ext(x[i], 16) * zero_ext(y[i], 16);
        else // signed multiplication
            temp[i] = sign_ext(x[i], 16) * sign_ext(y[i], 16);
        res[i] = temp[i]{(count 2 + 15):count 2};
    }
    GR[r_j] = concatenate4(res[3], res[2], res[1], res[0]);
    GR[r_j].nat = GR[r_2].nat || GR[r_3].nat;
}

Interruptions: Illegal Operation fault
**popcnt — Population Count**

**Format:**

```
(qp) popcnt r1 = r3
```

**Description:** The number of bits in GR R3 having the value 1 is counted, and the resulting sum is placed in GR R1.

**Operation:**

```
if (PR[qp]) {
    check_target_register(r1);
    res = 0;
    // Count up all the one bits
    for (i = 0; i < 64; i++) {
        res += GR[r3]{i};
    }
    GR[r1] = res;
    GR[r1].nat = GR[r3].nat;
}
```

**Interruptions:** Illegal Operation fault
probe — Probe Access

Format:

- \((qp)\) probe.t \(r_1 = r_3, r_2\)  
  read_form, register_form  
  M38
- \((qp)\) probe.w \(r_1 = r_3, r_2\)  
  write_form, register_form  
  M38
- \((qp)\) probe.t \(r_1 = r_3, \text{imm}_2\)  
  read_form, immediate_form  
  M39
- \((qp)\) probe.w \(r_1 = r_3, \text{imm}_2\)  
  write_form, immediate_form  
  M39
- \((qp)\) probe.t.fault \(r_3, \text{imm}_2\)  
  fault_form, read_form, immediate_form  
  M40
- \((qp)\) probe.w.fault \(r_3, \text{imm}_2\)  
  fault_form, write_form, immediate_form  
  M40
- \((qp)\) probe.rw.fault \(r_3, \text{imm}_2\)  
  fault_form, read_write_form, immediate_form  
  M40

Description:

This instruction determines whether read or write access, with a specified privilege level, to a given virtual address is permitted. GR \(r_1\) is set to 1 if the specified access is allowed and to 0 otherwise. In the fault_form, if the specified access is allowed this instruction does nothing; if the specified access is not allowed, a fault is taken.

When PSR.dt is 1, the DTLB and the VHPT are queried for present translations to determine if access to the virtual address specified by GR \(r_3\) bits \(60:0\) and the region register indexed by GR \(r_3\) bits \(63:61\), is permitted at the privilege level given by either GR \(r_2\) bits \(1:0\) or \(\text{imm}_2\). If PSR.pk is 1, protection key checks are also performed. The read or write form specifies whether the instruction checks for read or write access, or both.

When PSR.dt is 0, a non-faulting probe uses its address operand as a virtual address to query the DTLB only, because the VHPT walker is disabled. If the probed address is found in the DTLB, the non-faulting probe returns the appropriate value, if not an Alternate Data TLB fault is raised.

When PSR.dt is 0, a faulting probe treats its address operand as a physical address, and takes no TLB related faults.

A non-faulting probe to an unimplemented virtual address returns 0. A faulting probe to an unimplemented virtual address (when PSR.dt is 1) or unimplemented physical address (when PSR.dt is 0) takes an Unimplemented Data Address fault.

If this instruction faults, then it will set the non-access bit in the ISR and set the ISR read or write bits depending on the completer. The following faults are taken by the faulting form of the probe instruction only (the non-faulting form of the instruction does not take them): Unimplemented Data Address fault, Data Key Permissions fault, Data Access Rights fault, Data Dirty Bit fault, Data Access Bit fault, and Data Debug fault.

This instruction can only probe with equal or lower privilege levels. If the specified privilege level is higher (lower number), then the probe is performed with the current privilege level.
Operation:

if (PR[qp]) {
    itype = NON_ACCESS;
    itype |= (read_write_form) ? READ | WRITE : ((write_form) ? WRITE : READ);
    itype |= (fault_form) ? PROBE_FAULT : PROBE;
    if (!fault_form)
        check_target_register(rj);
    if (GR[rj].nat | (register_form ? GR[r2].nat : 0))
        register_nat_consumption_fault(itype);
    tmp_pl = (register_form) ? GR[r2][1:0] : imm2;
    if (tmp_pl < PSR.cpl)
        tmp_pl = PSR.cpl;
    if (fault_form) {
        tlb_translate(GR[rj], 1, itype, tmp_pl, &mattr, &defer);
    } else {
        GR[rj] = tlb_grant_permission(GR[rj], itype, tmp_pl);
        GR[rj].nat = 0;
    }
}

Interruptions:

Illegal Operation fault                      Data NaT Page Consumption fault
Register NaT Consumption fault               Data Key Miss fault
Unimplemented Data Address fault             Data Key Permission fault
Data Nested TLB fault                       Data Access Rights fault
Alternate Data TLB fault                    Data Dirty Bit fault
VHPT Data fault                             Data Access Bit fault
Data TLB fault                              Data Debug fault
Data Page Not Present fault
psad — Parallel Sum of Absolute Difference

Format: \((qp)\) psad1 \(r_1 = r_2, r_3\)

Description: The unsigned 8-bit elements of GR \(r_2\) are subtracted from the unsigned 8-bit elements of GR \(r_3\). The absolute value of each difference is accumulated across the elements and placed in GR \(r_1\).

Operation:

\[
\text{if } (\text{PR}[qp]) \{
    \text{check_target_register}(r_1);
    x[0] = \text{GR}[r_2](7:0);
    y[0] = \text{GR}[r_3](7:0);
    x[1] = \text{GR}[r_2](15:8);
    y[1] = \text{GR}[r_3](15:8);
    x[2] = \text{GR}[r_2](23:16);
    y[2] = \text{GR}[r_3](23:16);
    x[3] = \text{GR}[r_2](31:24);
    y[3] = \text{GR}[r_3](31:24);
    x[4] = \text{GR}[r_2](39:32);
    y[4] = \text{GR}[r_3](39:32);
    x[5] = \text{GR}[r_2](47:40);
    y[5] = \text{GR}[r_3](47:40);
    x[6] = \text{GR}[r_2](55:48);
    y[6] = \text{GR}[r_3](55:48);
    x[7] = \text{GR}[r_2](63:56);
    y[7] = \text{GR}[r_3](63:56);
    GR[r_1] = 0;
    \text{for } (i = 0; \ i < 8; \ i++) \{
        \text{temp}[i] = \text{zero_ext}(x[i], \ 8) - \text{zero_ext}(y[i], \ 8);
        \text{if } (\text{temp}[i] < 0)
            \text{temp}[i] = -\text{temp}[i];
        GR[r_1] += \text{temp}[i];
    \}
    GR[r_1].nat = \text{GR}[r_2].nat || \text{GR}[r_3].nat;
\}
\]

Interruptions: Illegal Operation fault
pshl — Parallel Shift Left

Format:

| (qp) pshl2 | \( r_j = r_2, r_3 \) | two-byte_form, variable_form | 17 |
| (qp) pshl2 | \( r_j = r_2, \text{count}_5 \) | two-byte_form, fixed_form | 18 |
| (qp) pshl4 | \( r_j = r_2, r_3 \) | four-byte_form, variable_form | 17 |
| (qp) pshl4 | \( r_j = r_2, \text{count}_5 \) | four-byte_form, fixed_form | 18 |

Description: The data elements of GR \( r_j \) are each independently shifted to the left by the scalar shift count in GR \( r_3 \), or in the immediate field \( \text{count}_5 \). The low-order bits of each element are filled with zeros. The shift count is interpreted as unsigned. Shift counts greater than 15 (for 16-bit quantities) or 31 (for 32-bit quantities) yield all zero results. The results are placed in GR \( r_1 \).

Figure 2-39. Parallel Shift Left Example

Operation:

```c
if (PR[qp]) {
    check_target_register(r_1);
    shift_count = (variable_form ? GR[r_3] : count_5);
    tmp_nat = (variable_form ? GR[r_3].nat : 0);
    if (two_byte_form) { // two_byte_form
        if (shift_count > 16)
            shift_count = 16;
        GR[r_1]{15:0} = GR[r_2]{15:0} << shift_count;
        GR[r_1]{31:16} = GR[r_2]{31:16} << shift_count;
        GR[r_1]{47:32} = GR[r_2]{47:32} << shift_count;
        GR[r_1]{63:48} = GR[r_2]{63:48} << shift_count;
    } else { // four_byte_form
        if (shift_count > 32)
            shift_count = 32;
        GR[r_1]{31:0} = GR[r_2]{31:0} << shift_count;
        GR[r_1]{63:32} = GR[r_2]{63:32} << shift_count;
    }
    GR[r_1].nat = GR[r_2].nat || tmp_nat;
}
```

Interruptions: Illegal Operation fault
pshladd — Parallel Shift Left and Add

Format:  \((qp)\) pshladd \(r_1\) = \(r_2\), \(count_2\), \(r_3\)

Description:  The four signed 16-bit data elements of GR \(r_2\) are each independently shifted to the left by \(count_2\) bits (shifting zeros into the low-order bits), and added to the four signed 16-bit data elements of GR \(r_3\). Both the left shift and the add operations are saturating: if the result of either the shift or the add is not representable as a signed 16-bit value, the final result is saturated. The four signed 16-bit results are placed in GR \(r_1\). The first operand can be shifted by 1, 2 or 3 bits.

Operation:  if \((PR[qp])\) {
  check_target_register\((r_1)\);
  x[0] = GR\([r_2]\{15:0\});  y[0] = GR\([r_3]\{15:0\});
  x[1] = GR\([r_2]\{31:16\});  y[1] = GR\([r_3]\{31:16\});

  max = sign_ext(0x7fff, 16);
  min = sign_ext(0x8000, 16);

  for (i = 0; i < 4; i++) {
    temp[i] = sign_ext\(x[i]\), 16) \ll count_2;
    if (temp[i] > max)
      res[i] = max;
    else if (temp[i] < min)
      res[i] = min;
    else {
      res[i] = temp[i] + sign_ext\(y[i]\), 16);
      if (res[i] > max)
        res[i] = max;
      if (res[i] < min)
        res[i] = min;
    }
  }

  GR\([r_1]\) = concatenate\(res[3], res[2], res[1], res[0]\);
  GR\([r_1]\).nat = GR\([r_2]\).nat || GR\([r_3]\).nat;
}

Interruptions:  Illegal Operation fault
pshr — Parallel Shift Right

Format:

\( (qp) \text{pshr} \ r_1 = r_3, r_2 \)  
\( (qp) \text{pshr} \ r_1 = r_3, \text{count}_5 \)  
\( (qp) \text{pshr}_u \ r_1 = r_3, r_2 \)  
\( (qp) \text{pshr}_u \ r_1 = r_3, \text{count}_5 \)  
\( (qp) \text{pshr} \ r_1 = r_3, \text{count}_5 \)  
\( (qp) \text{pshr}_u \ r_1 = r_3, \text{count}_5 \)  
\( (qp) \text{pshr}_u \ r_1 = r_3, \text{count}_5 \)  
\( (qp) \text{pshr}_u \ r_1 = r_3, \text{count}_5 \)

Description: The data elements of GR \( r_3 \) are each independently shifted to the right by the scalar shift count in GR \( r_2 \), or in the immediate field \( \text{count}_5 \). The high-order bits of each element are filled with either the initial value of the sign bits of the data elements in GR \( r_3 \) (arithmetic shift) or zeros (logical shift). The shift count is interpreted as unsigned. Shift counts greater than 15 (for 16-bit quantities) or 31 (for 32-bit quantities) yield all zero or all one results depending on the initial values of the sign bits of the data elements in GR \( r_3 \) and whether a signed or unsigned shift is done. The results are placed in GR \( r_1 \).

Operation:

```c
if (PR[qp]) {
    check_target_register(r_1);
    shift_count = (variable_form ? GR[r_2] : count_5);
    tmp_nat = (variable_form ? GR[r_2].nat : 0);
    if (two_byte_form) { // two_byte_form
        shift_count = 16;
        if (unsigned_form) { // unsigned shift
            GR[r_1]{15:0} = shift_right_unsigned(zero_ext(GR[r_3]{15:0}, 16), shift_count);
            GR[r_1]{31:16} = shift_right_unsigned(zero_ext(GR[r_3]{31:16}, 16), shift_count);
            GR[r_1]{47:32} = shift_right_unsigned(zero_ext(GR[r_3]{47:32}, 16), shift_count);
            GR[r_1]{63:48} = shift_right_unsigned(zero_ext(GR[r_3]{63:48}, 16), shift_count);
        } else { // signed shift
            GR[r_1]{15:0} = shift_right_signed(sign_ext(GR[r_3]{15:0}, 16), shift_count);
            GR[r_1]{31:16} = shift_right_signed(sign_ext(GR[r_3]{31:16}, 16), shift_count);
            GR[r_1]{47:32} = shift_right_signed(sign_ext(GR[r_3]{47:32}, 16), shift_count);
            GR[r_1]{63:48} = shift_right_signed(sign_ext(GR[r_3]{63:48}, 16), shift_count);
        }
    } else { // four_byte_form
        if (unsigned_form) { // unsigned shift
            GR[r_1]{31:0} = shift_right_unsigned(zero_ext(GR[r_3]{31:0}, 32), shift_count);
            GR[r_1]{63:32} = shift_right_unsigned(zero_ext(GR[r_3]{63:32}, 32), shift_count);
        } else { // signed shift
            GR[r_1]{31:0} = shift_right_signed(sign_ext(GR[r_3]{31:0}, 32), shift_count);
            GR[r_1]{63:32} = shift_right_signed(sign_ext(GR[r_3]{63:32}, 32), shift_count);
        }
    }
}
```
\[ \text{Interruptions: Illegal Operation fault} \]
pshradd — Parallel Shift Right and Add

Format: \((qp)\ pshradd2\ r1 = r2,\ count2,\ r3\)

Description: The four signed 16-bit data elements of GR \(r2\) are each independently shifted to the right by \(count2\) bits, and added to the four signed 16-bit data elements of GR \(r3\). The right shift operation fills the high-order bits of each element with the initial value of the sign bits of the data elements in GR \(r2\). The add operation is performed with signed saturation. The four signed 16-bit results of the add are placed in GR \(r1\). The first operand can be shifted by 1, 2 or 3 bits.

Operation:

\[
\text{if (PR[qp])} \{
\begin{align*}
\text{check_target_register}(r1); \\
\text{x}[0] &= \text{GR}[r2]\{15:0\}; & y[0] &= \text{GR}[r3]\{15:0\}; \\
\text{x}[1] &= \text{GR}[r2]\{31:16\}; & y[1] &= \text{GR}[r3]\{31:16\}; \\
\text{x}[2] &= \text{GR}[r2]\{47:32\}; & y[2] &= \text{GR}[r3]\{47:32\}; \\
\text{x}[3] &= \text{GR}[r2]\{63:48\}; & y[3] &= \text{GR}[r3]\{63:48\}; \\
\end{align*}
\]

\[
\text{max} = \text{sign_ext}(0x7fff, 16); \quad \text{min} = \text{sign_ext}(0x8000, 16);
\]

\[
\text{for (i = 0; i < 4; i++)} \{
\begin{align*}
\text{temp}[i] &= \text{shift_right_signed}((\text{sign_ext}(\text{x}[i], 16), \text{count2}); \\
\text{res}[i] &= \text{temp}[i] + \text{sign_ext}(\text{y}[i], 16); \\
\text{if (res}[i] > \text{max}) \\
\text{res}[i] &= \text{max}; \\
\text{if (res}[i] < \text{min}) \\
\text{res}[i] &= \text{min}; \\
\end{align*}
\}
\]

\[
\text{GR}[r1] = \text{concatenate4}(\text{res}[3], \text{res}[2], \text{res}[1], \text{res}[0]); \\
\text{GR}[r1].\text{nat} = \text{GR}[r2].\text{nat} \ || \ \text{GR}[r3].\text{nat};
\]

Interruptions: Illegal Operation fault
psub — Parallel Subtract

Format:

\[(qp)\] psub1  \( r_1 = r_2, r_3 \)
\[(qp)\] psub1.sss  \( r_1 = r_2, r_3 \)
\[(qp)\] psub1.uus  \( r_1 = r_2, r_3 \)
\[(qp)\] psub1.uuu  \( r_1 = r_2, r_3 \)
\[(qp)\] psub2  \( r_1 = r_2, r_3 \)
\[(qp)\] psub2.sss  \( r_1 = r_2, r_3 \)
\[(qp)\] psub2.uus  \( r_1 = r_2, r_3 \)
\[(qp)\] psub2.uuu  \( r_1 = r_2, r_3 \)
\[(qp)\] psub4  \( r_1 = r_2, r_3 \)

Description: The sets of elements from the two source operands are subtracted, and the results placed in GR \( r_1 \).

If the difference between two elements cannot be represented in the result element and a saturation completer is specified, then saturation clipping is performed. The saturation can either be signed or unsigned, as given in Table 2-47. If the difference of two elements is larger than the upper limit value, the result is the upper limit value. If it is smaller than the lower limit value, the result is the lower limit value. The saturation limits are given in Table 2-48.

Table 2-47. Parallel Subtract Saturation Completers

<table>
<thead>
<tr>
<th>Completer</th>
<th>Result ( r_1 ) Treated as</th>
<th>Source ( r_2 ) Treated as</th>
<th>Source ( r_3 ) Treated as</th>
</tr>
</thead>
<tbody>
<tr>
<td>sss</td>
<td>signed</td>
<td>signed</td>
<td>signed</td>
</tr>
<tr>
<td>uus</td>
<td>unsigned</td>
<td>unsigned</td>
<td>signed</td>
</tr>
<tr>
<td>uuu</td>
<td>unsigned</td>
<td>unsigned</td>
<td>unsigned</td>
</tr>
</tbody>
</table>

Table 2-48. Parallel Subtract Saturation Limits

<table>
<thead>
<tr>
<th>Size</th>
<th>Element Width</th>
<th>Result ( r_1 ) Signed</th>
<th>Result ( r_1 ) Unsigned</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Upper Limit</td>
<td>Lower Limit</td>
</tr>
<tr>
<td>1</td>
<td>8 bit</td>
<td>0x7f</td>
<td>0x80</td>
</tr>
<tr>
<td>2</td>
<td>16 bit</td>
<td>0x7fff</td>
<td>0x8000</td>
</tr>
</tbody>
</table>

Figure 2-40. Parallel Subtract Example
Operation: if (PR[qp]) {
    check_target_register(r1);

    if (one_byte_form) { // one-byte elements
        x[0] = GR[r2]{7:0};     y[0] = GR[r3]{7:0};

        if (sss_saturation_form) { // sss_saturation_form
            max = sign_ext(0x7f, 8);
            min = sign_ext(0x80, 8);
            for (i = 0; i < 8; i++) {
                temp[i] = sign_ext(x[i], 8) - sign_ext(y[i], 8);
            }
        } else if (uus_saturation_form) { // uus_saturation_form
            max = 0xff;
            min = 0x00;
            for (i = 0; i < 8; i++) {
                temp[i] = zero_ext(x[i], 8) - sign_ext(y[i], 8);
            }
        } else if (uuu_saturation_form) { // uuu_saturation_form
            max = 0xff;
            min = 0x00;
            for (i = 0; i < 8; i++) {
                temp[i] = zero_ext(x[i], 8) - zero_ext(y[i], 8);
            }
        } else { // modulo_form
            for (i = 0; i < 8; i++) {
                temp[i] = zero_ext(x[i], 8) - zero_ext(y[i], 8);
            }
        }
    }

    if (two_byte_form) { // two-byte elements
        x[0] = GR[r2]{15:0};     y[0] = GR[r3]{15:0};

        if (sss_saturation_form) { // sss_saturation_form
            max = sign_ext(0x7fff, 16);
            min = sign_ext(0x8000, 16);
            for (i = 0; i < 16; i++) {
                temp[i] = sign_ext(x[i], 16) - sign_ext(y[i], 16);
            }
        } else if (uus_saturation_form) { // uus_saturation_form
            max = 0xffff;
            min = 0x0000;
            for (i = 0; i < 16; i++) {
                temp[i] = zero_ext(x[i], 16) - sign_ext(y[i], 16);
            }
        } else {
            for (i = 0; i < 16; i++) {
                temp[i] = zero_ext(x[i], 16) - zero_ext(y[i], 16);
            }
        }
    }

    GR[r1] = concatenate8(temp[7], temp[6], temp[5], temp[4],
                          temp[3], temp[2], temp[1], temp[0]);
}

if (sss_saturation_form || uus_saturation_form ||
    uuu_saturation_form) {
    for (i = 0; i < 8; i++) {
        if (temp[i] > max)
            temp[i] = max;
        if (temp[i] < min)
            temp[i] = min;
    }
}

GR[r1] = concatenate8(temp[7], temp[6], temp[5], temp[4],
                      temp[3], temp[2], temp[1], temp[0]);
psub

max = 0xffff;
min = 0x0000;
for (i = 0; i < 4; i++) {
    temp[i] = zero_ext(x[i], 16) - sign_ext(y[i], 16);
}
else if (uuu_saturation_form) { // uuu_saturation_form
    max = 0xffff;
    min = 0x0000;
    for (i = 0; i < 4; i++) {
        temp[i] = zero_ext(x[i], 16) - zero_ext(y[i], 16);
    }
} else if (uuu_saturation_form) { // modulo_form
    for (i = 0; i < 4; i++) {
        temp[i] = zero_ext(x[i], 16) - zero_ext(y[i], 16);
    }
}
if (sss_saturation_form || uus_saturation_form ||
    uuu_saturation_form) {
    for (i = 0; i < 4; i++) {
        if (temp[i] > max)
            temp[i] = max;
        if (temp[i] < min)
            temp[i] = min;
    }
}
GR[r_1] = concatenate4(temp[3], temp[2], temp[1], temp[0]);
} else { // four-byte elements
    x[0] = GR[r_2]{31:0}; y[0] = GR[r_3]{31:0};
    for (i = 0; i < 2; i++) { // modulo_form
        temp[i] = zero_ext(x[i], 32) - zero_ext(y[i], 32);
    }
    GR[r_1] = concatenate2(temp[1], temp[0]);
}
GR[r_1].nat = GR[r_2].nat || GR[r_3].nat;

Interruptions: Illegal Operation fault
**ptc.e — Purge Translation Cache Entry**

**Format:**  
\[(qp) \text{ ptc.e } r_3\]

**Description:**  
One or more translation entries are purged from the local processor’s instruction and data translation cache. Translation Registers and the VHPT are not modified.

The number of translation cache entries purged is implementation specific. Some implementations may purge all levels of the translation cache hierarchy with one iteration of PTC.e, while other implementations may require several iterations to flush all levels, sets and associativities of both instruction and data translation caches. GR \(r_3\) specifies an implementation specific parameter associated with each iteration.

The following loop is defined to flush the entire translation cache for all processor models. Software can acquire parameters through a processor dependent layer that is accessed through a procedural interface. The selected region registers must remain unchanged during the loop.

```c
disable_interrupts();  
addr = base;  
for (i = 0; i < count1; i++) {  
  for (j = 0; j < count2; j++) {  
    ptc.e(addr);  
    addr += stride2;  
  }  
  addr += stride1;  
}  
enable_interrupts();
```

**Operation:**  
\[
\text{if } (\text{PR[qp]} \text{ }) \{  \
  \text{if } (\text{PSR.cpl} \neq 0)  
  \text{privileged_operation_fault(0);}  
  \text{if } (\text{GR[r_3].nat})  
  \text{register_nat_consumption_fault(0);}  
  \text{tlb_purge_translation_cache(GR[r_3]);}  
\}
\]

**Interruptions:**  
Privileged Operation fault  
Register NaT Consumption fault

**Serialization:**  
Software must issue a data serialization operation to ensure the purge is complete before issuing a data access or non-access reference dependent upon the purge. Software must issue instruction serialize operation before fetching an instruction dependent upon the purge.
ptc.g, ptc.ga — Purge Global Translation Cache

Format:

\[(qp)\] ptc.g \(r_3, r_2\) \hspace{1cm} \text{global\_form} \hspace{1cm} \text{M45}
\[(qp)\] ptc.ga \(r_3, r_2\) \hspace{1cm} \text{global\_alat\_form} \hspace{1cm} \text{M45}

Description:

The instruction and data translation cache for each processor in the local TLB coherence domain are searched for all entries whose virtual address and page size partially or completely overlap the specified purge virtual address and purge address range. These entries are removed.

The purge virtual address is specified by GR \(r_3\) bits \{60:0\} and the purge region identifier is selected by GR \(r_3\) bits \{63:61\}. GR \(r_2\) specifies the address range of the purge as \(1\ll GR[r_2]\{7:2\}\) bytes in size.

Based on the processor model, the translation cache may be also purged of more translations than specified by the purge parameters up to and including removal of all entries within the translation cache.

ptc.g has release semantics and is guaranteed to be made visible after all previous data memory accesses are made visible. The memory fence instruction forces all processors to complete the purge prior to any subsequent memory operations. Serialization is still required to observe the side-effects of a translation being removed.

ptc.g must be the last instruction in an instruction group; otherwise, its behavior (including its ordering semantics) is undefined.

The behavior of the ptc.ga instruction is similar to ptc.g. In addition to the behavior specified for ptc.g the ptc.ga instruction encodes an extra bit of information in the broadcast transaction. This information specifies the purge is due to a page remapping as opposed to a protection change or page tear down. The remote processors within the coherence domain will then take what ever additional action is necessary to make their ALAT consistent. The local ALAT is not purged.

This instruction can only be executed at the most privileged level.

Only one global purge transaction may be issued at a time by all processors, the operation is undefined otherwise. Software is responsible for enforcing this restriction.

Propagation of ptc.g between multiple local TLB coherence domains is platform dependent, and must be handled by software. It is expected that the local TLB coherence domain covers at least the processors on the same local bus.
Operation:
if (PR[qp]) {
  if (!followed_by_stop())
    undefined_behavior();
  if (PSR.cpl != 0)
    privileged_operation_fault(0);
  if (GR[r3].nat || GR[r2].nat)
    register_nat_consumption_fault(0);
  if (unimplemented_virtual_address(GR[r3]))
    unimplemented_data_address_fault(0);

  tmp_rid = RR[GR[r3][63:61]].rid;
  tmp_va = GR[r3][60:0];
  tmp_size = GR[r2][7:2];
  tmp_va = align_to_size_boundary(tmp_va, tmp_size);
  tlb_must_purge_dtc_entries(tmp_rid, tmp_va, tmp_size);
  tlb_must_purge_itc_entries(tmp_rid, tmp_va, tmp_size);
  if (global_alat_form) tmp_ptc_type = GLOBAL_ALAT_FORM;
  else tmp_ptc_type = GLOBAL_FORM;

  tlb_broadcast_purge(tmp_rid, tmp_va, tmp_size, tmp_ptc_type);}

Interruptions:
Machine Check abort
Privileged Operation fault
Register NaT Consumption fault
Unimplemented Data Address fault

Serialization:
The broadcast purge TC is not synchronized with the instruction stream on a remote processor.
Software cannot depend on any such synchronization with the instruction stream. Hardware on the
remote machine cannot reload an instruction from memory or cache after acknowledging a
broadcast purge TC without first retranslating the I-side access in the TLB. Hardware may continue
to use a valid private copy of the instruction stream data (possibly in an I-buffer) obtained prior to
acknowledging a broadcast purge TC to a page containing the i-stream data. Hardware must
retranslate access to an instruction page upon an interruption or any explicit or implicit instruction
serialization event (e.g., srlz.i, rfi).

Software must issue the appropriate data and/or instruction serialization operation to ensure the
purge is completed before a local data access, non-access reference, or local instruction fetch access
dependent upon the purge.
ptc.l — Purge Local Translation Cache

Format: \((qp)\) ptc.l \(r_3\), \(r_2\)

Description: The instruction and data translation cache of the local processor is searched for all entries whose virtual address and page size partially or completely overlap the specified purge virtual address and purge address range. All these entries are removed.

The purge virtual address is specified by GR\(r_3\) bits\{60:0\} and the purge region identifier is selected by GR\(r_3\) bits \{63:61\}. GR\(r_2\) specifies the address range of the purge as \(1^{\text{<}}\text{GR}[r_2]\{7:2\}\) bytes in size.

The processor ensures that all entries matching the purging parameters are removed. However, based on the processor model, the translation cache may be also purged of more translations than specified by the purge parameters up to and including removal of all entries within the translation cache.

This instruction can only be executed at the most privileged level.

This is a local operation, no purge broadcast to other processors occurs in a multiprocessor system.

Operation:

```c
if (PR[qp]) {
    if (PSR.cpl != 0)
        privileged_operation_fault(0);
    if (GR[r_3].nat || GR[r_2].nat)
        register_nat_consumption_fault(0);
    if (unimplemented_virtual_address(GR[r_3]))
        unimplemented_data_address_fault(0);

    tmp_rid = RR[GR[r_3]\{63:61\}].rid;
    tmp_va = GR[r_3]\{60:0\};
    tmp_size = GR[r_2]\{7:2\};
    tmp_va = align_to_size_boundary(tmp_va, tmp_size);
    tlb_must_purge_dtc_entries(tmp_rid, tmp_va, tmp_size);
    tlb_must_purge_itc_entries(tmp_rid, tmp_va, tmp_size);
}
```

Interruptions: Machine Check abort  Register NaT Consumption fault
Privileged Operation fault  Unimplemented Data Address fault

Serialization: Software must issue the appropriate data and/or instruction serialization operation to ensure the purge is completed before a data access, non-access reference, or instruction fetch access dependent upon the purge.
ptr — Purge Translation Register

**Format:**

\[(qp)\] ptr.d \(r_3, r_2\)  
\[(qp)\] ptr.i \(r_3, r_2\)

**Description:**

In the data form of this instruction, the data translation registers and caches are searched for all entries whose virtual address and page size partially or completely overlap the specified purge virtual address and purge address range. All these entries are removed. Entries in the instruction translation registers are unaffected by the data form of the purge.

In the instruction form, the instruction translation registers and caches are searched for all entries whose virtual address and page size partially or completely overlap the specified purge virtual address and purge address range. All these entries are removed. Entries in the data translation registers are unaffected by the instruction form of the purge.

In addition, in both forms, the instruction and data translation cache may be purged of more translations than specified by the purge parameters up to and including removal of all entries within the translation cache.

The purge virtual address is specified by GR \(r_3\) bits \(60:0\) and the purge region identifier is selected by GR \(r_3\) bits \(63:61\). GR \(r_2\) specifies the address range of the purge as \(1<<GR[r_2]\)\(7:2\) bytes in size.

This instruction can only be executed at the most privileged level.

This is a local operation, no purge broadcast to other processors occurs in a multiprocessor system.

As described in Section 4.1.1.2, “Translation Cache (TC)” on page 2:40, the processor may use the translation caches to cache virtual address mappings held by translation registers. The ptr.i and ptr.d instructions purge the processor’s translation registers as well as cached translation register copies that may be contained in the respective translation caches.
Operation:

\[
\text{if } (\text{PR}[qp]) \{ \\
\quad \text{if } (\text{PSR.cpl} != 0) \\
\quad \quad \text{privileged_operation_fault}(0); \\
\quad \text{if } (\text{GR}[r_3].\text{nat} || \text{GR}[r_2].\text{nat}) \\
\quad \quad \text{register_nat_consumption_fault}(0); \\
\text{if } (\text{unimplemented_virtual_address} \text{GR}[r_3]) \\
\quad \quad \text{unimplemented_data_address_fault}(0); \\
\}
\]

\[
tmp\_rid = \text{RR}[\text{GR}[r_3]{63:61}].\text{rid}; \\
tmp\_va = \text{GR}[r_3]{60:0}; \\
tmp\_size = \text{GR}[r_2]{7:2}; \\
tmp\_va = \text{align}\_to\_size\_boundary \text{tmp\_va, tmp\_size}; \\
\]

\[
\text{if } (\text{data\_form}) \{ \\
\text{tlb\_must\_purge\_dtr\_entries}(\text{tmp\_rid}, \text{tmp\_va}, \text{tmp\_size}); \\
\text{tlb\_must\_purge\_dtc\_entries}(\text{tmp\_rid}, \text{tmp\_va}, \text{tmp\_size}); \\
\text{tlb\_may\_purge\_itc\_entries}(\text{tmp\_rid}, \text{tmp\_va}, \text{tmp\_size}); \\
\} \quad \text{else} \quad \text{instruction\_form} \\
\text{tlb\_must\_purge\_itr\_entries}(\text{tmp\_rid}, \text{tmp\_va}, \text{tmp\_size}); \\
\text{tlb\_must\_purge\_itc\_entries}(\text{tmp\_rid}, \text{tmp\_va}, \text{tmp\_size}); \\
\text{tlb\_may\_purge\_dtc\_entries}(\text{tmp\_rid}, \text{tmp\_va}, \text{tmp\_size}); \\
\}
\]

Interruptions: Privileged Operation fault, Unimplemented Data Address fault, Register NaT Consumption fault

Serialization: For the data form, software must issue a data serialization operation to ensure the purge is completed before issuing an instruction dependent upon the purge. For the instruction form, software must issue an instruction serialization operation to ensure the purge is completed before fetching an instruction dependent on that purge.
rfi — Return From Interruption

Format: rfi

Description: The machine context prior to an interruption is restored. PSR is restored from IPSR, IPSR is unmodified, and IP is restored from IIP. Execution continues at the bundle address loaded into the IP, and the instruction slot loaded into PSR.ri.

This instruction must be immediately followed by a stop. Otherwise, an Illegal Operation fault is taken. This instruction switches to the register bank specified by IPSR.bn. Instructions in the same instruction group that access GR16 to GR31 reference the previous register bank. Subsequent instruction groups reference the new register bank.

This instruction performs instruction serialization, which ensures:

• prior modifications to processor register resources that affect fetching of subsequent instruction groups are observed.
• prior modifications to processor register resources that affect subsequent execution or data memory accesses are observed.
• prior memory synchronization (sync.i) operations have taken effect on the local processor instruction cache.
• subsequent instruction group fetches (including the target instruction group) are re-initiated after rfi completes.

The rfi instruction must be in an instruction group after the instruction group containing the operation that is to be serialized.

This instruction can only be executed at the most privileged level. This instruction cannot be predicated.

Execution of this instruction is undefined if PSR.ic or PSR.i are 1. Software must ensure that an interruption cannot occur that could modify IIP, IPSR, or IFS between when they are written and the subsequent rfi.

This instruction does not take Lower Privilege Transfer, Taken Branch or Single Step traps.

If this instruction sets PSR.ri to 2 and the target is an MLX bundle, then an Illegal Operation fault will be taken on the target bundle.

If IPSR.is is 1, control is resumed in the IA-32 instruction set at the virtual linear address specified by IIP{31:0}. PSR.di does not inhibit instruction set transitions for this instruction. If PSR.dfh is 1 after rfi completes execution, a Disabled FP Register fault is raised on the target IA-32 instruction.

If IPSR.is is 1 and an Unimplemented Instruction Address trap is taken, IIP will contain the original 64-bit target IP. (The value will not have been zero extended from 32 bits.)

When entering the IA-32 instruction set, the size of the current stack frame is set to zero, and all stacked general registers are left in an undefined state. Software cannot rely on the value of these registers across an instruction set transition. Software must ensure that BSPSTORE==BSP on entry to the IA-32 instruction set, otherwise undefined behavior may result.

Software must issue a mf instruction before this instruction if memory ordering is required between IA-32 processor-consistent and Itanium unordered memory references. The processor does not ensure Itanium-instruction-set-generated writes into the instruction stream are seen by subsequent IA-32 instructions.
Software must ensure the code segment descriptor and selector are loaded before issuing this instruction. If the target EIP value exceeds the code segment limit or has a code segment privilege violation, an IA-32_Exception(GPFault) exception is raised on the target IA-32 instruction. For entry into 16-bit IA-32 code, if IIP is not within 64K-bytes of CSD.base a GPFault is raised on the target instruction.

EFLAGS.rf and PSR.id are unmodified until the successful completion of the target IA-32 instruction. PSR.da, PSR.dd, PSR.ia and PSR.ed are cleared to zero before the target IA-32 instruction begins execution.

IA-32 instruction set execution leaves the contents of the ALAT undefined. Software can not rely on ALAT state across an instruction set transition. On entry to IA-32 code, existing entries in the ALAT are ignored.

**Operation:**

```c
if (!followed_by_stop())
    illegal_operation_fault();

unimplemented_address = 0;
if (PSR.cpl != 0)
    privileged_operation_fault(0);

taken_rfi = 1;

PSR = CR[IPSR];
if (CR[IPSR].is == 1) { //resume IA-32 instruction set
    tmp_IP = CR[IIP];
    if (!CR[IPSR].it && unimplemented_virtual_address(tmp_IP))
        unimplemented_address = 1;
    //compute effective instruction pointer
    EIP{31:0} = CR[IIP]{31:0} - AR[CSD].Base;
    //force zero-sized restored frame
    rse_restore_frame(0, 0, CFM.sof);
    CFM.sof = 0;
    CFM.sol = 0;
    CFM.sor = 0;
    CFM.rrb.gr = 0;
    CFM.rrb.fr = 0;
    CFM.rrb.pr = 0;
    rse_invalidate_non_current_regs();
    //The register stack engine is disabled during IA-32
    //instruction set execution.
} else { //return to Itanium instruction set
    tmp_IP = CR[IIP] & ~0xf;
    slot = CR[IPSR].ri;
    if (!CR[IPSR].it && unimplemented_virtual_address(tmp_IP))
        unimplemented_address = 1;
    if (CR[IFS].v) {
        tmp_growth = -CFM.sof;
        alat_frame_update(-CR[IFS].ifm.sof, 0);
        rse_restore_frame(CR[IFS].ifm.sof, tmp_growth, CFM.sof);
        CFM = CR[IFS].ifm;
    }
    rse_enable_current_frame_load();
}
IP = tmp_IP;
instruction_serialize();
if (unimplemented_address)
    unimplemented_instruction_address_trap(0, tmp_IP);
```
**Interruptions:**  Illegal Operation fault  
Unimplemented Instruction Address trap  
Additional Faults on IA-32 target instructions  
IA-32_Exception(GPFault)  
Disabled FP Reg Fault if PSR.dfh is 1

**Serialization:**  An implicit instruction and data serialization operation is performed.
**rsm — Reset System Mask**

**Format:**  
\((qp)\) rsm \(imm_{24}\)

**Description:**  
The complement of the \(imm_{24}\) operand is ANDed with the system mask (PSR\(\{23:0\}\)) and the result is placed in the system mask. See Section 3.3.2, “Processor Status Register (PSR)” on page 2:18.

The PSR system mask can only be written at the most privileged level.

When the current privilege level is zero (PSR.cpl is 0), an \(rsm\) instruction whose mask includes PSR.i may cause external interrupts to be disabled for an implementation-dependent number of instructions, even if the qualifying predicate for the \(rsm\) instruction is false. Architecturally, the extents of this external interrupt disabling “window” are defined as follows:

- External interrupts may be disabled for any instructions in the same instruction group as the \(rsm\), including those that precede the \(rsm\) in sequential program order, regardless of the value of the qualifying predicate of the \(rsm\) instruction.
- If the qualifying predicate of the \(rsm\) is true, then external interrupts are disabled immediately following the \(rsm\) instruction.
- If the qualifying predicate of the \(rsm\) is false, then external interrupts may be disabled until the next data serialization operation that follows the \(rsm\) instruction.

The external interrupt disable window is guaranteed to be no larger than defined by the above criteria, but it may be smaller, depending on the processor implementation.

When the current privilege level is non-zero (PSR.cpl is not 0), an \(rsm\) instruction whose mask includes PSR.i may briefly disable external interrupts, regardless of the value of the qualifying predicate of the \(rsm\) instruction. However, processor implementations guarantee that non-privileged code cannot lock out external interrupts indefinitely (e.g., via an arbitrarily long sequence of \(rsm\) instructions with zero-valued qualifying predicates).

**Operation:**  
```c
if (PR[qp]) {
    if (PSR.cpl != 0)
        privileged_operation_fault(0);
    if (is_reserved_field(PSR_TYPE, PSR_SM, \ imm_{24}\))
        reserved_register_field_fault();
    if (imm_{24}{1}) PSR{1} = 0; // be
    if (imm_{24}{2}) PSR{2} = 0; // up
    if (imm_{24}{3}) PSR{3} = 0; // ac
    if (imm_{24}{4}) PSR{4} = 0; // mfl
    if (imm_{24}{5}) PSR{5} = 0; // mfh
    if (imm_{24}{13}) PSR{13} = 0; // ic
    if (imm_{24}{14}) PSR{14} = 0; // i
    if (imm_{24}{15}) PSR{15} = 0; // pk
    if (imm_{24}{17}) PSR{17} = 0; // dt
    if (imm_{24}{18}) PSR{18} = 0; // dfl
    if (imm_{24}{19}) PSR{19} = 0; // dfh
    if (imm_{24}{20}) PSR{20} = 0; // sp
    if (imm_{24}{21}) PSR{21} = 0; // pp
    if (imm_{24}{22}) PSR{22} = 0; // di
    if (imm_{24}{23}) PSR{23} = 0; // si
}
```

**Interruptions:**  
- Privileged Operation fault
- Reserved Register/Field fault
**Serialization:** Software must use a data serialize or instruction serialize operation before issuing instructions dependent upon the altered PSR bits – except the PSR.i bit. The PSR.i bit is implicitly serialized and the processor ensures that external interrupts are masked by the time the next instruction executes.
rum — Reset User Mask

Format: \((qp) \text{ run } \text{imm}_2^4\)

Description: The complement of the \(\text{imm}_2^4\) operand is ANDed with the user mask (PSR\{5:0\}) and the result is placed in the user mask. See Section 3.3.2, “Processor Status Register (PSR)” on page 2:18.

PSR.up is only cleared if the secure performance monitor bit (PSR.sp) is zero. Otherwise PSR.up is not modified.

Operation:

\[
\begin{align*}
\text{if (PR[qp])} & \{
\text{if (is_reserved_field(PSR\_TYPE, PSR\_UM, \text{imm}_2^4))}
\quad \text{reserved_register_field_fault();}
\text{if (imm}_2^4(1)) & \quad \text{PSR}_1 = 0; \quad \text{// be}
\text{if (imm}_2^4(2) & PSR.sp == 0) & \quad \text{//non-secure perf monitor}
\quad \text{PSR}_2 = 0; \quad \text{// up}
\text{if (imm}_2^4(3)) & \quad \text{PSR}_3 = 0; \quad \text{// ac}
\text{if (imm}_2^4(4)) & \quad \text{PSR}_4 = 0; \quad \text{// mfl}
\text{if (imm}_2^4(5)) & \quad \text{PSR}_5 = 0; \quad \text{// mfh}
\}\n\end{align*}
\]

Interruptions: Reserved Register/Field fault

Serialization: All user mask modifications are observed by the next instruction group.
**setf — Set Floating-point Value, Exponent, or Significand**

**Format:**

- \((qp)\) setf.s \(f_1 = r_2\)  
- \((qp)\) setf.d \(f_1 = r_2\)  
- \((qp)\) setf.exp \(f_1 = r_2\)  
- \((qp)\) setf.sig \(f_1 = r_2\)

**single_form M18**

- \((qp)\) setf.s \(f_1 = r_2\)  
- \((qp)\) setf.d \(f_1 = r_2\)  
- \((qp)\) setf.exp \(f_1 = r_2\)  
- \((qp)\) setf.sig \(f_1 = r_2\)

**double_form M18**

- \((qp)\) setf.s \(f_1 = r_2\)  
- \((qp)\) setf.d \(f_1 = r_2\)  
- \((qp)\) setf.exp \(f_1 = r_2\)  
- \((qp)\) setf.sig \(f_1 = r_2\)

**exponent_form M18**

- \((qp)\) setf.exp \(f_1 = r_2\)

**significand_form M18**

- \((qp)\) setf.sig \(f_1 = r_2\)

**Description:**

In the single and double forms, GR \(r_2\) is treated as a single precision (in the single_form) or double precision (in the double_form) memory representation, converted into floating-point register format, and placed in FR \(f_1\), as shown in Figure 5-7 and Figure 5-8 on page 1:85, respectively.

In the exponent_form, bits 16:0 of GR \(r_2\) are copied to the exponent field of FR \(f_1\) and bit 17 of GR \(r_2\) is copied to the sign bit of FR \(f_1\). The significand field of FR \(f_1\) is set to one (0x800...000).

**Figure 2-41. Function of setf.exp**

In the significand_form, the value in GR \(r_2\) is copied to the significand field of FR \(f_1\).

The exponent field of FR \(f_1\) is set to the biased exponent for 2.063 (0x1003E) and the sign field of FR \(f_1\) is set to positive (0).

**Figure 2-42. Function of setf.sig**

For all forms, if the NaT bit corresponding to \(r_2\) is equal to 1, FR \(f_1\) is set to NaTVal instead of the computed result.
Operation:  
if (PR[qp]) {
    fp_check_target_register(f1);
    if (tmp_isrcode = fp_reg_disabled(f1, 0, 0, 0))
        disabled_fp_register_fault(tmp_isrcode, 0);

    if (!GR[r2].nat) {
        if (single_form)
            FR[f1] = fp_mem_to_fr_format(GR[r2], 4, 0);
        else if (double_form)
            FR[f1] = fp_mem_to_fr_format(GR[r2], 8, 0);
        else if (significand_form) {
            FR[f1].significand = GR[r2];
            FR[f1].exponent = FP_INTEGER_EXP;
            FR[f1].sign = 0;
        } else {// exponent_form
            FR[f1].significand = 0x8000000000000000;
            FR[f1].exp = GR[r2][16:0];
            FR[f1].sign = GR[r2][17];
        }
    } else
        FR[f1] = NATVAL;

    fp_update_psr(f1);
}

Interruptions:  
Illegal Operation fault  
Disabled Floating-point Register fault
shl — Shift Left

Format:  

- \((qp)\) shl \(r_j = r_2, r_3\)  
- \((qp)\) shl \(r_j = r_2, count_6\)  
- \(\text{pseudo-op of: } (qp) \text{ dep.z } r_j = r_2, count_6, 64 - count_6\)

Description:  
The value in GR \(r_2\) is shifted to the left, with the vacated bit positions filled with zeroes, and placed in GR \(r_j\). The number of bit positions to shift is specified by the value in GR \(r_3\) or by an immediate value \(count_6\). The shift count is interpreted as an unsigned number. If the value in GR \(r_3\) is greater than 63, then the result is all zeroes.

See “dep — Deposit” on page 3:45 for the immediate form.

Operation:  

if \((PR[qp])\) {  
  check_target_register\(r_j\);  
  count = GR\[r_3\];  
  GR\[r_j\] = (count > 63) ? 0 : GR\[r_2\] \(\ll\) count;  
  GR\[r_j\].nat = GR\[r_2\].nat || GR\[r_3\].nat;  
}

Interruptions:  
Illegal Operation fault
shladd — Shift Left and Add

Format: \((qp)\) shladd \(r_1 = r_2, count_2, r_3\)

Description: The first source operand is shifted to the left by \(count_2\) bits and then added to the second source operand and the result placed in GR \(r_1\). The first operand can be shifted by 1, 2, 3, or 4 bits.

Operation:

\[
\begin{array}{l}
\text{if (PR[qp])} \\
\quad \text{check_target_register}(r_1); \\
\quad \text{GR}[r_1] = (\text{GR}[r_2] << count_2) + \text{GR}[r_3]; \\
\quad \text{GR}[r_1].\text{nat} = \text{GR}[r_2].\text{nat} \; \text{||} \; \text{GR}[r_3].\text{nat}; \\
\end{array}
\]

Interruptions: Illegal Operation fault
shladdp4 — Shift Left and Add Pointer

Format: \((qp)\) shladdp4 \(r_1 = r_2, count_2, r_3\)

Description: The first source operand is shifted to the left by \(count_2\) bits and then is added to the second source operand. The upper 32 bits of the result are forced to zero, and then bits \(31:30\) of GR \(r_3\) are copied to bits \(62:61\) of the result. This result is placed in GR \(r_1\). The first operand can be shifted by 1, 2, 3, or 4 bits.

Operation:

\[
\begin{align*}
&\text{if (PR[qp])} \{ \\
&\quad \text{check_target_register}(r_1); \\
&\quad \text{tmp\_res} = (\text{GR}[r_2] \ll count_2) + \text{GR}[r_3]; \\
&\quad \text{tmp\_res} = \text{zero\_ext}((\text{tmp\_res}[31:0]), 32); \\
&\quad \text{tmp\_res}[62:61] = \text{GR}[r_3][31:30]; \\
&\quad \text{GR}[r_1] = \text{tmp\_res}; \\
&\quad \text{GR}[r_1].nat = \text{GR}[r_2].nat \ || \ \text{GR}[r_3].nat; \\
&\}\end{align*}
\]

Interruptions: Illegal Operation fault
shr — Shift Right

Format:

- `(qp) shr r_j, r_2` 
  - `signed_form` 15
- `(qp) shr.u r_j, r_2` 
  - `unsigned_form` 15
- `(qp) shr r_j = r_3, count_6` 
  - pseudo-op of: `(qp) extr r_j = r_3, count_6, 64–count_6`
- `(qp) shr.u r_j = r_3, count_6` 
  - pseudo-op of: `(qp) extr.u r_j = r_3, count_6, 64–count_6`

Description:
The value in GR `r_3` is shifted to the right and placed in GR `r_1`. In the `signed_form` the vacated bit positions are filled with bit 63 of GR `r_3`; in the `unsigned_form` the vacated bit positions are filled with zeroes. The number of bit positions to shift is specified by the value in GR `r_2` or by an immediate value `count_6`. The shift count is interpreted as an unsigned number. If the value in GR `r_2` is greater than 63, then the result is all zeroes (for the `unsigned_form`, or if bit 63 of GR `r_3` was 0) or all ones (for the `signed_form` if bit 63 of GR `r_3` was 1).

If the .u completer is specified, the shift is unsigned (logical), otherwise it is signed (arithmetic).

See “extr — Extract” on page 3:48 for the immediate forms.

Operation:

```c
if (PR[qp]) {
    check_target_register(r_j);
    if (signed_form) {
        count = (GR[r_2] > 63) ? 63 : GR[r_2];
        GR[r_j] = shift_right_signed(GR[r_3], count);
    } else {
        count = GR[r_2];
        GR[r_j] = (count > 63) ? 0 : shift_right_unsigned(GR[r_3], count);
    }
    GR[r_j].nat = GR[r_2].nat | GR[r_3].nat;
}
```

Interruptions: Illegal Operation fault
shrp — Shift Right Pair

Format: \((qp) \text{ shrp } r_1 = r_2, r_3, \text{count}_6\)

Description: The two source operands, GR\( r_2 \) and GR\( r_3 \), are concatenated to form a 128-bit value and shifted to the right \(\text{count}_6\) bits. The least-significant 64 bits of the result are placed in GR\( r_1 \).

The immediate value \(\text{count}_6\) can be any number in the range 0 to 63.

**Figure 2-44. Shift Right Pair**

```
Operation: if (PR[qp]) {
  check_target_register(r_1);
  temp1 = shift_right_unsigned(GR[r_3], \text{count}_6);
  temp2 = GR[r_2] \ll (64 - \text{count}_6);
  GR[r_1] = zero_ext(temp1, 64 - \text{count}_6) | temp2;
  GR[r_1].nat = GR[r_2].nat || GR[r_3].nat;
}
```

Interruptions: Illegal Operation fault
srlz — Serialize

Format: 

- \((qp)\) srlz.i instruction_form M24
- \((qp)\) srlz.d data_form M24

Description: Instruction serialization (srlz.i) ensures:

- prior modifications to processor register resources that affect fetching of subsequent instruction groups are observed,
- prior modifications to processor register resources that affect subsequent execution or data memory accesses are observed,
- prior memory synchronization (sync.i) operations have taken effect on the local processor instruction cache,
- subsequent instruction group fetches are re-initiated after srlz.i completes.

The srlz.i instruction must be in an instruction group after the instruction group containing the operation that is to be serialized. Operations dependent on the serialization must be in an instruction group after the instruction group containing the srlz.i.

Data serialization (srlz.d) ensures:

- prior modifications to processor register resources that affect subsequent execution or data memory accesses are observed.

The srlz.d instruction must be in an instruction group after the instruction group containing the operation that is to be serialized. Operations dependent on the serialization must follow the srlz.d, but they can be in the same instruction group as the srlz.d.

A srlz cannot be used to stall processor data memory references until prior data memory references, or memory fences are visible or “accepted” by the external platform.

The following processor resources require a serialize to ensure side-effects are observed; CRs, PSR, DBRs, IBRs, PMDs, PMCs, RRs, PKRs, TRs and TCs (refer to Section 3.2, “Serialization” on page 2:13 for details).

Operation:

```c
if (PR[qp]) {
    if (instruction_form)
        instruction_serialize();
    else // data_form
        data_serialize();
}
```

Interruptions: None
ssm — Set System Mask

Format: 
\[(qp) \text{ ssm imm}_{24}\]

Description: The \( \text{imm}_{24} \) operand is ORed with the system mask (PSR\{23:0\}) and the result is placed in the system mask. See Section 3.3.2, “Processor Status Register (PSR)” on page 2:18.

The PSR system mask can only be written at the most privileged level.

The contents of the interruption resources (that are overwritten when the PSR.ic bit is 1), are undefined if an interruption occurs between the enabling of the PSR.ic bit and a subsequent instruction serialize operation.

Operation:
\[
\text{if } (\text{PR[qp]}) \{ \\
\quad \text{if } (\text{PSR.cpl} != 0) \\
\quad \quad \text{privileged_operation_fault}(0); \\
\quad \text{if } (\text{is_reserved_field}(\text{PSR_TYPE, PSR_SM, } \text{imm}_{24})) \\
\quad \quad \text{reserved_register_field_fault}();
\]

\[
\quad \text{if } (\text{imm}_{24}\{1\}) \text{ PSR}\{1\} = 1; \quad \text{// be} \\
\quad \text{if } (\text{imm}_{24}\{2\}) \text{ PSR}\{2\} = 1; \quad \text{// up} \\
\quad \text{if } (\text{imm}_{24}\{3\}) \text{ PSR}\{3\} = 1; \quad \text{// ac} \\
\quad \text{if } (\text{imm}_{24}\{4\}) \text{ PSR}\{4\} = 1; \quad \text{// mfl} \\
\quad \text{if } (\text{imm}_{24}\{5\}) \text{ PSR}\{5\} = 1; \quad \text{// mfh} \\
\quad \text{if } (\text{imm}_{24}\{13\}) \text{ PSR}\{13\} = 1; \quad \text{// ic} \\
\quad \text{if } (\text{imm}_{24}\{14\}) \text{ PSR}\{14\} = 1; \quad \text{// i} \\
\quad \text{if } (\text{imm}_{24}\{15\}) \text{ PSR}\{15\} = 1; \quad \text{// pk} \\
\quad \text{if } (\text{imm}_{24}\{17\}) \text{ PSR}\{17\} = 1; \quad \text{// dt} \\
\quad \text{if } (\text{imm}_{24}\{18\}) \text{ PSR}\{18\} = 1; \quad \text{// dfl} \\
\quad \text{if } (\text{imm}_{24}\{19\}) \text{ PSR}\{19\} = 1; \quad \text{// dfh} \\
\quad \text{if } (\text{imm}_{24}\{20\}) \text{ PSR}\{20\} = 1; \quad \text{// sp} \\
\quad \text{if } (\text{imm}_{24}\{21\}) \text{ PSR}\{21\} = 1; \quad \text{// pp} \\
\quad \text{if } (\text{imm}_{24}\{22\}) \text{ PSR}\{22\} = 1; \quad \text{// di} \\
\quad \text{if } (\text{imm}_{24}\{23\}) \text{ PSR}\{23\} = 1; \quad \text{// si}
\}

Interruptions: Privileged Operation fault

Reserved Register/Field fault

Serialization: Software must issue a data serialize or instruction serialize operation before issuing instructions dependent upon the altered PSR bits from the \text{ssm} instruction. Unlike with the \text{rsm} instruction, setting the PSR.i bit is not treated specially. Refer to Section 3.2, “Serialization” on page 2:13 for a description of serialization.
st — Store

Format:

- \( \text{stsz}, \text{sttype}, \text{sthint} \ [r_3] = r_2 \)  
  normal_form, no_base_update_form  
  M4
- \( \text{stsz}, \text{sttype}, \text{sthint} \ [r_3] = r_2, \text{imm}_9 \)  
  normal_form, imm_base_update_form  
  M5
- \( \text{st16}, \text{sttype}, \text{sthint} \ [r_3] = r_2, \text{ar.csd} \)  
  sixteen_byte_form, no_base_update_form  
  M4
- \( \text{st8}, \text{spill}, \text{sthint} \ [r_3] = r_2 \)  
  spill_form, no_base_update_form  
  M4
- \( \text{st8}, \text{spill}, \text{sthint} \ [r_3] = r_2, \text{imm}_9 \)  
  spill_form, imm_base_update_form  
  M5

Description:

A value consisting of the least significant \( sz \) bytes of the value in GR \( r_2 \) is written to memory starting at the address specified by the value in GR \( r_3 \). The values of the \( sz \) completer are given in Table 2-32 on page 3:131. The \( sttype \) completer specifies special store operations, which are described in Table 2-49. If the NaT bit corresponding to GR \( r_3 \) is 1, or in sixteen_byte_form or normal_form, if the NaT bit corresponding to GR \( r_2 \) is 1, a Register NaT Consumption fault is taken.

In the sixteen_byte_form, two 8-byte values are stored as a single, 16-byte atomic memory write. The value in GR \( r_2 \) is written to memory starting at the address specified by the value in GR \( r_3 \). The value in the Compare and Store Data application register (AR[CSD]) is written to memory starting at the address specified by the value in GR \( r_3 \) plus 8.

In the spill_form, an 8-byte value is stored, and the NaT bit corresponding to GR \( r_2 \) is copied to a bit in the UNAT application register. This instruction is used for spilling a register/NaT pair. See Section 4.4.4, “Control Speculation” on page 1:51 for details.

In the imm_base_update form, the value in GR \( r_3 \) is added to a signed immediate value (\( \text{imm}_9 \)) and the result is placed back in GR \( r_3 \). This base register update is done after the store, and does not affect the store address, nor the value stored (for the case where \( r_2 \) and \( r_3 \) specify the same register). Base register update is not supported for the \( \text{st16} \) instruction.

Table 2-49. Store Types

<table>
<thead>
<tr>
<th>( sttype ) Completer</th>
<th>Interpretation</th>
<th>Special Store Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Normal store</td>
<td>An ordered store is performed with release semantics.</td>
</tr>
<tr>
<td>rel</td>
<td>Ordered store</td>
<td></td>
</tr>
</tbody>
</table>

For more details on ordered stores see Section 4.4.7, “Memory Access Ordering” on page 1:63.

The ALAT is queried using the physical memory address and the access size, and all overlapping entries are invalidated.

The value of the \( sthint \) completer specifies the locality of the memory access. The values of the \( sthint \) completer are given in Table 2-50. A prefetch hint is implied in the base update forms. The address specified by the value in GR \( r_3 \) after the base update acts as a hint to prefetch the indicated cache line. This prefetch uses the locality hints specified by \( sthint \). See Section 4.4.6, “Memory Hierarchy Control and Consistency” on page 1:60.

Hardware support for \( \text{st16} \) instructions that reference a page that is neither a cacheable page with write-back policy nor a NaTPage is optional. On processor models that do not support such \( \text{st16} \) accesses, an Unsupported Data Reference fault is raised when an unsupported reference is attempted.
### Table 2-50. Store Hints

<table>
<thead>
<tr>
<th>sthint</th>
<th>Completer Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>none</td>
<td>Temporal locality, level 1</td>
</tr>
<tr>
<td>nta</td>
<td>Non-temporal locality, all levels</td>
</tr>
</tbody>
</table>

#### Operation:

```c
if (PR[qp]) {
    size = spill_form ? 8 : (sixteen_byte_form ? 16 : sz);
    itype = WRITE;
    if (size == 16) itype |= UNCACHE_OPT;
    otype = (sttype == 'rel') ? RELEASE : UNORDERED;

    if (imm_base_update_form)
        check_target_register(r3);
    if (GR[r3].nat || ((sixteen_byte_form || normal_form) && GR[r2].nat))
        register_nat_consumption_fault(WRITE);

    paddr = tlb_translate(GR[r3], size, itype, PSR.cpl, &mattr, &tmpUnused);
    if (spill_form && GR[r2].nat)
        natd_gr_write(GR[r2], paddr, size, UM.be, mattr, otype, sthint);
    else {
        if (sixteen_byte_form)
            mem_write16(GR[r2], AR[CSD], paddr, UM.be, mattr, otype, sthint);
        else
            mem_write(GR[r2], paddr, size, UM.be, mattr, otype, sthint);
    }

    if (spill_form) {
        bit_pos = GR[r3]{8:3};
        AR[UNAT]{bit_pos} = GR[r2].nat;
    }

    alat_inval_multiple_entries(paddr, size);

    if (imm_base_update_form) {
        GR[r3] = GR[r3] + sign_ext(imm9, 9);
        GR[r3].nat = 0;
        mem_implicit_prefetch(GR[r3], sthint, WRITE);
    }
}
```

#### Interruptions:

- Illegal Operation fault
- Register NaT Consumption fault
- Unimplemented Data Address fault
- Data Nested TLB fault
- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault
- Data NaT Page Consumption fault
- Data Key Miss fault
- Data Key Permission fault
- Data Access Rights fault
- Data Dirty Bit fault
- Data Access Bit fault
- Data Debug fault
- Unaligned Data Reference fault
- Unsupported Data Reference fault
stf — Floating-point Store

Format: 

\[(ap) \text{stf(sz).sthint } [r_3] = f_2\]  
\[\text{normal_form, no_base_update_form M9}\]

\[(ap) \text{stf(sz).sthint } [r_3] = f_2, \text{imm}_9\]  
\[\text{normal_form, imm_base_update_form M10}\]

\[(ap) \text{stf8.sthint } [r_3] = f_2\]  
\[\text{integer_form, no_base_update_form M9}\]

\[(ap) \text{stf8.sthint } [r_3] = f_2, \text{imm}_9\]  
\[\text{integer_form, imm_base_update_form M10}\]

\[(ap) \text{stf.spill.sthint } [r_3] = f_2\]  
\[\text{spill_form, no_base_update_form M9}\]

\[(ap) \text{stf.spill.sthint } [r_3] = f_2, \text{imm}_9\]  
\[\text{spill_form, imm_base_update_form M10}\]

Description: A value, consisting of \(fsz\) bytes, is generated from the value in FR \(f_2\) and written to memory starting at the address specified by the value in GR \(r_3\). In the normal_form, the value in FR \(f_2\) is converted to the memory format and then stored. In the integer_form, the significand of FR \(f_2\) is stored. The values of the \(fsz\) completer are given in Table 2-35 on page 3:135. In the normal_form or the integer_form, if the NaT bit corresponding to GR \(r_3\) is 1 or if FR \(f_2\) contains NaTVal, a Register NaT Consumption fault is taken. See Section 5.1, “Data Types and Formats” on page 1:75 for details on conversion from floating-point register format.

In the spill_form, a 16-byte value from FR \(f_2\) is stored without conversion. This instruction is used for spilling a register. See Section 4.4.4, “Control Speculation” on page 1:51 for details.

In the imm_base_update form, the value in GR \(r_3\) is added to a signed immediate value (\(\text{imm}_9\)) and the result is placed back in GR \(r_3\). This base register update is done after the store, and does not affect the store address.

The ALAT is queried using the physical memory address and the access size, and all overlapping entries are invalidated.

The value of the \(sthint\) completer specifies the locality of the memory access. The values of the \(sthint\) completer are given in Table 2-50 on page 3:220. A prefetch hint is implied in the base update forms. The address specified by the value in GR \(r_3\) after the base update acts as a hint to prefetch the indicated cache line. This prefetch uses the locality hints specified by \(sthint\). See Section 4.4.6, “Memory Hierarchy Control and Consistency” on page 1:60.

Hardware support for \(\text{stfe}\) (10-byte) instructions that reference a page that is neither a cacheable page with write-back policy nor a NaTPage is optional. On processor models that do not support such \(\text{stfe}\) accesses, an Unsupported Data Reference fault is raised when an unsupported reference is attempted.
Operation:

```c
if (PR[qp]) {
    if (imm_base_update_form)
        check_target_register(r3);
    if (tmp_isrcode = fp_reg_disabled(f2, 0, 0, 0))
        disabled_fp_register_fault(tmp_isrcode, WRITE);
    if (GR[r3].nat || (!spill_form && (FR[f2] == NATVAL)))
        register_nat_consumption_fault(WRITE);
    size = spill_form ? 16 : (integer_form ? 8 : fsz);
    itype = WRITE;
    if (size == 10) itype |= UNCACHE_OPT;
    paddr = tlb_translate(GR[r3], size, itype, PSR.cpl, &mattr, &tmp_unused);
    val = fp_fr_to_mem_format(FR[f2], size, integer_form);
    mem_write(val, paddr, size, UM.be, mattr, UNORDERED, sthint);
    alat_inval_multiple_entries(paddr, size);
    if (imm_base_update_form) {
        GR[r3] = GR[r3] + sign_ext(imm, 9);
        GR[r3].nat = 0;
        mem_implicit_prefetch(GR[r3], sthint, WRITE);
    }
}
```

Interruptions:

- Illegal Operation fault
- Disabled Floating-point Register fault
- Register NaT Consumption fault
- Unimplemented Data Address fault
- Data Nested TLB fault
- Alternate Data TLB fault
- VHPT Data fault
- Data TLB fault
- Data Page Not Present fault

Data NaT Page Consumption fault
Data Key Miss fault
Data Key Permission fault
Data Access Rights fault
Data Dirty Bit fault
Data Access Bit fault
Data Debug fault
Unaligned Data Reference fault
Unsupported Data Reference fault
sub — Subtract

Format:  

\((qp)\) sub \(r_1 = r_2, r_3\) 
\((qp)\) sub \(r_1 = r_2, r_3, 1\) 
\((qp)\) sub \(r_1 = imm_8, r_3\)

Description: The second source operand (and an optional constant 1) are subtracted from the first operand and the result placed in GR \(r_1\). In the register form the first operand is GR \(r_2\); in the immediate form the first operand is taken from the sign-extended \(imm_8\) encoding field.

The minus1_form is available only in the register_form (although the equivalent effect can be achieved by adjusting the immediate).

Operation:  

\[
\text{if (PR[qp])} \{
\text{check_target_register}(r_1); 
\text{tmp_src} = (\text{register_form} \ ? \ \text{GR}[r_2] : \text{sign_ext}(\text{imm}_8, 8)); 
\text{tmp_nat} = (\text{register_form} \ ? \ \text{GR}[r_2].nat : 0); 
\text{if (minus1_form)} 
\quad \text{GR}[r_1] = \text{tmp_src} - \text{GR}[r_3] - 1; 
\text{else} 
\quad \text{GR}[r_1] = \text{tmp_src} - \text{GR}[r_3]; 
\quad \text{GR}[r_1].nat = \text{tmp_nat} \ || \ \text{GR}[r_3].nat; 
\}
\]

Interruptions: Illegal Operation fault
sum — Set User Mask

**Format:**

\[(qp) \text{sum} \ imm_{24}\]

**Description:**
The \(imm_{24}\) operand is ORed with the user mask (PSR\{5:0\}) and the result is placed in the user mask. See Section 3.3.2, “Processor Status Register (PSR)” on page 2:18.

PSR.up can only be set if the secure performance monitor bit (PSR.sp) is zero. Otherwise PSR.up is not modified.

**Operation:**

\[
\begin{align*}
\text{if } (\text{PR} [qp]) \{ \\
\quad & \text{if (is_reserved_field(PSR\_TYPE, PSR\_UM, imm_{24}))} \\
\quad & \quad \text{reserved_register_field_fault();} \\
\quad & \text{if (imm_{24}}) \quad PSR(1) = 1; \quad \text{// be} \\
\quad & \text{if (imm_{24}} \&\& \text{PSR.sp == 0}) \quad \text{//non-secure perf monitor} \\
\quad & \quad \text{PSR(2) = 1;} \quad \text{// up} \\
\quad & \text{if (imm_{24}}) \quad PSR(3) = 1; \quad \text{// ac} \\
\quad & \text{if (imm_{24}}) \quad PSR(4) = 1; \quad \text{// mfl} \\
\quad & \text{if (imm_{24}}) \quad PSR(5) = 1; \quad \text{// mfh} \\
\}\n\]

**Interruptions:**
Reserved Register/Field fault

**Serialization:**
All user mask modifications are observed by the next instruction group.
**sxt — Sign Extend**

**Format:** \((qp)\) \textit{sxt} xsz \(r_1 = r_3\)

**Description:** The value in GR \(r_3\) is sign extended from the bit position specified by \(xsz\) and the result is placed in GR \(r_1\). The mnemonic values for \(xsz\) are given in Table 2-51.

**Table 2-51. \(xsz\) Mnemonic Values**

<table>
<thead>
<tr>
<th>(xsz) Mnemonic</th>
<th>Bit Position</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7</td>
</tr>
<tr>
<td>2</td>
<td>15</td>
</tr>
<tr>
<td>4</td>
<td>31</td>
</tr>
</tbody>
</table>

**Operation:**

```c
if (PR[qp]) {
    check_target_register(r1);
    GR[r1] = sign_ext(GR[r3], xsz * 8);
    GR[r1].nat = GR[r3].nat;
}
```

**Interruptions:** Illegal Operation fault
sync — Memory Synchronization

Format:  

(qp) sync.i

Description:  
sync.i ensures that when previously initiated Flush Cache (fc, fc.i) operations issued by the local processor become visible to local data memory references, prior Flush Cache operations are also observed by the local processor instruction fetch stream. sync.i also ensures that at the time previously initiated Flush Cache (fc, fc.i) operations are observed on a remote processor by data memory references they are also observed by instruction memory references on the remote processor. sync.i is ordered with respect to all cache flush operations as observed by another processor. A sync.i and a previous fc must be in separate instruction groups. If semantically required, the programmer must explicitly insert ordered data references (acquire, release or fence type) to appropriately constrain sync.i (and hence fc and fc.i) visibility to the data stream on other processors.

sync.i is used to maintain an ordering relationship between instruction and data caches on local and remote processors. An instruction serialize operation must be used to ensure synchronization initiated by sync.i on the local processor has been observed by a given point in program execution.

An example of self-modifying code (local processor):

```c
st [L1] = data  //store into local instruction stream
fc.i L1          //flush stale datum from instruction/data cache
;;  //require instruction boundary between fc.i and sync.i
sync.i           //ensure local and remote data/inst caches
                    //are synchronized
;;
srcz.i           //ensure sync has been observed by the local processor,
;;  //ensure subsequent instructions observe
//modified memory
L1: target        //instruction modified
```

Operation:  

```c
if (PR[qp]) {
    instruction synchronize();
}
```

Interruptions: None
tak — Translation Access Key

Format: \((qp)\) tak \(r_1 = r_3\)

Description: The protection key for a given virtual address is obtained and placed in GR \(r_1\).

When PSR.dt is 1, the DTLB and the VHPT are searched for the virtual address specified by GR \(r_3\) and the region register indexed by GR \(r_3\) bits \{63:61\}. If a matching present translation is found the protection key of the translation is placed in GR \(r_1\). If a matching present translation is not found or if an unimplemented virtual address is specified by GR \(r_3\), the value 1 is returned.

When PSR.dt is 0, only the DTLB is searched, because the VHPT walker is disabled. If no matching present translation is found in the DTLB, the value 1 is returned.

A translation with the NaTPage attribute is not treated differently and returns its key field.

This instruction can only be executed at the most privileged level.

Operation:

\[
\text{if (PR[qp])} \quad \{
\text{itype} = \text{NON_ACCESS}\mid \text{TAK};
\text{check_target_register}([r_1]);
\text{if (PSR.cpl != 0)}
\quad \text{privileged_operation_fault}(\text{itype});
\text{if (GR[r_3].nat)}
\quad \text{register_nat_consumption_fault}(\text{itype});
\text{GR}[r_1] = \text{tlb_access_key}(\text{GR}[r_3], \text{itype});
\text{GR}[r_1].nat = 0;
\}\]

Interruptions: Illegal Operation fault

Register NaT Consumption fault

Privileged Operation fault
**tbit — Test Bit**

**Format:**
\[(qp) \ tbit.trel.ctype \ p1, p2 = r3, pos6\]

**Description:**
The bit specified by the \[pos6\] immediate is selected from GR \[r3\]. The selected bit forms a single bit result either complemented or not depending on the \[trel\] completer. This result is written to the two predicate register destinations \[p1\] and \[p2\]. The way the result is written to the destinations is determined by the compare type specified by \[ctype\]. See the Compare instruction and Table 2-15 on page 3:34.

The \[trel\] completer values .\[nz\] and .\[z\] indicate non-zero and zero sense of the test. For normal and unc types, only the .\[z\] value is directly implemented in hardware; the .\[nz\] value is actually a pseudo-op. For it, the assembler simply switches the predicate target specifiers and uses the implemented relation. For the parallel types, both relations are implemented in hardware.

**Table 2-52. Test Bit Relations for Normal and unc tbits**

<table>
<thead>
<tr>
<th>[trel]</th>
<th>Test Relation</th>
<th>Pseudo-op of</th>
</tr>
</thead>
<tbody>
<tr>
<td>[nz]</td>
<td>selected bit == 1</td>
<td>[Z] [p1 ↔ p2]</td>
</tr>
<tr>
<td>[z]</td>
<td>selected bit == 0</td>
<td></td>
</tr>
</tbody>
</table>

**Table 2-53. Test Bit Relations for Parallel tbits**

<table>
<thead>
<tr>
<th>[trel]</th>
<th>Test Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>[nz]</td>
<td>selected bit == 1</td>
</tr>
<tr>
<td>[z]</td>
<td>selected bit == 0</td>
</tr>
</tbody>
</table>

If the two predicate register destinations are the same (\[p1\] and \[p2\] specify the same predicate register), the instruction will take an Illegal Operation fault, if the qualifying predicate is set, or if the compare type is unc.
Operation:
if (PR[qp]) {
    if (p1 == p2)
        illegal_operation_fault();

    if (trel == 'nz') // 'nz' - test for 1
        tmp_rel = GR[r3]{pos6};
    else // 'z' - test for 0
        tmp_rel = !GR[r3]{pos6};

    switch (ctype) {
        case 'and': // and-type compare
            if (GR[r3].nat || !tmp_rel) {
                PR[p1] = 0;
                PR[p2] = 0;
            }
            break;
        case 'or': // or-type compare
            if (!GR[r3].nat && tmp_rel) {
                PR[p1] = 1;
                PR[p2] = 1;
            }
            break;
        case 'or.andcm': // or.andcm-type compare
            if (!GR[r3].nat && tmp_rel) {
                PR[p1] = 1;
                PR[p2] = 0;
            }
            break;
        case 'unc': // unc-type compare
            default: // normal compare
                if (GR[r3].nat) {
                    PR[p1] = 0;
                    PR[p2] = 0;
                } else {
                    PR[p1] = tmp_rel;
                    PR[p2] = !tmp_rel;
                }
                break;
        } else {
            if (ctype == 'unc') {
                if (p1 == p2)
                    illegal_operation_fault();
                PR[p1] = 0;
                PR[p2] = 0;
            }
        }
    }
}

Interruptions: Illegal Operation fault
thash — Translation Hashed Entry Address

Format: \( (qp) \text{ thash} \; r_1 = r_3 \)

Description: A Virtual Hashed Page Table (VHPT) entry address is generated based upon the specified virtual address and the result is placed in GR \( r_1 \). The virtual address is specified by GR \( r_3 \) and the region register selected by GR \( r_3 \) bits \( \{63:61\} \).

If \text{thash} is given a NaT input argument or an unimplemented virtual address as an input, the resulting target register value is undefined, and its NaT bit is set to one.

When the processor is configured to use the region-based short format VHPT (PTA.vf=0), the value returned by \text{thash} is defined by the architected short format hash function. See Section 4.1.5.3, “Region-based VHPT Short Format” on page 2:52.

When the processor is configured to use the long format VHPT (PTA.vf=1), \text{thash} performs an implementation-specific long format hash function on the virtual address to generate a hash index into the long format VHPT.

In the long format, a translation in the VHPT must be uniquely identified by its hash index generated by this instruction and the hash tag produced from the ttag instruction.

The hash function must use all implemented region bits and only virtual address bits \( \{60:0\} \) to determine the offset into the VHPT. Virtual address bits \( \{63:61\} \) are used only by the short format hash to determine the region of the VHPT.

This instruction must be implemented on all processor models, even processor models that do not implement a VHPT walker.

Operation: if (PR[qp]) {
check_target_register(r_1);
if (GR[r_3].nat || unimplemented_virtual_address(GR[r_3])) {
   GR[r_1] = undefined();
   GR[r_1].nat = 1;
} else {
   tmp_vr = GR[r_3]{63:61};
   tmp_va = GR[r_3]{60:0};
   GR[r_1] = tlb_vhpt_hash(tmp_vr, tmp_va, RR[tmp_vr].rid, RR[tmp_vr].ps);
   GR[r_1].nat = 0;
}
}

Interruptions: Illegal Operation fault
tnat — Test NaT

Format: \( (qp) \text{tnat} . \text{trel} . \text{ctype} \ p_1, p_2 = r_3 \)

Description: The NaT bit from GR \( r_3 \) forms a single bit result, either complemented or not depending on the \( \text{trel} \) completer. This result is written to the two predicate register destinations, \( p_1 \) and \( p_2 \). The way the result is written to the destinations is determined by the compare type specified by \( \text{ctype} \). See the Compare instruction and Table 2-15 on page 3:34.

The \( \text{trel} \) completer values .nz and .z indicate non-zero and zero sense of the test. For normal and unc types, only the .z value is directly implemented in hardware; the .nz value is actually a pseudo-op. For it, the assembler simply switches the predicate target specifiers and uses the implemented relation. For the parallel types, both relations are implemented in hardware.

Table 2-54. Test NaT Relations for Normal and unc tnats

<table>
<thead>
<tr>
<th>trel</th>
<th>Test Relation</th>
<th>Pseudo-op of</th>
</tr>
</thead>
<tbody>
<tr>
<td>nz</td>
<td>selected bit == 1</td>
<td>z ( p_1 \leftrightarrow p_2 )</td>
</tr>
<tr>
<td>z</td>
<td>selected bit == 0</td>
<td></td>
</tr>
</tbody>
</table>

Table 2-55. Test NaT Relations for Parallel tnats

<table>
<thead>
<tr>
<th>trel</th>
<th>Test Relation</th>
</tr>
</thead>
<tbody>
<tr>
<td>nz</td>
<td>selected bit == 1</td>
</tr>
<tr>
<td>z</td>
<td>selected bit == 0</td>
</tr>
</tbody>
</table>

If the two predicate register destinations are the same (\( p_1 \) and \( p_2 \) specify the same predicate register), the instruction will take an Illegal Operation fault, if the qualifying predicate is set, or if the compare type is unc.
Operation:

if (PR[q]) {
    if (p1 == p2)
        illegal_operationFault();

    if (trel == 'nz') // 'nz' - test for 1
        trel = GR[r3].nat;
    else // 'z' - test for 0
        trel = !GR[r3].nat;

    switch (ctype) {
        case 'and': // and-type compare
            if (!tmp_rel) {
                PR[p1] = 0;
                PR[p2] = 0;
            }
            break;
        case 'or': // or-type compare
            if (tmp_rel) {
                PR[p1] = 1;
                PR[p2] = 1;
            }
            break;
        case 'or.andcm': // or.andcm-type compare
            if (tmp_rel) {
                PR[p1] = 1;
                PR[p2] = 0;
            }
            break;
        case 'unc': // unc-type compare
            default: // normal compare
                PR[p1] = tmp_rel;
                PR[p2] = !tmp_rel;
                break;
        }
    }
}
else {
    if (ctype == 'unc') {
        if (p1 == p2)
            illegalOperationFault();
        PR[p1] = 0;
        PR[p2] = 0;
    }
}

Interruptions: Illegal Operation fault
tpa — Translate to Physical Address

Format: \( (qp) \ tpa \ r_1 = r_3 \)

Description: The physical address for the virtual address specified by GR \( r_3 \) is obtained and placed in GR \( r_1 \).

When PSR.dt is 1, the DTLB and the VHPT are searched for the virtual address specified by GR \( r_3 \) and the region register indexed by GR \( r_3 \) bits \{63:61\}. If a matching present translation is found the physical address of the translation is placed in GR \( r_1 \). If a matching present translation is not found the appropriate TLB fault is taken.

When PSR.dt is 0, only the DTLB is searched, because the VHPT walker is disabled. If no matching present translation is found in the DTLB, an Alternate Data TLB fault is raised if psr.ic is one or a Data Nested TLB fault is raised if psr.ic is zero.

If this instruction faults, then it will set the non-access bit in the ISR. The ISR read and write bits are not set.

This instruction can only be executed at the most privileged level.

Operation:

\[
\text{if (PR[qp])} \quad \{
\quad \text{itype} = \text{NON\_ACCESS}|\text{TPA};
\quad \text{check\_target\_register}(r_1);
\quad \text{if (PSR.cpl != 0)}
\quad \quad \text{privileged\_operation\_fault}(\text{itype});
\quad \text{if (GR[r_3].nat)}
\quad \quad \text{register\_nat\_consumption\_fault}(\text{itype});
\quad \quad \text{GR}[r_1] = \text{tlb\_translate\_nonaccess}(\text{GR}[r_3], \text{itype});
\quad \quad \text{GR}[r_1].nat = 0;
\quad \}
\]

Interruptions:

<table>
<thead>
<tr>
<th>Illegal Operation fault</th>
<th>Alternate Data TLB fault</th>
</tr>
</thead>
<tbody>
<tr>
<td>Privileged Operation fault</td>
<td>VHPT Data fault</td>
</tr>
<tr>
<td>Register NaT Consumption fault</td>
<td>Data TLB fault</td>
</tr>
<tr>
<td>Unimplemented Data Address fault</td>
<td>Data Page Not Present fault</td>
</tr>
<tr>
<td>Data Nested TLB fault</td>
<td>Data NaT Page Consumption fault</td>
</tr>
</tbody>
</table>
**ttag — Translation Hashed Entry Tag**

**Format:**

\[(qp) \quad ttag \quad r_1 = r_3\]

**Description:**

A tag used for matching during searches of the long format Virtual Hashed Page Table (VHPT) is generated and placed in GR \(r_1\). The virtual address is specified by GR \(r_3\) and the region register selected by GR \(r_3\) bits \(\{63:61\}\).

If \(ttag\) is given a NaT input argument or an unimplemented virtual address as an input, the resulting target register value is undefined, and its NaT bit is set to one.

The tag generation function generates an implementation-specific long format VHPT tag. The tag generation function must use all implemented region bits and only virtual address bits \(\{60:0\}\). PTA.vf is ignored by this instruction.

A translation in the long format VHPT must be uniquely identified by its hash index generated by the \(thash\) instruction and the tag produced from this instruction.

This instruction must be implemented on all processor models, even processor models that do not implement a VHPT walker.

**Operation:**

\[
\begin{align*}
\text{if } (PR[qp]) \{
\text{check_target_register}(r_1); \\
\text{if } (GR[r_3].nat \text{ or } \text{unimplemented_virtual_address}(GR[r_3])) \{
GR[r_1] = \text{undefined}(); \quad \text{GR}[r_1].nat = 1; \\
\} \text{ else } \\
\text{tmp_vr} = GR[r_3]\{63:61\}; \\
\text{tmp_va} = GR[r_3]\{60:0\}; \\
GR[r_1] = \text{tlb_vhpt_tag}(\text{tmp_va}, RR[\text{tmp_vr}].rid, RR[\text{tmp_vr}].ps); \\
\text{GR}[r_1].nat = 0; \\
\} \\
\}
\]

**Interruptions:** Illegal Operation fault
unpack — Unpack

Format:

- `(qp) unpack1.h r_j = r_2, r_3`  
  one_byte_form, high_form
- `(qp) unpack2.h r_j = r_2, r_3`  
  two_byte_form, high_form
- `(qp) unpack4.h r_j = r_2, r_3`  
  four_byte_form, high_form
- `(qp) unpack1.l r_j = r_2, r_3`  
  one_byte_form, low_form
- `(qp) unpack2.l r_j = r_2, r_3`  
  two_byte_form, low_form
- `(qp) unpack4.l r_j = r_2, r_3`  
  four_byte_form, low_form

Description: The data elements of GR \( r_2 \) and \( r_3 \) are unpacked, and the result placed in GR \( r_j \). In the high_form, the most significant elements of each source register are selected, while in the low_form the least significant elements of each source register are selected. Elements are selected alternately from the source registers.

Operation:  
```c
if (PR[qp]) {
    check_target_register(r_j);
    if (one_byte_form) { // one-byte elements
        x[0] = GR[r_2]{7:0}; y[0] = GR[r_3]{7:0};
        if (high_form)
            GR[r_j] = concatenate8( x[7], y[7], x[6], y[6],
                                  x[5], y[5], x[4], y[4]);
        else // low_form
            GR[r_j] = concatenate8( x[3], y[3], x[2], y[2],
                                  x[1], y[1], x[0], y[0]);
    } else if (two_byte_form) { // two-byte elements
        x[0] = GR[r_2]{15:0}; y[0] = GR[r_3]{15:0};
        if (high_form)
            GR[r_j] = concatenate4(x[3], y[3], x[2], y[2]);
        else // low_form
            GR[r_j] = concatenate4(x[1], y[1], x[0], y[0]);
    } else { // four-byte elements
        x[0] = GR[r_2]{31:0}; y[0] = GR[r_3]{31:0};
        if (high_form)
            GR[r_j] = concatenate2(x[1], y[1]);
        else // low_form
            GR[r_j] = concatenate2(x[0], y[0]);
}
GR[r_j].nat = GR[r_2].nat | | GR[r_3].nat;
```
Figure 2-45. Unpack Operation

unpack1.h

GR r2:

GR r3:

GR r1:

unpack1.1

GR r2:

GR r3:

GR r1:

unpack2.h

GR r2:

GR r3:

GR r1:

unpack2.1

GR r2:

GR r3:

GR r1:

unpack4.h

GR r2:

GR r3:

GR r1:

unpack4.1

GR r2:

GR r3:

GR r1:
xchg — Exchange

**Format:**

\[(qp)\ xchg\ ldhint\ r_1 = [r_2], r_3\]

**Description:**

A value consisting of \(sz\) bytes is read from memory starting at the address specified by the value in GR \(r_3\). The least significant \(sz\) bytes of the value in GR \(r_2\) are written to memory starting at the address specified by the value in GR \(r_3\). The value read from memory is then zero extended and placed in GR \(r_1\) and the NaT bit corresponding to GR \(r_1\) is cleared. The values of the \(sz\) completer are given in Table 2-56.

If the address specified by the value in GR \(r_3\) is not naturally aligned to the size of the value being accessed in memory, an Unaligned Data Reference fault is taken independent of the state of the User Mask alignment checking bit, UM.ac (PSR.ac in the Processor Status Register).

Both read and write access privileges for the referenced page are required.

### Table 2-56. Memory Exchange Size

<table>
<thead>
<tr>
<th>sz Completer</th>
<th>Bytes Accessed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1 byte</td>
</tr>
<tr>
<td>2</td>
<td>2 bytes</td>
</tr>
<tr>
<td>4</td>
<td>4 bytes</td>
</tr>
<tr>
<td>8</td>
<td>8 bytes</td>
</tr>
</tbody>
</table>

The exchange is performed with acquire semantics, i.e., the memory read/write is made visible prior to all subsequent data memory accesses. See Section 4.4.7, “Sequentiality Attribute and Ordering” on page 2:69 for details on memory ordering.

The memory read and write are guaranteed to be atomic.

This instruction is only supported to cacheable pages with write-back write policy. Accesses to NaTPages cause a Data NaT Page Consumption fault. Accesses to pages with other memory attributes cause an Unsupported Data Reference fault.

The value of the \(ldhint\) completer specifies the locality of the memory access. The values of the \(ldhint\) completer are given in Table 2-34 on page 3:132. Locality hints do not affect program functionality and may be ignored by the implementation. See Section 4.4.6, “Memory Hierarchy Control and Consistency” on page 1:60 for details.

**Operation:**

```c
if (PR[qp]) {
    check_target_register(r_1);
    check_target_register(r_2);
    if (GR[r_3].nat || GR[r_2].nat)
        register_nat_consumption_fault(SEMAPHORE);
    paddr = tlb_translate(GR[r_3], sz, SEMAPHORE, PSR.cpl, &mattr, &tmp_unused);
    if (!ma_supports_semaphores(mattr))
        unsupported_data_reference_fault(SEMAPHORE, GR[r_3]);
    val = mem_xchg(GR[r_2], paddr, sz, UM.be, mattr, ACQUIRE, ldhint);
    alat_inval_multiple_entries(paddr, sz);
    GR[r_1] = zero_ext(val, sz * 8);
    GR[r_1].nat = 0;
}
```
**Interruptions:**

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Illegal Operation fault</td>
<td>Data Key Miss fault</td>
</tr>
<tr>
<td>Register NaT Consumption fault</td>
<td>Data Key Permission fault</td>
</tr>
<tr>
<td>Unimplemented Data Address fault</td>
<td>Data Access Rights fault</td>
</tr>
<tr>
<td>Data Nested TLB fault</td>
<td>Data Dirty Bit fault</td>
</tr>
<tr>
<td>Alternate Data TLB fault</td>
<td>Data Access Bit fault</td>
</tr>
<tr>
<td>VHPT Data fault</td>
<td>Data Debug fault</td>
</tr>
<tr>
<td>Data TLB fault</td>
<td>Unaligned Data Reference fault</td>
</tr>
<tr>
<td>Data Page Not Present fault</td>
<td>Unsupported Data Reference fault</td>
</tr>
<tr>
<td>Data NaT Page Consumption fault</td>
<td></td>
</tr>
</tbody>
</table>
xma — Fixed-Point Multiply Add

Format:

- \((qp)\) xma.l \(f_1 = f_3, f_4, f_2\)
- \((qp)\) xma.lu \(f_1 = f_3, f_4, f_2\)
- \((qp)\) xma.h \(f_1 = f_3, f_4, f_2\)
- \((qp)\) xma.hu \(f_1 = f_3, f_4, f_2\)

Description:

Two source operands (FR \(f_3 \) and FR \(f_4 \) ) are treated as either signed or unsigned integers and multiplied. The third source operand (FR \(f_2 \) ) is zero extended and added to the product. The upper or lower 64 bits of the resultant sum are selected and placed in FR \(f_1 \).

In the high_unsigned_form, the significand fields of FR \(f_3 \) and FR \(f_4 \) are treated as unsigned integers and multiplied to produce a full 128-bit unsigned result. The significand field of FR \(f_2 \) is zero extended and added to the product. The most significant 64-bits of the resultant sum are placed in the significand field of FR \(f_1 \).

In the high_form, the significand fields of FR \(f_3 \) and FR \(f_4 \) are treated as signed integers and multiplied to produce a full 128-bit signed result. The significand field of FR \(f_2 \) is zero extended and added to the product. The most significant 64-bits of the resultant sum are placed in the significand field of FR \(f_1 \).

In the other forms, the significand fields of FR \(f_3 \) and FR \(f_4 \) are treated as signed integers and multiplied to produce a full 128-bit signed result. The significand field of FR \(f_2 \) is zero extended and added to the product. The least significant 64-bits of the resultant sum are placed in the significand field of FR \(f_1 \).

In all forms, the exponent field of FR \(f_1 \) is set to the biased exponent for 2.063 (0x1003E) and the sign field of FR \(f_1 \) is set to positive (0).

Note:  
\(f_1 \) as an operand is not an integer 1; it is just the register file format’s 1.0 value.

In all forms, if any of FR \(f_3 \), FR \(f_4 \), or FR \(f_2 \) is a NaTVal, FR \(f_1 \) is set to NaTVal instead of the computed result.

Operation:

```c
if (PR[qp]) {
    fp_check_target_register(f_1);
    if (tmp_isrcode = fp_reg_disabled(f_1, f_2, f_3, f_4))
        disabled_fp_register_fault(tmp_isrcode, 0);
    if (fp_is_natval(FR[f_2]) || fp_is_natval(FR[f_3]) ||
        fp_is_natval(FR[f_4])) {
        FR[f_1] = NATVAL;
    } else {
        if (low_form || high_form)
            tmp_res_128 = fp_I64_x_I64_to_I128(FR[f_3].significand, FR[f_4].significand);
        else // high_unsigned_form
            tmp_res_128 = fp_U64_x_U64_to_U128(FR[f_3].significand, FR[f_4].significand);
        tmp_res_128 = fp_U128_add(tmp_res_128, fp_U64_to_U128(FR[f_2].significand));
        if (high_form || high_unsigned_form)
            FR[f_1].significand = tmp_res_128.hi;
        else // low_form
            FR[f_1].significand = tmp_res_128.lo;
        FR[f_1].exponent = FP_INTEGER_EXP;
    }
```
FR[f_i].sign = FP_SIGN_POSITIVE;
}
fp_update_psr(f_i);

**Interruptions:**  Disabled Floating-point Register fault
xmpy — Fixed-Point Multiply

**Format:**

(qp) xmpy.l \(f_1 = f_3, f_4\)

(qp) xmpy.lu \(f_1 = f_3, f_4\)

(qp) xmpy.h \(f_1 = f_3, f_4\)

(qp) xmpy.hu \(f_1 = f_3, f_4\)

 pseudo-op of: (qp) xma.l \(f_1 = f_3, f_4\), \(f_0\)

 pseudo-op of: (qp) xma.l \(f_1 = f_3, f_4\), \(f_0\)

 pseudo-op of: (qp) xma.h \(f_1 = f_3, f_4\), \(f_0\)

 pseudo-op of: (qp) xma.hu \(f_1 = f_3, f_4\), \(f_0\)

**Description:**

Two source operands (FR \(f_3\) and FR \(f_4\)) are treated as either signed or unsigned integers and multiplied. The upper or lower 64 bits of the resultant product are selected and placed in FR \(f_1\).

In the high unsigned form, the significand fields of FR \(f_3\) and FR \(f_4\) are treated as unsigned integers and multiplied to produce a full 128-bit unsigned result. The most significant 64-bits of the resultant product are placed in the significand field of FR \(f_1\).

In the high form, the significand fields of FR \(f_3\) and FR \(f_4\) are treated as signed integers and multiplied to produce a full 128-bit signed result. The most significant 64-bits of the resultant product are placed in the significand field of FR \(f_1\).

In the other forms, the significand fields of FR \(f_3\) and FR \(f_4\) are treated as signed integers and multiplied to produce a full 128-bit signed result. The least significant 64-bits of the resultant product are placed in the significand field of FR \(f_1\).

In all forms, the exponent field of FR \(f_1\) is set to the biased exponent for \(2.0^{63}\) (0x1003E) and the sign field of FR \(f_1\) is set to positive (0). Note: \(f_1\) as an operand is not an integer 1; it is just the register file format’s 1.0 value.

**Operation:**

See “xma — Fixed-Point Multiply Add” on page 3:239.
xor — Exclusive Or

Format: 

\[(qp) \text{ xor } r_1 = r_2, r_3\] \hspace{1cm} \text{register_form} \hspace{1cm} A1

\[(qp) \text{ xor } r_1 = \text{imm}_8, r_3\] \hspace{1cm} \text{imm8_form} \hspace{1cm} A3

Description: The two source operands are logically XORed and the result placed in GR \(r_1\). In the register_form the first operand is GR \(r_2\); in the imm8_form the first operand is taken from the \(\text{imm}_8\) encoding field.

Operation: 

\[
\text{if } (PR[qp]) \{ \\
\text{check_target_register}(r_1); \\
\text{tmp}_\text{src} = (\text{register_form} ? \text{GR}[r_2] : \text{sign_ext}(\text{imm}_8, 8)); \\
\text{tmp}_\text{nat} = (\text{register_form} ? \text{GR}[r_2].\text{nat} : 0); \\
\text{GR}[r_1] = \text{tmp}_\text{src} \text{ ^ } \text{GR}[r_3]; \\
\text{GR}[r_1].\text{nat} = \text{tmp}_\text{nat} \text{ || } \text{GR}[r_3].\text{nat}; \\
\}
\]

Interruptions: Illegal Operation fault
zxt — Zero Extend

Format: \((qp)\) zxtsz z r1 = r3

Description: The value in GR \(r_3\) is zero extended above the bit position specified by sz and the result is placed in GR \(r_1\). The mnemonic values for sz are given in Table 2-51 on page 3:225.

Operation:

\[
\text{if (PR[qp])} \{
\text{check_target_register}(r_1); \\
\text{GR}[r_1] = \text{zero_ext}(\text{GR}[r_3], sz \times 8); \\
\text{GR}[r_1].nat = \text{GR}[r_3].nat;
\}
\]

Interruptions: Illegal Operation fault
This chapter contains a table of all pseudo-code functions used on the Itanium instruction pages.

### Table 3-1. Pseudo-Code Functions

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>xxx_fault(parameters ...)</td>
<td>There are several fault functions. Each fault function accepts parameters specific to the fault, e.g., exception code values, virtual addresses, etc. If the fault is deferred for speculative load exceptions the fault function will return with a deferral indication. Otherwise, fault routines do not return and terminate the instruction sequence.</td>
</tr>
<tr>
<td>xxx_trap(parameters ...)</td>
<td>There are several trap functions. Each trap function accepts parameters specific to the trap, e.g., trap code values, virtual addresses, etc. Trap routines do not return.</td>
</tr>
<tr>
<td>acceptance_fence()</td>
<td>Ensures prior data memory references to uncached ordered-sequential memory pages are “accepted”, before subsequent data memory references are performed by the processor.</td>
</tr>
<tr>
<td>alat_cmp(rtype, raddr)</td>
<td>Returns a one if the implementation finds an ALAT entry which matches the register type specified by rtype and the register address specified by raddr, else returns zero. This function is implementation-specific. Note that an implementation may optionally choose to return zero (indicating no match) even if a matching entry exists in the ALAT. This provides implementation flexibility in designing fast ALAT lookup circuits.</td>
</tr>
<tr>
<td>alat_frame_update(delta_bof, delta_sof)</td>
<td>Notifies the ALAT of a change in the bottom of frame and/or size of frame. This allows management of the ALAT’s tag bits or other management functions it might need.</td>
</tr>
<tr>
<td>alat_inval()</td>
<td>Invalidate all entries in the ALAT.</td>
</tr>
<tr>
<td>alat_inval_multiple_entries(paddr, size)</td>
<td>The ALAT is queried using the physical memory address specified by paddr and the access size specified by size. All matching ALAT entries are invalidated. No value is returned.</td>
</tr>
<tr>
<td>alat_inval_single_entry(rtype, rega)</td>
<td>The ALAT is queried using the register type specified by rtype and the register address specified by rega. At most one matching ALAT entry is invalidated. No value is returned.</td>
</tr>
<tr>
<td>alat_write(rtype, raddr, paddr, size)</td>
<td>Allocates a new ALAT entry using the register type specified by rtype, the register address specified by raddr, the physical memory address specified by paddr, and the access size specified by size. No value is returned. This function guarantees that only one ALAT entry exists for a given raddr. If a ld.c.nc, ldf.c.nc, or ldfp.c.nc instruction’s raddr matches an existing ALAT entry’s register tag, but the instruction’s size and/or paddr are different than that of the existing entry’s; then this function may either preserve the existing entry, or invalidate it and write a new entry with the instruction’s specified size and paddr.</td>
</tr>
<tr>
<td>align_to_size_boundary(vaddr, size)</td>
<td>Returns vaddr aligned to the boundary specified by size.</td>
</tr>
<tr>
<td>branch_predict(wh, ih, ret, target, tag)</td>
<td>Implementation-dependent routine which updates the processor’s branch prediction structures.</td>
</tr>
<tr>
<td>check_branch_implemented(check_type)</td>
<td>Implementation-dependent routine which returns TRUE or FALSE, depending on whether a failing check instruction causes a branch (TRUE), or a Speculative Operation fault (FALSE). The result may be different for different types of check instructions: CHKS_GENERAL, CHKS_FLOAT, CHKA_GENERAL, CHKA_FLOAT. In addition, the result may depend on other implementation-dependent parameters.</td>
</tr>
<tr>
<td>check_target_register(r1)</td>
<td>If r1 targets an out-of-frame stacked register (as defined by CFM), an illegal operation fault is delivered, and this function does not return.</td>
</tr>
<tr>
<td>check_target_register_sof(r1, newsof)</td>
<td>If r1 targets an out-of-frame stacked register (as defined by the newsof parameter), an illegal operation fault is delivered, and this function does not return.</td>
</tr>
<tr>
<td>concatenate2(x1, x2)</td>
<td>Concatenates the lower 32 bits of the 2 arguments, and returns the 64-bit result.</td>
</tr>
</tbody>
</table>
Table 3-1. Pseudo-Code Functions (Continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>concatenate4(x1, x2, x3, x4)</td>
<td>Concatenates the lower 16 bits of the 4 arguments, and returns the 64-bit result.</td>
</tr>
<tr>
<td>concatenate8(x1, x2, x3, x4, x5, x6, x7, x8)</td>
<td>Concatenates the lower 8 bits of the 8 arguments, and returns the 64-bit result.</td>
</tr>
<tr>
<td>data_serialize()</td>
<td>Ensures all prior register updates with side-effects are observed before subsequent execution and data memory references are performed.</td>
</tr>
<tr>
<td>deliver_unmasked_pending_interrupt()</td>
<td>This implementation-specific function checks whether any unmasked external interrupts are pending, and if so, transfers control to the external interrupt vector.</td>
</tr>
<tr>
<td>execute_hint(hint)</td>
<td>Executes the hint specified by \texttt{hint}.</td>
</tr>
<tr>
<td>fadd(fp_dp, fr2)</td>
<td>Adds a floating-point register value to the infinitely precise product and return the infinitely precise sum, ready for rounding.</td>
</tr>
<tr>
<td>fcmp_exception_fault_check(f2, f3, frel, sf, *tmp_fp_env)</td>
<td>Checks for all floating-point faulting conditions for the \texttt{fcmp} instruction.</td>
</tr>
<tr>
<td>fctv.fx_exception_fault_check(fr2, signed_form, trunc_form, sf, *tmp_fp_env)</td>
<td>Checks for all floating-point faulting conditions for the \texttt{fcvt.fx}, \texttt{fcvt.fxu}, \texttt{fcvt.fx.trunc} and \texttt{fcvt.fxu.trunc} instructions. It propagates NaNs.</td>
</tr>
<tr>
<td>fma_exception_check(f2, f3, f4, pc, sf, *tmp_fp_env)</td>
<td>Checks for all floating-point faulting conditions for the \texttt{fma} instruction. It propagates NaNs and special IEEE results.</td>
</tr>
<tr>
<td>fminmax_exception_check(f2, f3, f4, pc, sf, *tmp_fp_env)</td>
<td>Checks for all floating-point faulting conditions for the \texttt{famin}, \texttt{famax}, \texttt{fmax}, and \texttt{fmin} instructions.</td>
</tr>
<tr>
<td>fms_fma_exception_check(f2, f3, f4, pc, sf, *tmp_fp_env)</td>
<td>Checks for all floating-point faulting conditions for the \texttt{fms} and \texttt{fma} instructions. It propagates NaNs and special IEEE results.</td>
</tr>
<tr>
<td>fmul(fr3, fr4)</td>
<td>Performs an infinitely precise multiply of two floating-point register values.</td>
</tr>
<tr>
<td>followed_by_stop()</td>
<td>Returns \texttt{TRUE} if the current instruction is followed by a \texttt{stop}; otherwise, returns \texttt{FALSE}.</td>
</tr>
<tr>
<td>fp_check_target_register(f1)</td>
<td>If the specified floating-point register identifier is 0 or 1, this function causes an illegal operation fault.</td>
</tr>
<tr>
<td>fp_decode_fault(tmp_fp_env)</td>
<td>Returns floating-point exception fault code values for ISR.code.</td>
</tr>
<tr>
<td>fp_decode_traps(tmp_fp_env)</td>
<td>Returns floating-point trap code values for ISR.code.</td>
</tr>
<tr>
<td>fp_is_nan_or_inf(freg)</td>
<td>Returns true if the floating-point exception_check functions returned an IEEE fault disabled default result or a propagated NaN.</td>
</tr>
<tr>
<td>fp_equal(fr1, fr2)</td>
<td>IEEE standard equality relationship test.</td>
</tr>
<tr>
<td>fp_ieee_recip(num, den)</td>
<td>Returns the true quotient for special sets of operands, or an approximation to the reciprocal of the divisor to be used in the software divide algorithm.</td>
</tr>
<tr>
<td>fp_ieee_recip_sqrt(root)</td>
<td>Returns the true square root result for special operands, or an approximation to the reciprocal square root to be used in the software square root algorithm.</td>
</tr>
<tr>
<td>fp_is_nan(freg)</td>
<td>Returns true when floating register contains a NaN.</td>
</tr>
<tr>
<td>fp_is_natval(freg)</td>
<td>Returns true when floating register contains a NaTVal.</td>
</tr>
<tr>
<td>fp_is_normal(freg)</td>
<td>Returns true when floating register contains a normal number.</td>
</tr>
<tr>
<td>fp_is_pos_inf(freg)</td>
<td>Returns true when floating register contains a positive infinity.</td>
</tr>
<tr>
<td>fp_is_qnan(freg)</td>
<td>Returns true when floating register contains a quiet NaN.</td>
</tr>
<tr>
<td>fp_is_snan(freg)</td>
<td>Returns true when floating register contains a signalling NaN.</td>
</tr>
<tr>
<td>fp_is_unorm(freg)</td>
<td>Returns true when floating register contains an unnormalized number.</td>
</tr>
<tr>
<td>fp_is_unsupported(freg)</td>
<td>Returns true when floating register contains an unsupported format.</td>
</tr>
<tr>
<td>fp_less_than(fr1, fr2)</td>
<td>IEEE standard less-than relationship test.</td>
</tr>
<tr>
<td>fp_lesser_or_equal(fr1, fr2)</td>
<td>IEEE standard less-than or equal-to relationship test.</td>
</tr>
<tr>
<td>fp_normalize(fr1)</td>
<td>Normalizes an unnormalized fp value. This function flushes to zero any unnormal values which can not be represented in the register file.</td>
</tr>
<tr>
<td>fp_raise_fault(tmp_fp_env)</td>
<td>Checks the local instruction state for any faulting conditions which require an interruption to be raised.</td>
</tr>
</tbody>
</table>
Table 3-1. Pseudo-Code Functions (Continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>fp_raise_traps(tmp_fp_env)</code></td>
<td>Checks the local instruction state for any trapping conditions which require an interruption to be raised.</td>
</tr>
<tr>
<td><code>fp_reg_bank_conflict(f1, f2)</code></td>
<td>Returns true if the two specified FRs are in the same bank.</td>
</tr>
<tr>
<td><code>fp_reg_disabled(f1, f2, f3, f4)</code></td>
<td>Check for possible disabled floating-point register faults.</td>
</tr>
<tr>
<td><code>fp_reg_read(freg)</code></td>
<td>Reads the FR and gives canonical double-extended denormals (and pseudo-denormals) their true mathematical exponent. Other classes of operands are unaltered.</td>
</tr>
<tr>
<td><code>fp_unordered(fr1, fr2)</code></td>
<td>IEEE standard unordered relationship</td>
</tr>
<tr>
<td><code>fp_fr_to_mem_format(freg, size)</code></td>
<td>Converts a floating-point value in register format to floating-point memory format. It assumes that the floating-point value in the register has been previously rounded to the correct precision which corresponds with the size parameter.</td>
</tr>
<tr>
<td><code>fpcmp_exception_fault_check(f2, f3, rel, sf, *tmp_fp_env)</code></td>
<td>Checks for all floating-point faulting conditions for the <code>fpcmp</code> instruction.</td>
</tr>
<tr>
<td><code>fpcvt_exception_fault_check(f2, signed_form, trunc_form, sf, *tmp_fp_env)</code></td>
<td>Checks for all floating-point faulting conditions for the <code>fpcvt.fx, fpcvt.fxu, fpcvt.fx.trunc, and fpcvt.fxu.trunc</code> instructions. It propagates NaNs.</td>
</tr>
<tr>
<td><code>fpma_exception_fault_check(f2, f3, f4, sf, *tmp_fp_env)</code></td>
<td>Checks for all floating-point faulting conditions for the <code>fpma</code> instruction. It propagates NaNs and special IEEE results.</td>
</tr>
<tr>
<td><code>fpminmax_exception_fault_check(f2, f3, sf, *tmp_fp_env)</code></td>
<td>Checks for all floating-point faulting conditions for the <code>fpmin, fpmax, fpamin and fpamax</code> instructions.</td>
</tr>
<tr>
<td><code>fpms_fpma_exception_fault_check(f2, f3, f4, sf, *tmp_fp_env)</code></td>
<td>Checks for all floating-point faulting conditions for the <code>fpms</code> and <code>fpma</code> instructions. It propagates NaNs and special IEEE results.</td>
</tr>
<tr>
<td><code>fprcpa_exception_fault_check(f2, f3, sf, *tmp_fp_env, *limits_check)</code></td>
<td>Checks for all floating-point faulting conditions for the <code>fprcpa</code> instruction. It propagates NaNs and special IEEE results. It also indicates operand limit violations.</td>
</tr>
<tr>
<td><code>frsqrta_exception_fault_check(f3, sf, *tmp_fp_env)</code></td>
<td>Checks for all floating-point faulting conditions for the <code>frsqrta</code> instruction. It propagates NaNs and special IEEE results.</td>
</tr>
<tr>
<td><code>is_finite(freg)</code></td>
<td>Returns true when floating register contains a finite number.</td>
</tr>
<tr>
<td><code>is_ignored_reg(regnum)</code></td>
<td>Boolean function that returns true if <code>regnum</code> is an ignored application register, otherwise false.</td>
</tr>
<tr>
<td><code>is_infty(freg)</code></td>
<td>Returns true when floating register contains an infinite number.</td>
</tr>
<tr>
<td><code>is_interruption_cr(regnum)</code></td>
<td>Boolean function that returns true if <code>regnum</code> is one of the Interruption Control registers (see Section 3.3.5, &quot;Interruption Control Registers&quot; on page 2:29), otherwise false.</td>
</tr>
</tbody>
</table>
| `is_kernel_reg(ar_addr)` | Returns a one if `ar_addr` is the address of a kernel register application register.
## Table 3-1. Pseudo-Code Functions (Continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>is_read_only_reg(rtype, raddr)</code></td>
<td>Returns a one if the register addressed by <code>raddr</code> in the register bank of type <code>rtype</code> is a read only register.</td>
</tr>
<tr>
<td><code>is_reserved_field(regclass, arg2, arg3)</code></td>
<td>Returns true if the specified data would write a one in a reserved field.</td>
</tr>
<tr>
<td><code>is_reserved_reg(regclass, regnum)</code></td>
<td>Returns true if register <code>regnum</code> is reserved in the <code>regclass</code> register file.</td>
</tr>
<tr>
<td><code>is_supported_hint(hint)</code></td>
<td>Returns true if the implementation supports the specified <code>hint</code>. This function may depend on factors other than the <code>hint</code> value, such as which execution unit it is executed on or the slot number the instruction was encoded in.</td>
</tr>
<tr>
<td><code>long_branch_implemented()</code></td>
<td>Implementation-dependent routine which returns TRUE or FALSE, depending on whether long branches are implemented.</td>
</tr>
<tr>
<td><code>make_icache_coherent(paddr)</code></td>
<td>The cache line addressed by the physical address <code>paddr</code> is flushed in an implementation-specific manner that ensures that the instruction cache is coherent with the data caches.</td>
</tr>
<tr>
<td><code>mem_flush(paddr)</code></td>
<td>The line addressed by the physical address <code>paddr</code> is invalidated in all levels of the memory hierarchy above memory and written back to memory if it is inconsistent with memory.</td>
</tr>
<tr>
<td><code>mem_flush_pending_stores()</code></td>
<td>The processor is instructed to start draining pending stores in write coalescing and write buffers. This operation is a “hint”. There is no indication when prior stores have actually been drained.</td>
</tr>
<tr>
<td><code>mem_implicit_prefetch(vaddr, hint, type)</code></td>
<td>Moves the line addressed by <code>vaddr</code> to the location of the memory hierarchy specified by <code>hint</code>. This function is implementation dependent and can be ignored. The <code>type</code> allows the implementation to distinguish prefetches for different instruction types.</td>
</tr>
<tr>
<td><code>mem_promote(paddr, mtype, hint)</code></td>
<td>Moves the line addressed by <code>paddr</code> to the highest level of the memory hierarchy conditioned by the access hints specified by <code>hint</code>. Implementation dependent and can be ignored.</td>
</tr>
<tr>
<td><code>mem_read(paddr, size, border, mattr, otype, hint)</code></td>
<td>Returns the <code>size</code> bytes starting at the physical memory location specified by <code>paddr</code> with byte order specified by <code>border</code>, memory attributes specified by <code>mattr</code>, and access hint specified by <code>hint</code>. <code>otype</code> specifies the memory ordering attribute of this access, and must be UNORDERED or ACQUIRE.</td>
</tr>
<tr>
<td><code>mem_read_pair(*low_value, *high_value, paddr, size, border, mattr, otype, hint)</code></td>
<td>Reads the <code>size</code>/2 bytes of memory starting at the physical memory address specified by <code>paddr</code> into <code>low_value</code>, and the <code>size</code>/2 bytes of memory starting at the physical memory address specified by <code>(paddr + size/2)</code> into <code>high_value</code>, with byte order specified by <code>border</code>, memory attributes specified by <code>mattr</code>, and access hint specified by <code>hint</code>. <code>otype</code> specifies the memory ordering attribute of this access, and must be UNORDERED or ACQUIRE. No value is returned.</td>
</tr>
<tr>
<td><code>fp_mem_to_fr_format(mem, size)</code></td>
<td>Converts a floating-point value in memory format to floating-point register format.</td>
</tr>
<tr>
<td><code>mem_write(value, paddr, size, border, mattr, otype, hint)</code></td>
<td>Writes the least significant <code>size</code> bytes of <code>value</code> into memory starting at the physical memory address specified by <code>paddr</code> with byte order specified by <code>border</code>, memory attributes specified by <code>mattr</code>, and access hint specified by <code>hint</code>. <code>otype</code> specifies the memory ordering attribute of this access, and must be UNORDERED or RELEASE. No value is returned.</td>
</tr>
<tr>
<td><code>mem_write16(gr_value, ar_value, paddr, border, mattr, otype, hint)</code></td>
<td>Writes the 8 bytes of <code>gr_value</code> into memory starting at the physical memory address specified by <code>paddr</code>, and the 8 bytes of <code>ar_value</code> into memory starting at the physical memory address specified by <code>(paddr + 8)</code>, with byte order specified by <code>border</code>, memory attributes specified by <code>mattr</code>, and access hint specified by <code>hint</code>. <code>otype</code> specifies the memory ordering attribute of this access, and must be UNORDERED or RELEASE. No value is returned.</td>
</tr>
</tbody>
</table>
### Table 3-1. Pseudo-Code Functions (Continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>mem_xchg(data, paddr, size, byte_order, mattr, otype, hint)</code></td>
<td>Returns size bytes from memory starting at the physical address specified by <code>paddr</code>. The read is conditioned by the locality hint specified by <code>hint</code>. After the read, the least significant <code>size</code> bytes of data are written to <code>size</code> bytes in memory starting at the physical address specified by <code>paddr</code>. The read and write are performed atomically. Both the read and the write are conditioned by the memory attribute specified by <code>mattr</code> and the byte ordering in memory is specified by <code>byte_order</code>. <code>otype</code> specifies the memory ordering attribute of this access, and must be <code>ACQUIRE</code>.</td>
</tr>
<tr>
<td><code>mem_xchg_add(add_val, paddr, size, byte_order, mattr, otype, hint)</code></td>
<td>Returns <code>size</code> bytes from memory starting at the physical address specified by <code>paddr</code>. The read is conditioned by the locality hint specified by <code>hint</code>. The least significant <code>size</code> bytes of the sum of the value read from memory and <code>add_val</code> is then written to <code>size</code> bytes in memory starting at the physical address specified by <code>paddr</code>. The read and write are performed atomically. Both the read and the write are conditioned by the memory attribute specified by <code>mattr</code> and the byte ordering in memory is specified by <code>byte_order</code>. <code>otype</code> specifies the memory ordering attribute of this access, and has the value <code>ACQUIRE</code> or <code>RELEASE</code>.</td>
</tr>
<tr>
<td><code>mem_xchg_cond(cmp_val, data, paddr, size, byte_order, mattr, otype, hint)</code></td>
<td>Returns <code>size</code> bytes from memory starting at the physical address specified by <code>paddr</code>. The read is conditioned by the locality hint specified by <code>hint</code>. If the value read from memory is equal to <code>cmp_val</code>, then the least significant <code>size</code> bytes of data are written to <code>size</code> bytes in memory starting at the physical address specified by <code>paddr</code>. If the write is performed, the read and write are performed atomically. Both the read and the write are conditioned by the memory attribute specified by <code>mattr</code> and the byte ordering in memory is specified by <code>byte_order</code>. <code>otype</code> specifies the memory ordering attribute of this access, and has the value <code>ACQUIRE</code> or <code>RELEASE</code>.</td>
</tr>
<tr>
<td><code>mem_xchg16_cond(cmp_val, gr_data, ar_data, paddr, byte_order, mattr, otype, hint)</code></td>
<td>Returns 8 bytes from memory starting at the physical address specified by <code>paddr</code>. The read is conditioned by the locality hint specified by <code>hint</code>. If the value read from memory is equal to <code>cmp_val</code>, then the 8 bytes of <code>gr_data</code> are written to 8 bytes in memory starting at the physical address specified by <code>paddr &amp; ~0x4</code>, and the 8 bytes of <code>ar_data</code> are written to 8 bytes in memory starting at the physical address specified by <code>((paddr &amp; ~0x4) + 8)</code>. If the write is performed, the read and write are performed atomically. Both the read and the write are conditioned by the memory attribute specified by <code>mattr</code> and the byte ordering in memory is specified by <code>byte_order</code>. The byte ordering only affects the ordering of bytes within each of the 8-byte values stored. <code>otype</code> specifies the memory ordering attribute of this access, and has the value <code>ACQUIRE</code> or <code>RELEASE</code>.</td>
</tr>
<tr>
<td><code>ordering_fence()</code></td>
<td>Ensures prior data memory references are made visible before future data memory references are made visible by the processor.</td>
</tr>
<tr>
<td><code>partially_implemented_ip()</code></td>
<td>Implementation-dependent routine which returns TRUE if the implementation, on an Unimplemented Instruction Address trap, writes IIP with the sign-extended virtual address or zero-extended physical address for what would have been the next value of IP. Returns FALSE if the implementation, on this trap, simply writes IIP with the full address which would have been the next value of IP.</td>
</tr>
<tr>
<td><code>pr_phys_to_virt(phys_id)</code></td>
<td>Returns the virtual register id of the predicate from the physical register id, <code>phys_id</code> of the predicate.</td>
</tr>
<tr>
<td><code>rotate_regs()</code></td>
<td>Decrements the Register Rename Base registers, effectively rotating the register files. CFM.rb_gr is decremented only if CFM.sor is non-zero.</td>
</tr>
<tr>
<td><code>rse_enable_current_frame_load()</code></td>
<td>If the RSE load pointer (RSE.BSPLoad) is greater than AR[BSP], the RSE.CFLE bit is set to indicate that mandatory RSE loads are allowed to restore registers in the current frame (in no other case does the RSE spill or fill registers in the current frame). This function does not perform mandatory RSE loads. This procedure does not cause any interruptions.</td>
</tr>
</tbody>
</table>
### Table 3-1. Pseudo-Code Functions (Continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>rseEnsureRegsLoaded(number_of_bytes)</td>
<td>All registers and NaT collections between AR[BSP] and (AR[BSP]-number_of_bytes) which are not already in stacked registers are loaded into the register stack with mandatory RSE loads. If the number of registers to be loaded is greater than RSE.N_STACK_PHYS an Illegal Operation fault is raised. All registers starting with backing store address (AR[BSP]-8) and decrementing down to and including backing store address (AR[BSP]-number_of_bytes) are made part of the dirty partition. With exception of the current frame, all other stacked registers are made part of the invalid partition. Note that number_of_bytes may be zero. The resulting sequence of RSE loads may be interrupted. Mandatory RSE loads may cause an interruption; see Table 6-6 on page 2:126.</td>
</tr>
<tr>
<td>rseInvalidateNonCurrentRegs()</td>
<td>All registers outside the current frame are invalidated.</td>
</tr>
<tr>
<td>rseLoad(type)</td>
<td>Restores a register or NaT collection from the backing store (load_address = RSE.BspLoad-8). If load_address{8:3} is equal to 0x3f then a NaT collection is loaded into a NaT dispersal register. (dispersal register may not be the same as AR[RNAT].) If load_address{8:3} is not equal to 0x3f then the register RSE.LoadReg-1 is loaded and the NaT bit for that register is set to dispersal_register{load_address{8:3}}. If the load is successful RSE.BspLoad is decremented by 8. If the load is successful and a register was loaded RSE.LoadReg is decremented by 1 (possibly wrapping in the stacked registers). The load moves a register from the invalid partition to the current frame if RSE.CFLE is 1, or to the clean partition if RSE.CFLE is 0. For mandatory RSE loads, type is MANDATORY. Mandatory RSE loads may cause interruptions. See Table 6-6 on page 2:126.</td>
</tr>
<tr>
<td>rseNewFrame(current_frame_size, new_frame_size)</td>
<td>A new frame is defined without changing any register renaming. The new frame size is completely defined by the new_frame_size parameter (successive calls are not cumulative). If new_frame_size is larger than current_frame_size and the number of registers in the invalid and clean partitions is less than the size of frame growth then mandatory RSE stores are issued until enough registers are available. The resulting sequence of RSE stores may be interrupted. Mandatory RSE stores may cause interruptions; see Table 6-6 on page 2:126.</td>
</tr>
<tr>
<td>rsePreserveFrame(preserved_frame_size)</td>
<td>The number of registers specified by preserved_frame_size are marked to be preserved by the RSE. Register renaming causes the preserved_frame_size registers after GR[32] to be renamed to GR[32]. AR[BSP] is updated to contain the backing store address where the new GR[32] will be stored.</td>
</tr>
<tr>
<td>rseRestoreFrame(preserved_sol, growth, current_frame_size)</td>
<td>The first two parameters define how the current frame is about to be updated by a branch return or rfi: preserved_sol defines how many registers need to be restored below RSE.BOF: growth defines by how many registers the top of the current frame will grow (growth will generally be negative). The number of registers specified by preserved_sol are marked to be restored. Register renaming causes the preserved_sol registers before GR[32] to be renamed to GR[32]. AR[BSP] is updated to contain the backing store address where the new GR[32] will be stored. If the number of dirty and clean registers is less than preserved_sol then mandatory RSE loads must be issued before the new current frame is considered valid. This function does not perform mandatory RSE loads. This function returns TRUE if the preserved frame grows beyond the invalid and clean regions into the dirty region. In this case the third argument, current_frame_size, is used to force the returned to frame to zero (see Section 6.5.5, “Bad PFS Used by Branch Return” on page 2:124).</td>
</tr>
</tbody>
</table>
### Table 3-1. Pseudo-Code Functions (Continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>rse_store(type)</strong></td>
<td>Saves a register or NaT collection to the backing store (store_address = AR[BSPSTORE]). If store_address(8:3) is equal to 0x3f then the NaT collection AR[RNAT] is stored. If store_address(8:3) is not equal to 0x3f then the register RSE.StoreReg is stored and the NaT bit from that register is deposited in AR[RNAT][store_address(8:3)]. If the store is successful AR[BSPSTORE] is incremented by 8. If the store is successful and a register was stored RSE.StoreReg is incremented by 1 (possibly wrapping in the stacked registers). This store moves a register from the dirty partition to the clean partition. For mandatory RSE stores, type is MANDATORY. Mandatory RSE stores may cause interruptions. See Table 6-6 &quot;RSE Interruption Summary&quot; on page 2:126.</td>
</tr>
<tr>
<td><strong>rse_update_internal_stack_pointers(new_store_pointer)</strong></td>
<td>Given a new value for AR[BSPSTORE] (new_store_pointer) this function computes the new value for AR[BSP]. This value is equal to new_store_pointer plus the number of dirty registers plus the number of intervening NaT collections. This means that the size of the dirty partition is the same before and after a write to AR[BSPSTORE]. All clean registers are moved to the invalid partition.</td>
</tr>
<tr>
<td><strong>sign_ext(value, pos)</strong></td>
<td>Returns a 64 bit number with bits pos-1 through 0 taken from value and bit pos-1 of value replicated in bit positions pos through 63. If pos is greater than or equal to 64, value is returned.</td>
</tr>
<tr>
<td>*<em>spontaneous_deferral(paddr, size, border, mattr, otype, hint, <em>defer)</em></em></td>
<td>Implementation-dependent routine which optionally forces *defer to TRUE if all of the following are true: spontaneous deferral is enabled, spontaneous deferral is permitted by the programming model, and the processor determines it would be advantageous to defer the speculative load (e.g., based on a miss in some particular level of cache).</td>
</tr>
<tr>
<td><strong>spontaneous_deferral_enabled()</strong></td>
<td>Implementation-dependent routine which returns TRUE or FALSE, depending on whether spontaneous deferral of speculative loads is enabled or disabled in the processor.</td>
</tr>
<tr>
<td><strong>tlb_access_key(vaddr)</strong></td>
<td>This function returns the access key from the TLB for the entry corresponding to vaddr.</td>
</tr>
<tr>
<td><strong>tlb_broadcast_purge(rid, vaddr, size, type)</strong></td>
<td>Sends a broadcast purge DTC and ITC transaction to other processors in the multi-processor coherency domain, where the region identifier (rid), virtual address (vaddr) and page size (size) specify the translation entry to purge. The operation waits until all processors that receive the purge have completed the purge operation. The purge type (type) specifies whether the ALAT on other processors should also be purged in conjunction with the TC.</td>
</tr>
<tr>
<td><strong>tlb_enter_privileged_code()</strong></td>
<td>This function determines the new privilege level for epc from the TLB entry for the page containing this instruction. If the page containing the epc instruction has execute-only page access rights and the privilege level assigned to the page is higher than (numerically less than) the current privilege level, then the current privilege level is set to the privilege level field in the translation for the page containing the epc instruction.</td>
</tr>
<tr>
<td><strong>tlb_grant_permission(vaddr, type, pl)</strong></td>
<td>Returns a boolean indicating if read, write access is granted for the specified virtual memory address (vaddr) and privilege level (pl). The access type (type) specifies either read or write. The following faults are checked; VHPT Translation, TLB Miss, Nested TLB, Page Not Present, NaT Page Consumption, and Key Miss. If a fault is generated, this function does not return.</td>
</tr>
<tr>
<td><strong>tlb_insert_data(slot, pte0, pte1, vaddr, rid, tr)</strong></td>
<td>Inserts an entry into the DTLB, at the specified slot number. pte0.pte1 compose the translation. vaddr and rid specify the virtual address and region identifier for the translation. If tr is true the entry is placed in the TR section, otherwise the TC section.</td>
</tr>
<tr>
<td><strong>tlb_insert_inst(slot, pte0, pte1, vaddr, rid, tr)</strong></td>
<td>Inserts an entry into the ITLB, at the specified slot number. pte0.pte1 compose the translation. vaddr and rid specify the virtual address and region identifier for the translation. If tr is true, the entry is placed in the TR section, otherwise the TC section.</td>
</tr>
</tbody>
</table>
Table 3-1. Pseudo-Code Functions (Continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>tlb_may_purge_dtc_entries(rid, vaddr, size)</td>
<td>May locally purge DTC entries that match the specified virtual address (vaddr), region identifier (rid) and page size (size). May also invalidate entries that partially overlap the parameters. The extent of purging is implementation dependent. If the purge size is not supported, an implementation may generate a machine check abort or over purge the translation cache up to and including removal of all entries from the translation cache.</td>
</tr>
<tr>
<td>tlb_may_purge_itc_entries(rid, vaddr, size)</td>
<td>May locally purge ITC entries that match the specified virtual address (vaddr), region identifier (rid) and page size (size). May also invalidate entries that partially overlap the parameters. The extent of purging is implementation dependent. If the purge size is not supported, an implementation may generate a machine check abort or over purge the translation cache up to and including removal of all entries from the translation cache.</td>
</tr>
<tr>
<td>tlb_must_purge_dtc_entries(rid, vaddr, size)</td>
<td>Purges all local, possibly overlapping, DTC entries matching the specified region identifier (rid), virtual address (vaddr) and page size (size). vaddr(63:61) (VRN) is ignored in the purge, i.e all entries that match vaddr(60:0) must be purged regardless of the VRN bits. If the purge size is not supported, an implementation may generate a machine check abort or over purge the translation cache up to and including removal of all entries from the translation cache. If the specified purge values overlap with an existing DTR translation, an implementation may generate a machine check abort.</td>
</tr>
<tr>
<td>tlb_must_purge_itc_entries(rid, vaddr, size)</td>
<td>Purges all local, possibly overlapping, ITC entry matching the specified region identifier (rid), virtual address (vaddr) and page size (size). vaddr(63:61) (VRN) is ignored in the purge, i.e all entries that match vaddr(60:0) must be purged regardless of the VRN bits. If the purge size is not supported, an implementation may generate a machine check abort or over purge the translation cache up to and including removal of all entries from the translation cache. If the specified purge values overlap with an existing ITR translation, an implementation may generate a machine check abort.</td>
</tr>
<tr>
<td>tlb_must_purge_dtr_entries(rid, vaddr, size)</td>
<td>Purges all local, possibly overlapping, DTR entries matching the specified region identifier (rid), virtual address (vaddr) and page size (size). vaddr(63:61) (VRN) is ignored in the purge, i.e all entries that match vaddr(60:0) must be purged regardless of the VRN bits. If the purge size is not supported, an implementation may generate a machine check abort or over purge the translation cache up to and including removal of all entries from the translation cache.</td>
</tr>
<tr>
<td>tlb_must_purge_itr_entries(rid, vaddr, size)</td>
<td>Purges all local, possibly overlapping, ITR entry matching the specified region identifier (rid), virtual address (vaddr) and page size (size). vaddr(63:61) (VRN) is ignored in the purge, i.e all entries that match vaddr(60:0) must be purged regardless of the VRN bits. If the purge size is not supported, an implementation may generate a machine check abort or over purge the translation cache up to and including removal of all entries from the translation cache.</td>
</tr>
<tr>
<td>tlb_purge_translation_cache(loop)</td>
<td>Removes 1 to N translations from the local processor's ITC and DTC. The number of entries removed is implementation-specific. The parameter loop is used to generate an implementation-specific purge parameter.</td>
</tr>
<tr>
<td>tlb_replacement_algorithm(tlb)</td>
<td>Returns the next ITC or DTC slot number to replace. Replacement algorithms are implementation-specific. tlb specifies to perform the algorithm on the ITC or DTC.</td>
</tr>
<tr>
<td>tlb_search_pkr(key)</td>
<td>Searches for a valid protection key register with a matching protection key. The search algorithm is implementation-specific. Returns the PKR register slot number if found, otherwise returns Not Found.</td>
</tr>
</tbody>
</table>
Table 3-1. Pseudo-Code Functions (Continued)

<table>
<thead>
<tr>
<th>Function</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>tlb_translate(vaddr, size, type, cpl, *attr, *defer)</code></td>
<td>Returns the translated data physical address for the specified virtual memory address (<code>vaddr</code>) when translation enabled; otherwise, returns <code>vaddr</code>. <code>size</code> specifies the size of the access, <code>type</code> specifies the type of access (e.g., read, write, advance, spec). <code>cpl</code> specifies the privilege level for access checking purposes. <code>*attr</code> returns the mapped physical memory attribute. If any fault conditions are detected and deferred, <code>tlb_translate</code> returns with <code>*defer</code> set. If a fault is generated but the fault is not deferred, <code>tlb_translate</code> does not return. <code>tlb_translate</code> checks the following faults: • VHPT Data fault • Data Nested TLB fault • Data TLB fault • Alternate Data TLB fault • Data page not present fault • Data NaT page consumption fault • Data key miss fault • Data key permission fault • Data access rights fault • Data dirty bit fault • Data access bit fault • Data debug fault • Unsupported Data Reference fault</td>
</tr>
<tr>
<td><code>tlb_translate_nonaccess(vaddr, type)</code></td>
<td>Returns the translated data physical address for the specified virtual memory address (<code>vaddr</code>). <code>type</code> specifies the type of access (e.g., FC, TPA). If a fault is generated, <code>tlb_translate_nonaccess</code> does not return. The following faults are checked: • VHPT data fault • Data TLB fault • Data Nested TLB fault • Data page not present fault • Data NaT page consumption fault</td>
</tr>
<tr>
<td><code>tlb_vhpt_hash(vrn, vaddr61, rid, size)</code></td>
<td>Generates a VHPT entry address for the specified virtual region number (<code>vrn</code>) and 61-bit virtual offset (<code>vaddr61</code>), region identifier (<code>rid</code>) and page size (<code>size</code>). <code>Tlb_vhpt_hash</code> hashes <code>vaddr</code>, <code>rid</code> and <code>size</code> parameters to produce a hash index. The hash index is then masked based on PTA.size and concatenated with PTA.base to generate the VHPT entry address. The long format hash is implementation-specific.</td>
</tr>
<tr>
<td><code>tlb_vhpt_tag(vaddr, rid, size)</code></td>
<td>Generates a VHPT tag identifier for the specified virtual address (<code>vaddr</code>), region identifier (<code>rid</code>) and page size (<code>size</code>). <code>Tlb_vhpt_tag</code> hashes the <code>vaddr</code>, <code>rid</code> and <code>size</code> parameters to produce translation identifier. The tag in conjunction with the hash index is used to uniquely identify translations in the VHPT. Tag generation is implementation-specific. All processor models tag function must guarantee that bit 63 of the generated tag is zero (ti bit).</td>
</tr>
<tr>
<td><code>unimplemented_physical_address(paddr)</code></td>
<td>Return TRUE if the presented physical address is unimplemented on this processor model; FALSE otherwise. This function is model-specific.</td>
</tr>
<tr>
<td><code>undefined()</code></td>
<td>Returns an undefined 64-bit value.</td>
</tr>
<tr>
<td><code>undefined_behavior()</code></td>
<td>Causes undefined processor behavior. Extent of undefined behavior is described in Section 3.5, “Undefined Behavior” on page 1:38.</td>
</tr>
<tr>
<td><code>unimplemented_virtual_address(vaddr)</code></td>
<td>Return TRUE if the presented virtual address is unimplemented on this processor model; FALSE otherwise. This function is model-specific.</td>
</tr>
<tr>
<td><code>fp_update_fpsr(sf, tmp_fp_env)</code></td>
<td>Copies a floating-point instruction’s local state into the global FPSR.</td>
</tr>
<tr>
<td><code>fp_update_psr(dest_freg)</code></td>
<td>Conditionally sets PSR.mfl or PSR.mfh based on <code>dest_freg</code>.</td>
</tr>
<tr>
<td><code>zero_ext(value, pos)</code></td>
<td>Returns a 64 bit unsigned number with bits <code>pos-1</code> through 0 taken from <code>value</code> and zeroes in bit positions <code>pos</code> through 63. If <code>pos</code> is greater than or equal to 64, <code>value</code> is returned.</td>
</tr>
</tbody>
</table>
Each Itanium instruction is categorized into one of six types; each instruction type may be executed on one or more execution unit types. Table 4-1 lists the instruction types and the execution unit type on which they are executed:

**Table 4-1. Relationship between Instruction Type and Execution Unit Type**

<table>
<thead>
<tr>
<th>Instruction Type</th>
<th>Description</th>
<th>Execution Unit Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>Integer ALU</td>
<td>I-unit or M-unit</td>
</tr>
<tr>
<td>I</td>
<td>Non-ALU integer</td>
<td>I-unit</td>
</tr>
<tr>
<td>M</td>
<td>Memory</td>
<td>M-unit</td>
</tr>
<tr>
<td>F</td>
<td>Floating-point</td>
<td>F-unit</td>
</tr>
<tr>
<td>B</td>
<td>Branch</td>
<td>B-unit</td>
</tr>
<tr>
<td>L+X</td>
<td>Extended</td>
<td>I-unit/B-unit²</td>
</tr>
</tbody>
</table>

a. L+X Major Opcodes 0 - 7 execute on an I-unit. L+X Major Opcodes 8 - F execute on a B-unit.

Three instructions are grouped together into 128-bit sized and aligned containers called bundles. Each bundle contains three 41-bit instruction slots and a 5-bit template field. The format of a bundle is depicted in Figure 4-1.

**Figure 4-1. Bundle Format**

```
127 87 86 46 45 5 4 0
instruction slot 2  instruction slot 1  instruction slot 0  template
 41 41 41 5
```

The template field specifies two properties: stops within the current bundle, and the mapping of instruction slots to execution unit types. Not all combinations of these two properties are allowed - Table 4-2 indicates the defined combinations. The three rightmost columns correspond to the three instruction slots in a bundle; listed within each column is the execution unit type controlled by that instruction slot for each encoding of the template field. A double line to the right of an instruction slot indicates that a stop occurs at that point within the current bundle. See “Instruction Encoding Overview” on page 32 for the definition of a stop. Within a bundle, execution order proceeds from slot 0 to slot 2. Unused template values (appearing as empty rows in Table 4-2) are reserved and cause an Illegal Operation fault.

Extended instructions, used for long immediate integer and long branch instructions, occupy two instruction slots. Depending on the major opcode, extended instructions execute on a B-unit (long branch/call) or an I-unit (all other L+X instructions).
### Table 4-2. Template Field Encoding and Instruction Slot Mapping

<table>
<thead>
<tr>
<th>Template</th>
<th>Slot 0</th>
<th>Slot 1</th>
<th>Slot 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>M-unit</td>
<td>I-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>01</td>
<td>M-unit</td>
<td>I-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>02</td>
<td>M-unit</td>
<td>I-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>03</td>
<td>M-unit</td>
<td>L-unit</td>
<td>X-unit</td>
</tr>
<tr>
<td>04</td>
<td>M-unit</td>
<td>L-unit</td>
<td>X-unit</td>
</tr>
<tr>
<td>05</td>
<td>M-unit</td>
<td>L-unit</td>
<td>X-unit</td>
</tr>
<tr>
<td>06</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>07</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>08</td>
<td>M-unit</td>
<td>M-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>09</td>
<td>M-unit</td>
<td>M-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>0A</td>
<td>M-unit</td>
<td>M-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>0B</td>
<td>M-unit</td>
<td>M-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>0C</td>
<td>M-unit</td>
<td>M-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>0D</td>
<td>M-unit</td>
<td>M-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>0E</td>
<td>M-unit</td>
<td>M-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>0F</td>
<td>M-unit</td>
<td>M-unit</td>
<td>I-unit</td>
</tr>
<tr>
<td>10</td>
<td>M-unit</td>
<td>I-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>11</td>
<td>M-unit</td>
<td>I-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>12</td>
<td>M-unit</td>
<td>B-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>13</td>
<td>M-unit</td>
<td>B-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>14</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>B-unit</td>
<td>B-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>17</td>
<td>B-unit</td>
<td>B-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>18</td>
<td>M-unit</td>
<td>M-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>19</td>
<td>M-unit</td>
<td>M-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>1A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1C</td>
<td>M-unit</td>
<td>F-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>1D</td>
<td>M-unit</td>
<td>F-unit</td>
<td>B-unit</td>
</tr>
<tr>
<td>1E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1F</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

a. The MLX template was formerly called MLI, and for compatibility, the X slot may encode break.i and nop.i in addition to any X-unit instruction.

### 4.1 Format Summary

All instructions in the instruction set are 41 bits in length. The leftmost 4 bits (40:37) of each instruction are the major opcode. Table 4-3 shows the major opcode assignments for each of the 5 instruction types — ALU (A), Integer (I), Memory (M), Floating-point (F), and Branch (B). Bundle template bits are used to distinguish among the 4 columns, so the same major op values can be reused in each column.
Unused major ops (appearing as blank entries in Table 4-3) behave in one of four ways:

- Ignored major ops (white entries in Table 4-3) execute as \texttt{nop} instructions.
- Reserved major ops (light gray in the gray scale version of Table 4-3, brown in the color version) cause an Illegal Operation fault.
- Reserved if PR[qp] is 1 major ops (dark gray in the gray scale version of Table 4-3, purple in the color version) cause an Illegal Operation fault if the predicate register specified by the qp field of the instruction (bits 5:0) is 1 and execute as a \texttt{nop} instruction if 0.
- Reserved if PR[qp] is 1 B-unit major ops (medium gray in the gray scale version of Table 4-3, cyan in the color version) cause an Illegal Operation fault if the predicate register specified by the qp field of the instruction (bits 5:0) is 1 and execute as a \texttt{nop} instruction if 0. These differ from the Reserved if PR[qp] is 1 major ops (purple) only in their RAW dependency behavior (see “RAW Dependency Table” on page 338).

### Table 4-3. Major Opcode Assignments

<table>
<thead>
<tr>
<th>Major Op (Bits 40:37)</th>
<th>Instruction Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Misc</td>
</tr>
<tr>
<td>1</td>
<td>Sys/Mem Mgmt</td>
</tr>
<tr>
<td>2</td>
<td>FP Misc</td>
</tr>
<tr>
<td>3</td>
<td>Indirect Call</td>
</tr>
<tr>
<td>4</td>
<td>Deposit</td>
</tr>
<tr>
<td>5</td>
<td>Int Ld +Reg/letf</td>
</tr>
<tr>
<td>6</td>
<td>FP Ld/St +Reg/setf</td>
</tr>
<tr>
<td>7</td>
<td>MM Mpy/Shift</td>
</tr>
<tr>
<td>8</td>
<td>ALU/MM ALU</td>
</tr>
<tr>
<td>9</td>
<td>Add Imm22</td>
</tr>
<tr>
<td>A</td>
<td>Int Ld +Reg/setf</td>
</tr>
<tr>
<td>B</td>
<td>FP Ld/St +Imm</td>
</tr>
<tr>
<td>C</td>
<td>FP Ld/St +Imm</td>
</tr>
<tr>
<td>D</td>
<td>FP Ld +Reg/letf</td>
</tr>
<tr>
<td>E</td>
<td>FP Ld/St +Reg/setf</td>
</tr>
<tr>
<td>F</td>
<td>FP Ld/St +Reg/setf</td>
</tr>
</tbody>
</table>

Table 4-4 on page 4-258 summarizes all the instruction formats. The instruction fields are color-coded for ease of identification, as described in Table 4-5 on page 4-260. A color version of this chapter is available for those heavily involved in working with the instruction encodings.

The instruction field names, used throughout this chapter, are described in Table 4-6 on page 4-260. The set of special notations (such as whether an instruction is privileged) are listed in Table 4-7 on page 4-261. These notations appear in the “Instruction” column of the opcode tables.

Most instruction containing immediates encode those immediates in more than one instruction field. For example, the 14-bit immediate in the Add Imm14 instruction (format A4) is formed from the imm7b, imm6d, and s fields. Table 4-74 on page 4-332 shows how the immediates are formed from the instruction fields for each instruction which has an immediate.
### Table 4-4. Instruction Format Summary

<table>
<thead>
<tr>
<th>Category</th>
<th>Instruction Format</th>
<th>Format</th>
<th>Length</th>
<th>Notation</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALU</td>
<td>A1</td>
<td>8</td>
<td>x3a_x4_x2b</td>
<td>r3</td>
</tr>
<tr>
<td>ALU Imm8</td>
<td>A2</td>
<td>8</td>
<td>x3a_x4_imm8</td>
<td>r3</td>
</tr>
<tr>
<td>Add Imm14</td>
<td>A3</td>
<td>8</td>
<td>x3a_x4_x2b</td>
<td>r3</td>
</tr>
<tr>
<td>Add Imm22</td>
<td>A4</td>
<td>8</td>
<td>x3a_x4_imm22</td>
<td>r3</td>
</tr>
<tr>
<td>Compare</td>
<td>A5</td>
<td>9</td>
<td>imm9d_imm27b</td>
<td>r3</td>
</tr>
<tr>
<td>Compare to Zero</td>
<td>A6</td>
<td>c</td>
<td>x3a_x4_x2b</td>
<td>r3</td>
</tr>
<tr>
<td>Compare Imm15</td>
<td>A7</td>
<td>c</td>
<td>x3a_x4_x2b</td>
<td>r3</td>
</tr>
<tr>
<td>MM ALU</td>
<td>A8</td>
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### Table 4-4. Instruction Format Summary (Continued)

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<td>x3 x2 x4 y ih imm20a</td>
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<td>Translation Purge M44</td>
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<td>Translation Access M45</td>
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<td>Counted Branch B2</td>
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<td>Indirect Call B5</td>
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<td>Fixed Multiply Add F2</td>
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<td>FP Compare F4</td>
<td>4 r2 st f3</td>
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<td>FP Class F5</td>
<td>5 t2</td>
<td>t1 t0</td>
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### Table 4-5. Instruction Field Color Key

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<td>Integer Instruction</td>
<td>Opcode Hint Extension</td>
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<td>Memory Instruction</td>
<td>Immediate</td>
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<td>Branch Instruction</td>
<td>Indirect Source</td>
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<tr>
<td>Floating-point Instruction</td>
<td>Predicate Destination</td>
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<td>Integer Source</td>
<td>Integer Destination</td>
</tr>
<tr>
<td>Memory Source</td>
<td>Memory Source &amp; Destination</td>
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<tr>
<td>Shift Source</td>
<td>Shift Immediate</td>
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<tr>
<td>Special Register Source</td>
<td>Special Register Destination</td>
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<td>Floating-point Source</td>
<td>Floating-point Destination</td>
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<td>Branch Source</td>
<td>Branch Destination</td>
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<td>Address Source</td>
<td>Branch Tag Immediate</td>
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<tr>
<td>Qualifying Predicate</td>
<td>Reserved Instruction</td>
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<td>Ignored Field/Instruction</td>
<td>Reserved Inst if PR[qp] is 1</td>
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<td>Reserved B-type Inst if PR[qp] is 1</td>
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### Table 4-6. Instruction Field Names

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<td>branch register source/target</td>
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<td>btype</td>
<td>branch type opcode extension</td>
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<td>c</td>
<td>complement compare relation opcode extension</td>
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<td>ccount_{bc}</td>
<td>multimedia shift left complemented shift count immediate</td>
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<td>count_{6d}, count_{6d}</td>
<td>multimedia shift right/shift right pair shift count immediate</td>
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<td>cpos_{x}</td>
<td>deposit complemented bit position immediate</td>
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<td>cr3</td>
<td>control register source/target</td>
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<td>ct2d</td>
<td>multimedia multiply shift/shift and add shift count immediate</td>
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<td>f</td>
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</tbody>
</table>
The remaining sections of this chapter present the detailed encodings of all instructions. The “A-Unit Instruction encodings” are presented first, followed by the “I-Unit Instruction Encodings” on page 272, “M-Unit Instruction Encodings” on page 285, “B-Unit Instruction Encodings” on page 313, “F-Unit Instruction Encodings” on page 320, and “X-Unit Instruction Encodings” on page 329.

Within each section, the instructions are grouped by function, and appear with their instruction format in the same order as in Table 4-4 “Instruction Format Summary” on page 3:258. The opcode extension fields are briefly described and tables present the opcode extension assignments. Unused instruction encodings (appearing as blank entries in the opcode extensions tables) behave in one of four ways:

- Ignored instructions (white color entries in the tables) execute as `nop` instructions.
- Reserved instructions (light gray color in the gray scale version of the tables, brown color in the color version) cause an Illegal Operation fault.
- Reserved if PR[qp] is 1 instructions (dark gray in the gray scale version of the tables, purple in the color version) cause an Illegal Operation fault if the predicate register specified by the qp field of the instruction (bits 5:0) is 1 and execute as a `nop` instruction if 0.
- Reserved if PR[qp] is 1 B-unit instructions (medium gray in the gray scale version of the tables, cyan in the color version) cause an Illegal Operation fault if the predicate register specified by the qp field of the instruction (bits 5:0) is 1 and execute as a `nop` instruction if 0. These differ from the Reserved if PR[qp] is 1 instructions (purple) only in their RAW dependency behavior (see “RAW Dependency Table” on page 338).

Some processors may implement the Reserved if PR[qp] is 1 (purple) and Reserved if PR[qp] is 1 B-unit (cyan) encodings in the L+X opcode space as Reserved (brown). These encodings appear in the L+X column of Table 4-3 on page 4-257, and in Table 4-69 on page 4-330, Table 4-70 on
page 4-330, Table 4-71 on page 4-331, and Table 4-72 on page 4-331. On processors which implement these encodings as Reserved (brown), the operating system is required to provide an Illegal Operation fault handler which emulates them as Reserved if PR[qp] is 1 (cyan/purple) by decoding the reserved opcodes, checking the qualifying predicate, and returning to the next instruction if PR[qp] is 0.

Constant 0 fields in instructions must be 0 or undefined operation results. The undefined operation may include checking that the constant field is 0 and causing an Illegal Operation fault if it is not. If an instruction having a constant 0 field also has a qualifying predicate (qp field), the fault or other undefined operation must not occur if PR[qp] is 0. For constant 0 fields in instruction bits 5:0 (normally used for qp), the fault or other undefined operation may or may not depend on the PR addressed by those bits.

Ignored (white space) fields in instructions should be coded as 0. Although ignored in this revision of the architecture, future architecture revisions may define these fields as hint extensions. These hint extensions will be defined such that the 0 value in each field corresponds to the default hint. It is expected that assemblers will automatically set these fields to zero by default.

## 4.2 A-Unit Instruction Encodings

### 4.2.1 Integer ALU

All integer ALU instructions are encoded within major opcode 8 using a 2-bit opcode extension field in bits 35:34 ($x_{2a}$) and most have a second 2-bit opcode extension field in bits 28:27 ($x_{2b}$), a 4-bit opcode extension field in bits 32:29 ($x_{4}$), and a 1-bit reserved opcode extension field in bit 33 ($v_e$). Table 4-8 shows the 2-bit $x_{2a}$ and 1-bit $v_e$ assignments, Table 4-9 shows the integer ALU 4-bit+2-bit assignments, and Table 4-12 on page 4-268 shows the multimedia ALU 1-bit+2-bit assignments (which also share major opcode 8).

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>$x_{2a}$ Bits 35:34</th>
<th>$v_e$ Bit 33</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

- **0**: Integer ALU 4-bit+2-bit Ext (Table 4-9)
- **1**: Multimedia ALU 1-bit+2-bit Ext (Table 4-12)
- **2**: adds – imm_{14} A4
- **3**: addp4 – imm_{14} A4
Table 4-9. Integer ALU 4-bit+2-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x2a Bits 35:34</th>
<th>x2b Bits 32:29</th>
<th>x4 Bits 31:29</th>
<th>x4 Bits 32:29</th>
<th>Bits 28:27</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>add A1</td>
<td>add +1 A1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>sub –1 A1</td>
<td>sub A1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>addp4 A1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>and A1</td>
<td>andcm A1</td>
<td>or A1</td>
<td>xor A1</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>shiadd A2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>shiaddp4 A2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
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<td>6</td>
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<td></td>
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<td></td>
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<td>8</td>
<td>sub – imm8 A3</td>
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</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
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</tr>
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</table>

4.2.1.1 Integer ALU – Register-Register

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<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>add</td>
<td>r1 = r2, r3</td>
<td>8</td>
<td>x2a 0 0 0</td>
</tr>
<tr>
<td>sub</td>
<td>r1 = r2, r3</td>
<td>8</td>
<td>x2a 1 1 0</td>
</tr>
<tr>
<td>addp4</td>
<td>r1 = r2, r3</td>
<td>8</td>
<td>x2a 2 0 0</td>
</tr>
<tr>
<td>and</td>
<td>r1 = r2, r3</td>
<td>8</td>
<td>x2a 3 1 2</td>
</tr>
<tr>
<td>or</td>
<td>r1 = r2, r3</td>
<td>8</td>
<td>x2a 4 1 2</td>
</tr>
</tbody>
</table>

4.2.1.2 Shift Left and Add

<table>
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<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>shiadd</td>
<td>r1 = r2, count2, r3</td>
<td>8</td>
<td>x2a 4 6 0</td>
</tr>
<tr>
<td>shiaddp4</td>
<td>r1 = r2, count2, r3</td>
<td>8</td>
<td>x2a 4 6 0</td>
</tr>
</tbody>
</table>
4.2.1.3 Integer ALU – Immediate₈-Register

A3

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<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>sub</td>
<td></td>
<td>8</td>
<td>x₂ₐ vₑ x₄ x₂₉</td>
</tr>
<tr>
<td>and</td>
<td>r₁ = imm₈, r₃</td>
<td>0 0 9 1</td>
<td></td>
</tr>
<tr>
<td>andcm</td>
<td>or</td>
<td>xor</td>
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4.2.1.4 Add Immediate₁₄

A4

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<th>Extension</th>
</tr>
</thead>
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<tr>
<td>adds</td>
<td>r₁ = imm₁₄, r₃</td>
<td>8 2 0</td>
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</tr>
<tr>
<td>addp4</td>
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<td></td>
</tr>
</tbody>
</table>

4.2.1.5 Add Immediate₂₂

A5

<table>
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<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
</tr>
</thead>
<tbody>
<tr>
<td>addl</td>
<td>r₁ = imm₂₂, r₃</td>
<td>9</td>
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</table>

4.2.2 Integer Compare

The integer compare instructions are encoded within major opcodes C – E using a 2-bit opcode extension field (x₂) in bits 35:34 and three 1-bit opcode extension fields in bits 33 (tₐ), 36 (tₙ), and 12 (c), as shown in Table 4-10. The integer compare immediate instructions are encoded within major opcodes C – E using a 2-bit opcode extension field (x₂) in bits 35:34 and two 1-bit opcode extension fields in bits 33 (tₐ) and 12 (c), as shown in Table 4-11.
### Table 4-10. Integer Compare Opcode Extensions

<table>
<thead>
<tr>
<th>$x_2$ Bits 35:34</th>
<th>$t_b$ Bit 36</th>
<th>$t_a$ Bit 33</th>
<th>$c$ Bit 12</th>
<th>Opcode Bits 40:37</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>cmp.lt A6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>cmp.ltu A6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>cmp.eq A6</td>
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<tr>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>cmp.lt.unc A6</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0</td>
<td>cmp.ltu.unc A6</td>
</tr>
<tr>
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<td></td>
<td>1</td>
<td>cmp.eq.unc A6</td>
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<td>0</td>
<td>cmp.eq.and A6</td>
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<td>0</td>
<td>cmp.eq.or A6</td>
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<td></td>
<td>1</td>
<td>cmp.eq.or.andcm A6</td>
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<td>0</td>
<td>cmp.ne.and A6</td>
</tr>
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<td>cmp.ne.or A6</td>
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<td>cmp.gt.and A7</td>
</tr>
<tr>
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<td></td>
<td>1</td>
<td>cmp.gt.or A7</td>
</tr>
<tr>
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<td></td>
<td></td>
<td>1</td>
<td>cmp.gt.or.andcm A7</td>
</tr>
<tr>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>cmp.le.and A7</td>
</tr>
<tr>
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<td>cmp.le.or A7</td>
</tr>
<tr>
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<td></td>
<td>1</td>
<td>cmp.le.or.andcm A7</td>
</tr>
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<td>0</td>
<td>0</td>
<td>cmp4.lt A6</td>
</tr>
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<td></td>
<td></td>
<td>0</td>
<td>cmp4.ltu A6</td>
</tr>
<tr>
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<td></td>
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<td>cmp4.eq A6</td>
</tr>
<tr>
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<td>0</td>
<td>0</td>
<td>cmp4.lt.unc A6</td>
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<td>cmp4.ltu.unc A6</td>
</tr>
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<td>cmp4.eq.and A6</td>
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<td>cmp4.eq.or A6</td>
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<td>cmp4.ne.or A6</td>
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<td>0</td>
<td>cmp4.le.and A7</td>
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<td>cmp4.le.or A7</td>
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</table>

### Table 4-11. Integer Compare Immediate Opcode Extensions

<table>
<thead>
<tr>
<th>$x_2$ Bits 35:34</th>
<th>$t_b$ Bit 36</th>
<th>$t_a$ Bit 33</th>
<th>$c$ Bit 12</th>
<th>Opcode Bits 40:37</th>
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<tr>
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<td>cmp.lt – immg A8</td>
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<tr>
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<td></td>
<td>1</td>
<td>cmp.ltu – immg A8</td>
</tr>
<tr>
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<td>cmp.eq – immg A8</td>
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<td>0</td>
<td>0</td>
<td>cmp.lt.unc – immg A8</td>
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<td>cmp.eq.and – immg A8</td>
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<td>cmp.eq.or – immg A8</td>
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### 4.2.2.1 Integer Compare – Register-Register

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
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<tr>
<td><code>cmp.lt</code></td>
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Extension: 0x2 tb ta cp

$p1, p2 = r2, r3$
### Integer Compare to Zero – Register

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$p_1, p_2 = r_0, r_3$
4.2.2.3 Integer Compare – Immediate-Register

A8

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$P_1, P_2 = \text{imm}_8, r_3$

4.2.3 Multimedia

All multimedia ALU instructions are encoded within major opcode 8 using two 1-bit opcode extension fields in bits 36 ($z_a$) and 33 ($z_b$) and a 2-bit opcode extension field in bits 35:34 ($x_{2a}$) as shown in Table 4-12. The multimedia ALU instructions also have a 4-bit opcode extension field in bits 32:29 ($x_3$), and a 2-bit opcode extension field in bits 28:27 ($x_{2b}$) as shown in Table 4-13 on page 4-269.

Table 4-12. Multimedia ALU 2-bit+1-bit Opcode Extensions

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<tr>
<th>Opcode Bits 40:37</th>
<th>$x_{2a}$ Bits 35:34</th>
<th>$z_a$ Bit 36</th>
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Multimedia ALU Size 1 (Table 4-13)
Multimedia ALU Size 2 (Table 4-14)
Multimedia ALU Size 4 (Table 4-15)
Table 4-13. Multimedia ALU Size 1 4-bit+2-bit Opcode Extensions

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<th>x2a Bits 35:34</th>
<th>x2b Bits 32:29</th>
<th>x3a Bit 36</th>
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Table 4-14. Multimedia ALU Size 2 4-bit+2-bit Opcode Extensions

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A
B
C
D
E
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Volume 3: Instruction Formats
### 4.2.3.1 Multimedia ALU

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<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>pshladd2</td>
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<td>1</td>
</tr>
<tr>
<td>pshraad2</td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

Volume 3: Instruction Formats
4.3 I-Unit Instruction Encodings

4.3.1 Multimedia and Variable Shifts

All multimedia multiply/shift/max/min/mix/mux/pack/unpack and variable shift instructions are encoded within major opcode 7 using two 1-bit opcode extension fields in bits 36 (za) and 33 (zb) and a 1-bit reserved opcode extension in bit 32 (ve) as shown in Table 4-16. They also have a 2-bit opcode extension field in bits 35:34 (x2a) and a 2-bit field in bits 29:28 (x2b) and most have a 2-bit field in bits 31:30 (x2c) as shown in Table 4-17.

**Table 4-16. Multimedia and Variable Shift 1-bit Opcode Extensions**

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>za Bit 36</th>
<th>zb Bit 33</th>
<th>ve Bit 32</th>
</tr>
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<tbody>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>0</td>
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<td>0</td>
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**Table 4-17. Multimedia Opcode 7 Size 1 2-bit Opcode Extensions**

<table>
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<tr>
<th>Opcode Bits 40:37</th>
<th>za Bit 36</th>
<th>zb Bit 33</th>
<th>x2a Bits 35:34</th>
<th>x2b Bits 29:28</th>
<th>x2c Bits 31:30</th>
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</thead>
<tbody>
<tr>
<td>7</td>
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<td>0</td>
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### Table 4-18. Multimedia Opcode 7 Size 2 2-bit Opcode Extensions

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<th>$z_a$ Bit 36</th>
<th>$z_b$ Bit 33</th>
<th>$v_e$ Bit 32</th>
<th>$x_{2a}$ Bits 35:34</th>
<th>$x_{2b}$ Bits 32:29</th>
<th>$x_{2c}$ Bits 31:30</th>
</tr>
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<tbody>
<tr>
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<td>2</td>
<td>3</td>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>psr2.u – var I5</td>
<td>pshl2 – var I7</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pmpyshr2.u I1</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>psr2 – var I5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pmpyshr2 I1</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>pshr2 – fixed I6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>popcnt I9</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>3</td>
<td>pshr4.u – fixed I6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pmpy2.r I2</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>2</td>
<td>1</td>
<td>pack2.uss I2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td>unpack2.h I2</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>pack2.sss I2</td>
<td></td>
<td></td>
</tr>
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<td></td>
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<td></td>
<td>unpack2.l I2</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>3</td>
<td>1</td>
<td>pmin2 I2</td>
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</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>pmax2 I2</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pmpy2.l I2</td>
</tr>
<tr>
<td>8</td>
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<td>1</td>
<td>0</td>
<td>pshr2 – fixed I8</td>
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<td>mux2 I4</td>
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<td>2</td>
<td>2</td>
<td>pshr4 – fixed I6</td>
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</tr>
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<td></td>
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<td></td>
<td></td>
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<td>3</td>
<td>3</td>
<td>pshr4 – fixed I6</td>
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<td>pmpy4.s I2</td>
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### Table 4-19. Multimedia Opcode 7 Size 4 2-bit Opcode Extensions

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<th>$v_e$ Bit 32</th>
<th>$x_{2a}$ Bits 35:34</th>
<th>$x_{2b}$ Bits 32:29</th>
<th>$x_{2c}$ Bits 31:30</th>
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<tbody>
<tr>
<td>0</td>
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<td>0</td>
<td>0</td>
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<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>psr4.u – var I5</td>
<td>pshl4 – var I7</td>
<td></td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td>pmpyshr4.u I1</td>
</tr>
<tr>
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<td>0</td>
<td>1</td>
<td>3</td>
<td>psr4 – var I5</td>
<td></td>
<td></td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>pmpyshr4 I1</td>
</tr>
<tr>
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<td>0</td>
<td>2</td>
<td>1</td>
<td>psr4 – fixed I6</td>
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</tr>
<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>popcnt I9</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>pack4.uss I2</td>
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<td></td>
</tr>
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<td></td>
<td></td>
<td>unpack4.h I2</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>3</td>
<td>1</td>
<td>pack4.sss I2</td>
<td></td>
<td></td>
</tr>
<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>unpack4.l I2</td>
</tr>
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<td>0</td>
<td>3</td>
<td>2</td>
<td>pmin4 I2</td>
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<td></td>
</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>pmax4 I2</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>pshr4 – fixed I8</td>
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<td></td>
<td></td>
<td>pmpy4.s I2</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>pshr4 – fixed I8</td>
<td></td>
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</tr>
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<td></td>
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<td>pmpy4.r I2</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>3</td>
<td>3</td>
<td>pshr4 – fixed I8</td>
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<td></td>
</tr>
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<td></td>
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<td>pmpy4.s I2</td>
</tr>
</tbody>
</table>
Table 4-20. Variable Shift Opcode 7 2-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>za Bit 36</th>
<th>zb Bit 33</th>
<th>ve Bit 32</th>
<th>$x_{2a}$ Bits 35:34</th>
<th>$x_{2b}$ Bits 29:28</th>
<th>$x_{2c}$ Bits 31:30</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 1 1 0</td>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
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</tbody>
</table>

4.3.1.1 Multimedia Multiply and Shift

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<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>pmpyshr2</td>
<td>$r_f = r_2$, $r_3$, count 2</td>
<td>7</td>
<td>za zb ve $x_{2a}$ $x_{2b}$</td>
</tr>
<tr>
<td>pmpyshr2.u</td>
<td></td>
<td>7</td>
<td>0 1 0 0 0 3 1</td>
</tr>
</tbody>
</table>

Instruction Operands Opcode Extension

40 37 36 35 34 33 32 31 30 29 28 27 26 20 19 13 12 6 5 0

Instruction Operands Opcode Extension

40 37 36 35 34 33 32 31 30 29 28 27 26 20 19 13 12 6 5 0
### 4.3.1.2 Multimedia Multiply/Mix/Pack/Unpack

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<th>Extension</th>
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</thead>
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<tr>
<td>pmpy2.l</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mix1.r</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mix2.r</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mix4.r</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mix1.l</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mix2.l</td>
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<td>mix4.l</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pack2.uss</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pack2.sss</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pack4.sss</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>r1 = r2, r3</td>
<td></td>
<td>7</td>
<td>0 2 0</td>
</tr>
<tr>
<td>unpack1.h</td>
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<td></td>
</tr>
<tr>
<td>unpack2.h</td>
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<tr>
<td>unpack4.h</td>
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<tr>
<td>unpack1.l</td>
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<td>unpack2.l</td>
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<tr>
<td>unpack4.l</td>
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<td>pmin1.u</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>pmax1.u</td>
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<tr>
<td>pmin2</td>
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### 4.3.1.3 Multimedia Mux1

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<th>Extension</th>
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### 4.3.1.4 Multimedia Mux2

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<th>Extension</th>
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### 4.3.1.5 Shift Right – Variable

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<th>Extension</th>
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</thead>
<tbody>
<tr>
<td><code>pshr2</code></td>
<td></td>
<td><code>7</code></td>
<td><code>za zb ve x2a x2b x2c</code></td>
</tr>
<tr>
<td><code>pshr4</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>shr</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>pshr2.u</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
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### 4.3.1.6 Multimedia Shift Right – Fixed

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<th>Extension</th>
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<td></td>
<td><code>7</code></td>
<td><code>za zb ve x2a x2b x2c</code></td>
</tr>
<tr>
<td><code>pshr4</code></td>
<td></td>
<td></td>
<td></td>
</tr>
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### 4.3.1.7 Shift Left – Variable

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<th>Extension</th>
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<td><code>za zb ve x2a x2b x2c</code></td>
</tr>
<tr>
<td><code>pshl4</code></td>
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<td><code>shl</code></td>
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### 4.3.1.8 Multimedia Shift Left – Fixed

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<th>Extension</th>
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</thead>
<tbody>
<tr>
<td><code>pshl2</code></td>
<td></td>
<td><code>7</code></td>
<td><code>za zb ve x2a x2b x2c</code></td>
</tr>
<tr>
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4.3.1.9 Population Count

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<th>Opcode</th>
<th>Extension</th>
</tr>
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<tbody>
<tr>
<td>popcnt</td>
<td>z_a = z_b</td>
<td>7</td>
<td>0 1 0 1 1 2</td>
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</table>

4.3.2 Integer Shifts

The integer shift, test bit, and test NaT instructions are encoded within major opcode 5 using a 2-bit opcode extension field in bits 35:34 (x2) and a 1-bit opcode extension field in bit 33 (x). The extract and test bit instructions also have a 1-bit opcode extension field in bit 13 (y). Table 4-21 shows the test bit, extract, and shift right pair assignments.

Table 4-21. Integer Shift/Test Bit/Test NaT 2-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x2 Bits 35:34</th>
<th>x Bit 33</th>
<th>y Bit 13</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Most deposit instructions also have a 1-bit opcode extension field in bit 26 (y). Table 4-22 shows these assignments.

Table 4-22. Deposit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x2 Bits 35:34</th>
<th>x Bit 33</th>
<th>y Bit 26</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4.3.2.1 Shift Right Pair

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>shrp</td>
<td>r_f = r_2, r_3, count_6d</td>
<td>5</td>
<td>3 0</td>
</tr>
</tbody>
</table>

Volume 3: Instruction Formats
### 4.3.2.2 Extract

#### Instruction Operands Opcode Extension

| extr.u | $r_1 = r_3, pos_6, len_6$ | 5 | 1 | 0 |
| extr   |                          |   |   | 1 |

### 4.3.2.3 Zero and Deposit

#### Instruction Operands Opcode Extension

| dep.z  | $r_1 = r_2, pos_6, len_6$ | 5 | 1 | 1 |

### 4.3.2.4 Zero and Deposit Immediate

#### Instruction Operands Opcode Extension

| dep.z  | $r_1 = imm_8, pos_6, len_6$ | 5 | 1 | 1 | 1 |

### 4.3.2.5 Deposit Immediate

#### Instruction Operands Opcode Extension

| dep    | $r_1 = imm_1, r_3, pos_6, len_6$ | 5 | 3 | 1 |

### 4.3.2.6 Deposit

#### Instruction Operands Opcode

| dep    | $r_1 = r_2, r_3, pos_6, len_4$ | 4 |   |   |
4.3.3 Test Bit

All test bit instructions are encoded within major opcode 5 using a 2-bit opcode extension field in bits 35:34 ($x_2$) plus four 1-bit opcode extension fields in bits 33 ($t_a$), 36 ($t_b$), 12 (c), and 19 (y). Table 4-23 summarizes these assignments.

Table 4-23. Test Bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>$x_2$ Bits 35:34</th>
<th>$t_a$ Bit 33</th>
<th>$t_b$ Bit 36</th>
<th>c Bit 12</th>
<th>y Bit 13</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>0</td>
<td></td>
<td>1</td>
</tr>
</tbody>
</table>

4.3.3.1 Test Bit

Instruction Operands Opcode Extension

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>$x_2$</th>
<th>$t_a$</th>
<th>$t_b$</th>
<th>y</th>
<th>c</th>
</tr>
</thead>
<tbody>
<tr>
<td>tbit.z</td>
<td></td>
<td>5</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>tbit.z.unc</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tbit.z.and</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tbit.nz.and</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tbit.z.or</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tbit.nz.or</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tbit.z.or.andcm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>tbit.nz.or.andcm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$p_1, p_2 = r_3, pos_6$
4.3.3.2 Test NaT

The miscellaneous I-unit instructions are encoded in major opcode 0 using a 3-bit opcode extension field ($x_3$) in bits 35:33. Some also have a 6-bit opcode extension field ($x_6$) in bits 32:27. Table 4-24 shows the 3-bit assignments and Table 4-25 summarizes the 6-bit assignments.

Table 4-24. Misc I-Unit 3-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>$tnat.z$</td>
<td></td>
<td>5</td>
<td>x2 t3 t0 y c</td>
</tr>
<tr>
<td>$tnat.z.unc$</td>
<td></td>
<td></td>
<td>0 0 0 1 0 0</td>
</tr>
<tr>
<td>$tnat.z.and$</td>
<td></td>
<td></td>
<td>0 1 1 0 1 1</td>
</tr>
<tr>
<td>$tnat.nz.and$</td>
<td></td>
<td></td>
<td>0 0 0 1 1 1</td>
</tr>
<tr>
<td>$tnat.z.or$</td>
<td></td>
<td></td>
<td>1 1 0 0 0 1</td>
</tr>
<tr>
<td>$tnat.nz.or$</td>
<td></td>
<td></td>
<td>1 1 1 0 0 1</td>
</tr>
<tr>
<td>$tnat.z.or.andcm$</td>
<td></td>
<td></td>
<td>1 1 0 0 1 1</td>
</tr>
<tr>
<td>$tnat.nz.or.andcm$</td>
<td></td>
<td></td>
<td>1 1 1 0 1 1</td>
</tr>
</tbody>
</table>

4.3.4 Miscellaneous I-Unit Instructions

The miscellaneous I-unit instructions are encoded in major opcode 0 using a 3-bit opcode extension field ($x_3$) in bits 35:33. Some also have a 6-bit opcode extension field ($x_6$) in bits 32:27. Table 4-24 shows the 3-bit assignments and Table 4-25 summarizes the 6-bit assignments.
4.3.4.1 Nop/Hint (I-Unit)

I-unit nop and hint instructions are encoded within major opcode 0 using a 3-bit opcode extension field in bits 35:33 ($x_3$), a 6-bit opcode extension field in bits 32:27 ($x_6$), and a 1-bit opcode extension field in bit 26 ($y$), as shown in Table 4-26.

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>$x_3$ Bits 35:33</th>
<th>$x_6$ Bits 32:27</th>
<th>$y$ Bit 26</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>zxt1 I29</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov from ip I25</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>zxt2 I29</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov from b I22</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>zxt4 I29</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov.i from ar I28</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>sxt1 I29</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>sxt2 I29</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>sxt4 I29</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>czx1.i I29</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>czx2.i I29</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>mov.i to ar – imm8 I27</td>
<td>mov.i to ar I26</td>
</tr>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td>czx1.r I29</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td></td>
<td>czx2.r I29</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4-25. Misc I-Unit 6-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>$x_3$ Bits 35:33</th>
<th>$x_6$ Bits 32:27</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>zxt1 I29</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov from ip I25</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>zxt2 I29</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov from b I22</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>zxt4 I29</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov.i from ar I28</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>sxt1 I29</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>sxt2 I29</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>sxt4 I29</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>czx1.i I29</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>czx2.i I29</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>mov.i to ar – imm8 I27</td>
</tr>
<tr>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td>czx1.r I29</td>
</tr>
<tr>
<td>D</td>
<td></td>
<td>czx2.r I29</td>
</tr>
<tr>
<td>E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4-26. Misc I-Unit 1-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>nop.i</td>
<td></td>
<td>x_3</td>
<td>x_6</td>
</tr>
<tr>
<td>hint.i</td>
<td>imm_{2f}</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>
4.3.4.2  Break (I-Unit)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>break.i</td>
<td>imm_{21}</td>
<td>0</td>
<td>0 0</td>
</tr>
</tbody>
</table>

4.3.4.3  Integer Speculation Check (I-Unit)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>chk.s.i</td>
<td>r_{2}, target_{25}</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

4.3.5  GR/BR Moves

The GR/BR move instructions are encoded in major opcode 0. See “Miscellaneous I-Unit Instructions” on page 280 for a summary of the opcode extensions. The mov to BR instruction uses a 2-bit “whether” prediction hint field in bits 21:20 (wh) as shown in Table 4-27.

Table 4-27. Move to BR Whether Hint Completer

<table>
<thead>
<tr>
<th>wh Bits 21:20</th>
<th>mwh</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>splk</td>
</tr>
<tr>
<td>1</td>
<td>none</td>
</tr>
<tr>
<td>2</td>
<td>dptk</td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

The mov to BR instruction also uses a 1-bit opcode extension field (x) in bit 22 to distinguish the return form from the normal form, and a 1-bit hint extension in bit 23 (ih) (see Table 4-56 on page 4-318).

4.3.5.1  Move to BR

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov.mwh.ih</td>
<td></td>
<td>b_{1} = r_{2}, tag_{13}</td>
<td>0</td>
</tr>
</tbody>
</table>
4.3.5.2 Move from BR

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov</td>
<td>( r_1 = b_2 )</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

4.3.6 GR/Predicate/IP Moves

The GR/Predicate/IP move instructions are encoded in major opcode 0. See “Miscellaneous I-Unit Instructions” on page 280 for a summary of the opcode extensions.

4.3.6.1 Move to Predicates – Register

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov</td>
<td>( pr = r_2, mask_{17} )</td>
<td>0</td>
<td>3</td>
</tr>
</tbody>
</table>

4.3.6.2 Move to Predicates – Immediate\(_{44}\)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov</td>
<td>( pr.rot = imm_{44} )</td>
<td>0</td>
<td>2</td>
</tr>
</tbody>
</table>

4.3.6.3 Move from Predicates/IP

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov</td>
<td>( r_1 = ip ) ( r_1 = pr )</td>
<td>0</td>
<td>30</td>
</tr>
</tbody>
</table>
4.3.7 GR/AR Moves (I-Unit)

The I-Unit GR/AR move instructions are encoded in major opcode 0. (Some ARs are accessed using system/memory management instructions on the M-unit. See “GR/AR Moves (M-Unit)” on page 4-306.) See “Miscellaneous I-Unit Instructions” on page 280 for a summary of the I-Unit GR/AR opcode extensions.

4.3.7.1 Move to AR – Register (I-Unit)

4.3.7.2 Move to AR – Immediate8 (I-Unit)

4.3.7.3 Move from AR (I-Unit)
4.3.8 Sign/Zero Extend/Compute Zero Index

All load and store instructions are encoded within major opcodes 4, 5, 6, and 7 using a 6-bit opcode extension field in bits 35:30 ($x_6$). Instructions in major opcode 4 (integer load/store, semaphores, and get FR) use two 1-bit opcode extension fields in bit 36 (m) and bit 27 (x) as shown in Table 4-28. Instructions in major opcode 6 (floating-point load/store, load pair, and set FR) use two 1-bit opcode extension fields in bit 36 (m) and bit 27 (x) as shown in Table 4-29.

### Table 4-28. Integer Load/Store/Semaphore/Get FR 1-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>m Bit 36</th>
<th>x Bit 27</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>Load/Store (Table 4-30)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>Semaphore/get FR (Table 4-33)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>Load +Reg (Table 4-31)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

### Table 4-29. Floating-point Load/Store/Load Pair/Set FR 1-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>m Bit 36</th>
<th>x Bit 27</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>0</td>
<td>0</td>
<td>FP Load/Store (Table 4-34)</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>1</td>
<td>FP Load Pair/set FR (Table 4-37)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td>FP Load +Reg (Table 4-35)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>FP Load Pair +Imm (Table 4-38)</td>
</tr>
</tbody>
</table>

4.4 M-Unit Instruction Encodings

4.4.1 Loads and Stores
The integer load/store opcode extensions are summarized in Table 4-30 on page 4-286, Table 4-31 on page 4-287, and Table 4-32 on page 4-287, and the semaphore and get FR opcode extensions in Table 4-33 on page 4-288. The floating-point load/store opcode extensions are summarized in Table 4-34 on page 4-288, Table 4-35 on page 4-289, and Table 4-36 on page 4-289, the floating-point load pair and set FR opcode extensions in Table 4-37 on page 4-290 and Table 4-38 on page 4-290.

Table 4-30. Integer Load/Store Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>m Bit 36</th>
<th>x Bit 27</th>
<th>Bits 35:32</th>
<th>Bits 31:30</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>ld1 M1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
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Table 4-31. Integer Load +Reg Opcode Extensions

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Table 4-32. Integer Load/Store +Imm Opcode Extensions

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### Table 4-33. Semaphore/Get FR/16-Byte Opcode Extensions

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### Table 4-34. Floating-point Load/Store/Lfetch Opcode Extensions

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Table 4-35. Floating-point Load/Lfetch +Reg Opcode Extensions

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Table 4-36. Floating-point Load/Store/Lfetch +Imm Opcode Extensions

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The load and store instructions all have a 2-bit opcode extension field in bits 29:28 (hint) which encodes locality hint information. Table 4-39 and Table 4-40 summarize these assignments.
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### 4.4.1.1 Integer Load

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*See Table 4-39 on page 4-291*
### 4.4.1.2 Integer Load – Increment by Register

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### 4.4.1.3 Integer Load – Increment by Immediate

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- \( r_1 = [r_3], \text{imm}_9 \)
- See Table 4-39 on page 4-291
### 4.4.1.4 Integer Store

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### 4.4.1.5 Integer Store – Increment by Immediate

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### 4.4.1.6 Floating-point Load

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</table>

Example:

`ldfs.a.ldhint` with `f1 = [r3]` produces the following encoding:

- Instruction: `ldfs.a.ldhint`
- Operands: `m`, `x`, `x6`, `hint`
- Opcode: 6
- Extension: 00

See Table 4-39 on page 4-291 for more information.
### 4.4.1.7 Floating-point Load – Increment by Register

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<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>ldfs.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfd.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldf8.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfe.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfs.s.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfd.s.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldf8.s.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfe.s.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfs.a.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfd.a.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldf8.a.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfe.a.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfs.sa.ldhint</code></td>
<td>f₁ = [r₃], r₂</td>
<td>6  1  0</td>
<td></td>
</tr>
<tr>
<td><code>ldfd.sa.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldf8.sa.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfe.sa.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldf.fill.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfs.c.clr.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfd.c.clr.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldf8.c.clr.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfe.c.clr.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfs.c.nc.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfd.c.nc.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldf8.c.nc.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><code>ldfe.c.nc.ldhint</code></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

See Table 4-39 on page 4-291.
### 4.4.1.8 Floating-point Load – Increment by Immediate

- **M8**
  - Instruction Operands Opcode Extension
  - `ldfs.ldhint` | `r3` | 02
  - `ldfd.ldhint` | `r3` | 03
  - `ldf8.ldhint` | `r3` | 01
  - `ldfe.ldhint` | `r3` | 00
  - `ldfs.s.ldhint` | `r3` | 06
  - `ldfd.s.ldhint` | `r3` | 07
  - `ldf8.s.ldhint` | `r3` | 05
  - `ldfe.s.ldhint` | `r3` | 04
  - `ldfs.a.ldhint` | `r3` | 0A
  - `ldfd.a.ldhint` | `r3` | 0B
  - `ldf8.a.ldhint` | `r3` | 09
  - `ldfe.a.ldhint` | `r3` | 08
  - `ldfs.sa.ldhint` | `r3`, `imm9` | 0E
  - `ldfd.sa.ldhint` | `r3`, `imm9` | 0F
  - `ldf8.sa.ldhint` | `r3`, `imm9` | 0D
  - `ldfe.sa.ldhint` | `r3`, `imm9` | 0C
  - `ldf.fill.ldhint` | | 1B
  - `ldfs.c.clr.ldhint` | | 22
  - `ldfd.c.clr.ldhint` | | 23
  - `ldf8.c.clr.ldhint` | | 21
  - `ldfe.c.clr.ldhint` | | 20
  - `ldfs.c.nc.ldhint` | | 26
  - `ldfd.c.nc.ldhint` | | 27
  - `ldf8.c.nc.ldhint` | | 25
  - `ldfe.c.nc.ldhint` | | 24

### 4.4.1.9 Floating-point Store

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>stfs.sthint</code></td>
<td><code>f2</code></td>
<td>6</td>
<td><code>x6</code></td>
</tr>
<tr>
<td><code>stfd.sthint</code></td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td><code>stf8.sthint</code></td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td><code>stfe.sthint</code></td>
<td></td>
<td>0</td>
<td></td>
</tr>
<tr>
<td><code>stf.spill.sthint</code></td>
<td></td>
<td>3B</td>
<td></td>
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</tbody>
</table>
### 4.4.1.10 Floating-point Store – Increment by Immediate

<table>
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<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>stfs.sthint</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>std.sthint</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>stfd.sthint</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>stfe.sthint</td>
<td>[r₃] = f₂, imm₉</td>
<td>7</td>
<td></td>
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<tr>
<td>stf.spill.sthint</td>
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<td></td>
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</table>

M10

<table>
<thead>
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<th>Extension</th>
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</thead>
<tbody>
<tr>
<td>ldfps.ldhint</td>
<td></td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>ldpd.ldhint</td>
<td></td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>ldfp8.ldhint</td>
<td></td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>ldpd.s.ldhint</td>
<td></td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>ldpd.a.ldhint</td>
<td></td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>ldpd.sa.ldhint</td>
<td></td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>ldpd.c.clr.ldhint</td>
<td></td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>ldpd.c.clr.ldhint</td>
<td></td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>ldpd.c.nc.ldhint</td>
<td></td>
<td>6</td>
<td>2</td>
</tr>
</tbody>
</table>

### 4.4.1.11 Floating-point Load Pair

<table>
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<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
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</thead>
<tbody>
<tr>
<td>ldfps.ldhint</td>
<td></td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>ldpd.ldhint</td>
<td></td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>ldfp8.ldhint</td>
<td></td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>ldpd.s.ldhint</td>
<td></td>
<td>6</td>
<td>6</td>
</tr>
<tr>
<td>ldpd.a.ldhint</td>
<td></td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>ldpd.sa.ldhint</td>
<td></td>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>ldpd.c.clr.ldhint</td>
<td></td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>ldpd.c.clr.ldhint</td>
<td></td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>ldpd.c.nc.ldhint</td>
<td></td>
<td>6</td>
<td>2</td>
</tr>
</tbody>
</table>

M11

See Table 4-39 on page 4-291.
4.4.1.12 Floating-point Load Pair – Increment by Immediate

The line prefetch instructions are encoded in major opcodes 6 and 7 along with the floating-point load/store instructions. See “Loads and Stores” on page 285 for a summary of the opcode extensions.

The line prefetch instructions all have a 2-bit opcode extension field in bits 29:28 (hint) which encodes locality hint information as shown in Table 4-41.

### Table 4-41. Line Prefetch Hint Completer

<table>
<thead>
<tr>
<th>hint Bits 29:28</th>
<th>hint</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>none</td>
</tr>
<tr>
<td>1</td>
<td>nt1</td>
</tr>
<tr>
<td>2</td>
<td>nt2</td>
</tr>
<tr>
<td>3</td>
<td>nta</td>
</tr>
</tbody>
</table>
## 4.4.2.1 Line Prefetch

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>m</td>
<td>x&lt;sub&gt;6&lt;/sub&gt;</td>
<td>hint</td>
<td>x</td>
</tr>
</tbody>
</table>

### Example

Instruction: lfetch.excl./fhint

Operands: [r<sub>3</sub>]

Opcode: 6

Extension: 0, 0, 2C, 2D, 2E, 2F

## 4.4.2.2 Line Prefetch – Increment by Register

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>m</td>
<td>x&lt;sub&gt;6&lt;/sub&gt;</td>
<td>hint</td>
<td>x</td>
</tr>
</tbody>
</table>

### Example

Instruction: lfetch.excl./fhint

Operands: [r<sub>3</sub>, r<sub>2</sub>]

Opcode: 6

Extension: 0, 0, 2C, 2D, 2E, 2F

## 4.4.2.3 Line Prefetch – Increment by Immediate

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>m</td>
<td>x&lt;sub&gt;6&lt;/sub&gt;</td>
<td>hint</td>
<td>i</td>
</tr>
</tbody>
</table>

### Example

Instruction: lfetch.excl./fhint

Operands: [r<sub>3</sub>, imm<sub>7b</sub>]

Opcode: 7

Extension: 0, 0, 2C, 2D, 2E, 2F
4.4.3 Semaphores

The semaphore instructions are encoded in major opcode 4 along with the integer load/store instructions. See “Loads and Stores” on page 285 for a summary of the opcode extensions.

### 4.4.3.1 Exchange/Compare and Exchange

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>cmpxchg1.acq.ldhint</td>
<td></td>
<td>4</td>
<td>00</td>
</tr>
<tr>
<td>cmpxchg2.acq.ldhint</td>
<td></td>
<td>4</td>
<td>01</td>
</tr>
<tr>
<td>cmpxchg4.acq.ldhint</td>
<td></td>
<td>4</td>
<td>02</td>
</tr>
<tr>
<td>cmpxchg8.acq.ldhint</td>
<td></td>
<td>4</td>
<td>03</td>
</tr>
<tr>
<td>cmpxchg1.rel.ldhint</td>
<td>( r_j = [r_3], r_2, \text{ar.ccv} )</td>
<td>4 ( \text{See Table 4-39 on page 4-291} )</td>
<td>04</td>
</tr>
<tr>
<td>cmpxchg2.rel.ldhint</td>
<td></td>
<td>4</td>
<td>05</td>
</tr>
<tr>
<td>cmpxchg4.rel.ldhint</td>
<td></td>
<td>4</td>
<td>06</td>
</tr>
<tr>
<td>cmpxchg8.rel.ldhint</td>
<td></td>
<td>4</td>
<td>07</td>
</tr>
<tr>
<td>cmp8xchg16.acq.ldhint</td>
<td></td>
<td>4</td>
<td>20</td>
</tr>
<tr>
<td>cmp8xchg16.rel.ldhint</td>
<td></td>
<td>4</td>
<td>24</td>
</tr>
<tr>
<td>xchg1.ldhint</td>
<td></td>
<td>4</td>
<td>08</td>
</tr>
<tr>
<td>xchg2.ldhint</td>
<td></td>
<td>4</td>
<td>09</td>
</tr>
<tr>
<td>xchg4.ldhint</td>
<td></td>
<td>4</td>
<td>0A</td>
</tr>
<tr>
<td>xchg8.ldhint</td>
<td></td>
<td>4</td>
<td>0B</td>
</tr>
</tbody>
</table>

### 4.4.3.2 Fetch and Add – Immediate

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fetchadd4.acq.ldhint</td>
<td></td>
<td>4</td>
<td>12</td>
</tr>
<tr>
<td>fetchadd8.acq.ldhint</td>
<td></td>
<td>4</td>
<td>13</td>
</tr>
<tr>
<td>fetchadd4.rel.ldhint</td>
<td>( r_j = [r_3], \text{inc}_3 )</td>
<td>4 ( \text{See Table 4-39 on page 4-291} )</td>
<td>16</td>
</tr>
<tr>
<td>fetchadd8.rel.ldhint</td>
<td></td>
<td>4</td>
<td>17</td>
</tr>
</tbody>
</table>
4.4.4 Set/Get FR

The set FR instructions are encoded in major opcode 6 along with the floating-point load/store instructions. The get FR instructions are encoded in major opcode 4 along with the integer load/store instructions. See “Loads and Stores” on page 285 for a summary of the opcode extensions.

4.4.4.1 Set FR

4.4.4.2 Get FR

4.4.5 Speculation and Advanced Load Checks

The speculation and advanced load check instructions are encoded in major opcodes 0 and 1 along with the system/memory management instructions. See “System/Memory Management” on page 308 for a summary of the opcode extensions.

4.4.5.1 Integer Speculation Check (M-Unit)
4.4.5.2 Floating-point Speculation Check

### Instruction Format

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>chk.s</code></td>
<td><code>f2, target25</code></td>
<td>1</td>
<td><code>x3</code></td>
</tr>
</tbody>
</table>

4.4.5.3 Integer Advanced Load Check

### Instruction Format

<table>
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<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>chk.a.nc</code></td>
<td><code>r1, target25</code></td>
<td>0</td>
<td><code>x3</code></td>
</tr>
<tr>
<td><code>chk.a.clr</code></td>
<td><code>r1, target25</code></td>
<td>0</td>
<td><code>x3</code></td>
</tr>
</tbody>
</table>

4.4.5.4 Floating-point Advanced Load Check

### Instruction Format

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<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>chk.a.nc</code></td>
<td><code>f1, target25</code></td>
<td>0</td>
<td><code>x3</code></td>
</tr>
<tr>
<td><code>chk.a.clr</code></td>
<td><code>f1, target25</code></td>
<td>0</td>
<td><code>x3</code></td>
</tr>
</tbody>
</table>

4.4.6 Cache/Synchronization/RSE/ALAT

The cache/synchronization/RSE/ALAT instructions are encoded in major opcode 0 along with the memory management instructions. See “System/Memory Management” on page 308 for a summary of the opcode extensions.
### 4.4.6.1 Sync/Fence/Serialize/ALAT Control

<table>
<thead>
<tr>
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<th>Opcode</th>
<th>Extension</th>
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<tr>
<td>invala</td>
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</tr>
<tr>
<td>fwb</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>mf</td>
<td>0</td>
<td>2</td>
</tr>
<tr>
<td>mf.a</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>srlz.d</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>srlz.i</td>
<td>0</td>
<td>3</td>
</tr>
<tr>
<td>sync.i</td>
<td>0</td>
<td>3</td>
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</table>

### 4.4.6.2 RSE Control

<table>
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<td>flushrs</td>
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<td>C</td>
</tr>
<tr>
<td>loadrs</td>
<td>0</td>
<td>A</td>
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</table>

### 4.4.6.3 Integer ALAT Entry Invalidate

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<th>Opcode</th>
<th>Extension</th>
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</thead>
<tbody>
<tr>
<td>invala.e</td>
<td>r1</td>
<td>0</td>
<td>2</td>
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### 4.4.6.4 Floating-point ALAT Entry Invalidate

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<tr>
<td>invala.e</td>
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</table>
4.4.6.5 Flush Cache

<table>
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<td>r3</td>
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<td></td>
<td>23</td>
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<tr>
<td></td>
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<td>24</td>
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<tr>
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<tr>
<td></td>
<td></td>
<td>26</td>
<td></td>
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<tr>
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<td></td>
<td>27</td>
<td></td>
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<tr>
<td></td>
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<td></td>
<td>30</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>31</td>
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<tr>
<td></td>
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<td>32</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
<td></td>
</tr>
</tbody>
</table>

4.4.7 GR/AR Moves (M-Unit)

The M-Unit GR/AR move instructions are encoded in major opcode 0 along with the system/memory management instructions. (Some ARs are accessed using system control instructions on the I-unit. See “GR/AR Moves (I-Unit)” on page 4-284.) See “System/Memory Management” on page 308 for a summary of the M-Unit GR/AR opcode extensions.

4.4.7.1 Move to AR – Register (M-Unit)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ar3</td>
<td>r2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>x3</td>
<td>x6</td>
<td>x</td>
</tr>
</tbody>
</table>

4.4.7.2 Move to AR – Immediate8 (M-Unit)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>ar3</td>
<td>imm8</td>
<td></td>
</tr>
<tr>
<td></td>
<td>x3</td>
<td>x4</td>
<td>x2</td>
</tr>
</tbody>
</table>

4.4.7.3 Move from AR (M-Unit)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>rj</td>
<td>ar3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>x3</td>
<td>x6</td>
<td>x</td>
</tr>
</tbody>
</table>
4.4.8 **GR/CR Moves**

The GR/CR move instructions are encoded in major opcode 0 along with the system/memory management instructions. See “System/Memory Management” on page 308 for a summary of the opcode extensions.

4.4.8.1 **Move to CR**

```plaintext
M32
```

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov p</td>
<td>cr3 = r2</td>
<td>1</td>
<td>0 2C</td>
</tr>
</tbody>
</table>

4.4.8.2 **Move from CR**

```plaintext
M33
```

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov p</td>
<td>r1 = cr3</td>
<td>1</td>
<td>0 24</td>
</tr>
</tbody>
</table>

4.4.9 **Miscellaneous M-Unit Instructions**

The miscellaneous M-unit instructions are encoded in major opcode 0 along with the system/memory management instructions. See “System/Memory Management” on page 308 for a summary of the opcode extensions.

4.4.9.1 **Allocate Register Stack Frame**

```plaintext
M34
```

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>alloc</td>
<td>r1 = ar.pfs, i, l, o, r</td>
<td>1</td>
<td>6</td>
</tr>
</tbody>
</table>

**Note:** The three immediates in the instruction encoding are formed from the operands as follows:

- sof = i + l + o
- sol = i + l
- sor = r >> 3
4.4.9.2 Move to PSR

M35

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov[^]p</td>
<td>psr.l = r2</td>
<td>1</td>
<td>0 2D</td>
</tr>
<tr>
<td>mov</td>
<td>psr.um = r2</td>
<td>1</td>
<td>0 29</td>
</tr>
</tbody>
</table>

4.4.9.3 Move from PSR

M36

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov[^]p</td>
<td>r1 = psr</td>
<td>1</td>
<td>0 25</td>
</tr>
<tr>
<td>mov</td>
<td>r1 = psr.um</td>
<td>1</td>
<td>0 21</td>
</tr>
</tbody>
</table>

4.4.9.4 Break (M-Unit)

M37

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>break.m</td>
<td>imm21</td>
<td>0</td>
<td>0 0 0 0</td>
</tr>
</tbody>
</table>

4.4.10 System/Memory Management

All system/memory management instructions are encoded within major opcodes 0 and 1 using a 3-bit opcode extension field (x3) in bits 35:33. Some instructions also have a 4-bit opcode extension field (x4) in bits 30:27, or a 6-bit opcode extension field (x6) in bits 32:27. Most of the instructions having a 4-bit opcode extension field also have a 2-bit extension field (x2) in bits 32:31. Table 4-42 shows the 3-bit assignments for opcode 0, Table 4-43 summarizes the 4-bit+2-bit assignments for opcode 0, Table 4-44 shows the 3-bit assignments for opcode 1, and Table 4-45 summarizes the 6-bit assignments for opcode 1.
Table 4-42. Opcode 0 System/Memory Management 3-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>X3 Bits 35:33</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>System/Memory Management 4-bit+2-bit Ext (Table 4-43)</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>chk.a.nc – int M22</td>
</tr>
<tr>
<td>5</td>
<td>chk.a.clr – int M22</td>
</tr>
<tr>
<td>6</td>
<td>chk.a.nc – fp M23</td>
</tr>
<tr>
<td>7</td>
<td>chk.a.clr – fp M23</td>
</tr>
</tbody>
</table>

Table 4-43. Opcode 0 System/Memory Management 4-bit+2-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>X3 Bits 35:33</th>
<th>X4 Bits 30:27</th>
<th>X2 Bits 32:31</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>break.m M37</td>
<td>invala M24</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1-bit Ext (Table 4-46)</td>
<td>invala.e – int M26</td>
</tr>
<tr>
<td>2</td>
<td>2</td>
<td>invala.e – fp M27</td>
<td>mf.a M24</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>4</td>
<td></td>
<td>sum M44</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
<td></td>
<td>rum M44</td>
</tr>
<tr>
<td>6</td>
<td>6</td>
<td></td>
<td>ssm M44</td>
</tr>
<tr>
<td>7</td>
<td>7</td>
<td></td>
<td>rsm M44</td>
</tr>
<tr>
<td>8</td>
<td>8</td>
<td></td>
<td>mov.m to ar – imm8 M30</td>
</tr>
<tr>
<td>9</td>
<td>9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td>10</td>
<td>loadrs M25</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td>12</td>
<td>flushrs M25</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>13</td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>15</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 4-44. Opcode 1 System/Memory Management 3-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>X3 Bits 35:33</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>System/Memory Management 6-bit Ext (Table 4-45)</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
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<td></td>
</tr>
<tr>
<td>6</td>
<td>alloc M34</td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>
4.4.10.1 Probe – Register

Table 4-45. Opcode 1 System/Memory Management 6-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x3 Bits 35:33</th>
<th>x6 Bits 30:27</th>
<th>Bits 26:19</th>
<th>Bits 18:12</th>
<th>Bits 11:4</th>
<th>Bits 3:0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to rr M42</td>
<td>mov from rr M43</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to dbr M42</td>
<td>mov from dbr M43</td>
<td>mov from psr.um M36</td>
<td>probe.rw.fault – imm M40</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to ibr M42</td>
<td>mov from ibr M43</td>
<td>mov from ar M31</td>
<td>probe.r.fault – imm M40</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to pkr M42</td>
<td>mov from pkr M43</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to pnc M42</td>
<td>mov from pnc M43</td>
<td>mov from M33</td>
<td>ptc.e M47</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to pmd M42</td>
<td>mov from pmd M43</td>
<td>mov from psr M36</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to ibr M42</td>
<td>mov from ibr M43</td>
<td>mov from ar M31</td>
<td>probe.r.fault – imm M40</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to pkr M42</td>
<td>mov from pkr M43</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to pnc M42</td>
<td>mov from pnc M43</td>
<td>mov from M33</td>
<td>ptc.e M47</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to pmd M42</td>
<td>mov from pmd M43</td>
<td>mov from psr M36</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov from cpuid M43</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.r – imm M39</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>probe.w – imm M39</td>
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<td>mov to psr.um M35</td>
<td>probe.w M38</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>pltc.g M45</td>
<td>pltc.m M45</td>
<td>ttag M46</td>
<td>mov.m to ar M29</td>
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<td></td>
<td></td>
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<tr>
<td>pltc.ga M45</td>
<td>ttag M46</td>
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<tr>
<td>ptr.d M45</td>
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<tr>
<td>ptr.i M45</td>
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<tr>
<td>itr.d M42</td>
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</tr>
<tr>
<td>itr.i M42</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.r – imm M39</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.w – imm M39</td>
<td></td>
<td>mov to psr.um M35</td>
<td>probe.w M38</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov to cr M32</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mov from cpuid M43</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.r – imm M39</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.w – imm M39</td>
<td></td>
<td>mov to psr.um M35</td>
<td>probe.w M38</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>probe.r</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.w</td>
<td>R1 = R3, R2</td>
<td>1</td>
<td>0, 38</td>
</tr>
</tbody>
</table>

4.4.10.2 Probe – Immediate2

Table 4-45. Opcode 1 System/Memory Management 6-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x3 Bits 35:33</th>
<th>x6 Bits 30:27</th>
<th>Bits 26:19</th>
<th>Bits 18:12</th>
<th>Bits 11:4</th>
<th>Bits 3:0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.r</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.w</td>
<td>R1 = R3, imm M2</td>
<td>1</td>
<td>0, 18</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>probe.r</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.w</td>
<td>R1 = R3, imm M2</td>
<td>1</td>
<td>0, 19</td>
</tr>
</tbody>
</table>
### 4.4.10.3  Probe Fault – Immediate

**M40**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>probe.rw.fault</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.r.fault</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.w.fault</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>probe.rw.fault</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.r.fault</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.w.fault</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>probe.rw.fault</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.r.fault</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>probe.w.fault</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 4.4.10.4  Translation Cache Insert

**M41**

<table>
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<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>itc.d[iP]</td>
<td></td>
<td>1</td>
<td>2E</td>
</tr>
<tr>
<td>itc.i[iP]</td>
<td></td>
<td>1</td>
<td>2F</td>
</tr>
</tbody>
</table>

### 4.4.10.5  Move to Indirect Register/Translation Register Insert

**M42**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>movP</td>
<td></td>
<td>1</td>
<td>00</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>01</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>02</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>03</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>04</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>05</td>
</tr>
<tr>
<td>itr.d P</td>
<td></td>
<td>1</td>
<td>0E</td>
</tr>
<tr>
<td>itr.i P</td>
<td></td>
<td>1</td>
<td>0F</td>
</tr>
</tbody>
</table>
### 4.4.10.6 Move from Indirect Register

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>mov&lt;sup&gt;P&lt;/sup&gt;</td>
<td>( r_1 = r[r_3] )</td>
<td>10</td>
<td>( x_3 )</td>
</tr>
</tbody>
</table>
| | \( r_1 = 
\) | 11 | \( x_3 \) |
| | \( r_1 = dbr[r_3] \) | 12 | \( x_3 \) |
| | \( r_1 = ibr[r_3] \) | 13 | \( x_3 \) |
| | \( r_1 = pk[r_3] \) | 14 | \( x_3 \) |
| | \( r_1 = pmc[r_3] \) | 15 | \( x_3 \) |
| | \( r_1 = pmid[r_3] \) | 17 | \( x_3 \) |

### 4.4.10.7 Set/Reset User/System Mask

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>sum</td>
<td>( imm_{24} )</td>
<td>4</td>
<td>( x_3 )</td>
</tr>
<tr>
<td>rum</td>
<td>( imm_{24} )</td>
<td>5</td>
<td>( x_3 )</td>
</tr>
<tr>
<td>ssm&lt;sup&gt;P&lt;/sup&gt;</td>
<td>( imm_{24} )</td>
<td>6</td>
<td>( x_3 )</td>
</tr>
<tr>
<td>rsm&lt;sup&gt;P&lt;/sup&gt;</td>
<td>( imm_{24} )</td>
<td>7</td>
<td>( x_3 )</td>
</tr>
</tbody>
</table>

### 4.4.10.8 Translation Purge

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>ptc.&lt;sup&gt;P&lt;/sup&gt;</td>
<td>( r_3, r_2 )</td>
<td>09</td>
<td>( x_3 )</td>
</tr>
<tr>
<td>ptc.&lt;sup&gt;G&lt;/sup&gt;</td>
<td>( r_3, r_2 )</td>
<td>0A</td>
<td>( x_3 )</td>
</tr>
<tr>
<td>ptc.&lt;sup&gt;GA&lt;/sup&gt;</td>
<td>( r_3, r_2 )</td>
<td>0B</td>
<td>( x_3 )</td>
</tr>
<tr>
<td>ptr.&lt;sup&gt;D&lt;/sup&gt;</td>
<td>( r_3, r_2 )</td>
<td>0C</td>
<td>( x_3 )</td>
</tr>
<tr>
<td>ptr.&lt;sup&gt;I&lt;/sup&gt;</td>
<td>( r_3, r_2 )</td>
<td>0D</td>
<td>( x_3 )</td>
</tr>
</tbody>
</table>
4.4.10.9 Translation Access

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>thash</td>
<td></td>
<td>r_f = r_3</td>
<td>1 0 1A</td>
</tr>
<tr>
<td>ttag</td>
<td></td>
<td></td>
<td>1 1B</td>
</tr>
<tr>
<td>tpa^p</td>
<td></td>
<td></td>
<td>1 1E</td>
</tr>
<tr>
<td>tak^p</td>
<td></td>
<td></td>
<td>1 1F</td>
</tr>
</tbody>
</table>

4.4.10.10 Purge Translation Cache Entry

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>ptc.e^p</td>
<td>r_3</td>
<td>1 0</td>
<td>34</td>
</tr>
</tbody>
</table>

4.4.11 Nop/Hint (M-Unit)

M-unit nop and hint instructions are encoded within major opcode 0 using a 3-bit opcode extension field in bits 35:33 (x3), a 2-bit opcode extension field in bits 32:31 (x2), a 4-bit opcode extension field in bits 30:27 (x4), and a 1-bit opcode extension field in bit 26 (y), as shown in Table 4-46.

Table 4-46. Misc M-Unit 1-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x3 Bits 35:33</th>
<th>x4 Bits 30:27</th>
<th>x2 Bits 32:31</th>
<th>y Bit 26</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

4.5 B-Unit Instruction Encodings

The branch-unit includes branch, predict, and miscellaneous instructions.
4.5.1 Branches

Opcode 0 is used for indirect branch, opcode 1 for indirect call, opcode 4 for IP-relative branch, and opcode 5 for IP-relative call.

The IP-relative branch instructions encoded within major opcode 4 use a 3-bit opcode extension field in bits 8:6 (btype) to distinguish the branch types as shown in Table 4-47.

### Table 4-47. IP-Relative Branch Types

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>btype Bits 8:6</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>br.cond B1</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>br.wexit B1</td>
</tr>
<tr>
<td>3</td>
<td>br.wtop B1</td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>br.cloop B2</td>
</tr>
<tr>
<td>6</td>
<td>br.cexit B2</td>
</tr>
<tr>
<td>7</td>
<td>br.ctop B2</td>
</tr>
</tbody>
</table>

The indirect branch, indirect return, and miscellaneous branch-unit instructions are encoded within major opcode 0 using a 6-bit opcode extension field in bits 32:27 (x₆). Table 4-48 summarizes these assignments.

### Table 4-48. Indirect/Miscellaneous Branch Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x₆ Bits 32:31</th>
<th>Bits 30:27</th>
<th>Bits 32:31</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
<td>0 1 2 3</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The indirect branch instructions encoded within major opcodes 0 use a 3-bit opcode extension field in bits 8:6 (btype) to distinguish the branch types as shown in Table 4-49.
The indirect return branch instructions encoded within major opcodes 0 use a 3-bit opcode extension field in bits 8:6 (btype) to distinguish the branch types as shown in Table 4-50.

Table 4-50. Indirect Return Branch Types

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x₆ Bits 32:27</th>
<th>btype Bits 8:6</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>20</td>
<td>br.cond B4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>br.ia B4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>e</td>
</tr>
<tr>
<td></td>
<td></td>
<td>e</td>
</tr>
<tr>
<td></td>
<td></td>
<td>e</td>
</tr>
<tr>
<td></td>
<td></td>
<td>e</td>
</tr>
<tr>
<td></td>
<td></td>
<td>e</td>
</tr>
<tr>
<td></td>
<td></td>
<td>e</td>
</tr>
<tr>
<td></td>
<td></td>
<td>e</td>
</tr>
</tbody>
</table>

All of the branch instructions have a 1-bit opcode extension field, p, in bit 12 which provides a sequential prefetch hint. Table 4-51 summarizes these assignments.

Table 4-51. Sequential Prefetch Hint Completer

<table>
<thead>
<tr>
<th>p Bit 12</th>
<th>ph</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>few</td>
</tr>
<tr>
<td>1</td>
<td>many</td>
</tr>
</tbody>
</table>

The IP-relative and indirect branch instructions all have a 2-bit opcode extension field in bits 34:33 (wh) which encodes branch prediction “whether” hint information as shown in Table 4-52. Indirect call instructions have a 3-bit opcode extension field in bits 34:32 (wh) for “whether” hint information as shown in Table 4-53.

Table 4-52. Branch Whether Hint Completer

<table>
<thead>
<tr>
<th>wh Bits 34:33</th>
<th>bwh</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>.spk</td>
</tr>
<tr>
<td>1</td>
<td>.spnt</td>
</tr>
<tr>
<td>2</td>
<td>.dpk</td>
</tr>
<tr>
<td>3</td>
<td>.dpnt</td>
</tr>
</tbody>
</table>
The branch instructions also have a 1-bit opcode extension field in bit 35 (d) which encodes a branch cache deallocation hint as shown in Table 4-54.

Table 4-53. Indirect Call Whether Hint Completer

<table>
<thead>
<tr>
<th>wh Bits 34:32</th>
<th>bwh</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>.sptk</td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>.spnt</td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>.dptk</td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>.dpnt</td>
</tr>
</tbody>
</table>

Table 4-54. Branch Cache Deallocation Hint Completer

<table>
<thead>
<tr>
<th>d Bit 35</th>
<th>dh</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>none</td>
</tr>
<tr>
<td>1</td>
<td>.clr</td>
</tr>
</tbody>
</table>

4.5.1.1 IP-Relative Branch

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>br.cond.bwh.ph.dh</td>
<td>target25</td>
<td>4</td>
<td>See Table 4-51 on page 4-315</td>
</tr>
<tr>
<td>br.wexit.bwh.ph.dh</td>
<td>target25</td>
<td>4</td>
<td>See Table 4-52 on page 4-315</td>
</tr>
<tr>
<td>br.wtop.bwh.ph.dh</td>
<td>target25</td>
<td>4</td>
<td>See Table 4-54 on page 4-316</td>
</tr>
</tbody>
</table>

4.5.1.2 IP-Relative Counted Branch

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>br.cloop.bwh.ph.dh</td>
<td>target25</td>
<td>4</td>
<td>See Table 4-51 on page 4-315</td>
</tr>
<tr>
<td>br.cexit.bwh.ph.dh</td>
<td>target25</td>
<td>4</td>
<td>See Table 4-52 on page 4-315</td>
</tr>
<tr>
<td>br.ctop.bwh.ph.dh</td>
<td>target25</td>
<td>4</td>
<td>See Table 4-54 on page 4-316</td>
</tr>
</tbody>
</table>
4.5.1.3 IP-Relative Call

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>br.call.bwh.ph.dh</td>
<td>b1 = target25</td>
<td>5</td>
<td>See Table 4-51 on page 4-315</td>
</tr>
</tbody>
</table>

4.5.1.4 Indirect Branch

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>br.cond.bwh.ph.dh</td>
<td></td>
<td>20</td>
<td>See Table 4-51 on page 4-315</td>
</tr>
</tbody>
</table>

4.5.1.5 Indirect Call

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>br.call.bwh.ph.dh</td>
<td>b1 = b2</td>
<td>1</td>
<td>See Table 4-51 on page 4-315</td>
</tr>
</tbody>
</table>

4.5.2 Branch Predict/Nop/Hint

The branch predict, nop, and hint instructions are encoded in major opcodes 2 (Indirect Predict/Nop/Hint) and 7 (IP-relative Predict). The indirect predict, nop, and hint instructions in major opcode 2 use a 6-bit opcode extension field in bits 32:27 (x6). Table 4-55 summarizes these assignments.
The branch predict instructions all have a 1-bit opcode extension field in bit 35 (ih) which encodes a branch importance hint. The mov to BR instruction (page 4-282) also has this hint in bit 23. Table 4-56 shows these assignments.

Table 4-56. Branch Importance Hint Completer

<table>
<thead>
<tr>
<th>ih Bit 23 or Bit 35</th>
<th>ih</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>none</td>
</tr>
<tr>
<td>1</td>
<td>.imp</td>
</tr>
</tbody>
</table>

The IP-relative branch predict instructions have a 2-bit opcode extension field in bits 4:3 (wh) which encodes branch prediction “whether” hint information as shown in Table 4-57. Note that the combination of the .loop or .exit whether hint completer with the none importance hint completer is undefined.

Table 4-57. IP-Relative Predict Whether Hint Completer

<table>
<thead>
<tr>
<th>wh Bits 4:3</th>
<th>ipwh</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>.sptk</td>
</tr>
<tr>
<td>1</td>
<td>.loop</td>
</tr>
<tr>
<td>2</td>
<td>.dptk</td>
</tr>
<tr>
<td>3</td>
<td>.exit</td>
</tr>
</tbody>
</table>

The indirect branch predict instructions have a 2-bit opcode extension field in bits 4:3 (wh) which encodes branch prediction “whether” hint information as shown in Table 4-58.
Table 4-58. Indirect Predict Whether Hint Completer

<table>
<thead>
<tr>
<th>wh Bits 4:3</th>
<th>indwh</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>.spltk</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>.dpltk</td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
</tbody>
</table>

4.5.2.1 IP-Relative Predict

4.5.2.2 Indirect Predict

4.5.3 Miscellaneous B-Unit Instructions

The miscellaneous branch-unit instructions include a number of instructions encoded within major opcode 0 using a 6-bit opcode extension field in bits 32:27 (x6) as described in Table 4-48 on page 4-314.
4.5.3.1 Miscellaneous (B-Unit)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>cover&lt;sup&gt;1&lt;/sup&gt;</td>
<td>002</td>
<td>x&lt;sub&gt;6&lt;/sub&gt;</td>
</tr>
<tr>
<td>clrrb&lt;sup&gt;1&lt;/sup&gt;</td>
<td>004</td>
<td></td>
</tr>
<tr>
<td>clrrb.pr&lt;sup&gt;1&lt;/sup&gt;</td>
<td>005</td>
<td></td>
</tr>
<tr>
<td>rfi e&lt;sup&gt;1&lt;/sup&gt;p</td>
<td>008</td>
<td></td>
</tr>
<tr>
<td>bsw.0&lt;sup&gt;1&lt;/sup&gt;p</td>
<td>00C</td>
<td></td>
</tr>
<tr>
<td>bsw.1&lt;sup&gt;1&lt;/sup&gt;p</td>
<td>00D</td>
<td></td>
</tr>
<tr>
<td>epc</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

4.5.3.2 Break/Nop/Hint (B-Unit)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>break.b&lt;sup&gt;2&lt;/sup&gt;</td>
<td>imm&lt;sub&gt;21&lt;/sub&gt;</td>
<td>0</td>
<td>x&lt;sub&gt;6&lt;/sub&gt;</td>
</tr>
<tr>
<td>nop.b</td>
<td></td>
<td>2</td>
<td>00</td>
</tr>
<tr>
<td>hint.b</td>
<td></td>
<td></td>
<td>01</td>
</tr>
</tbody>
</table>

4.6 F-Unit Instruction Encodings

The floating-point instructions are encoded in major opcodes 8 – E for floating-point and fixed-point arithmetic, opcode 4 for floating-point compare, opcode 5 for floating-point class, and opcodes 0 and 1 for miscellaneous floating-point instructions.

The miscellaneous and reciprocal approximation floating-point instructions are encoded within major opcodes 0 and 1 using a 1-bit opcode extension field (x) in bit 33 and either a second 1-bit extension field in bit 36 (q) or a 6-bit opcode extension field (x<sub>6</sub>) in bits 32:27. Table 4-59 shows the 1-bit x assignments, Table 4-62 shows the additional 1-bit q assignments for the reciprocal approximation instructions; Table 4-60 and Table 4-61 summarize the 6-bit x<sub>6</sub> assignments.

Table 4-59. Miscellaneous Floating-point 1-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode</th>
<th>x Bit 33</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td></td>
<td>6-bit Ext (Table 4-60)</td>
</tr>
<tr>
<td>0 1</td>
<td></td>
<td>Reciprocal Approximation (Table 4-62)</td>
</tr>
<tr>
<td>1 0</td>
<td></td>
<td>6-bit Ext (Table 4-61)</td>
</tr>
<tr>
<td>1 1</td>
<td></td>
<td>Reciprocal Approximation (Table 4-62)</td>
</tr>
</tbody>
</table>
### Table 4-60. Opcode 0 Miscellaneous Floating-point 6-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x Bit 33</th>
<th>Bits 30:27</th>
<th>Bits 32:31</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>x6</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>break.f F15</td>
<td>fmerge.s F9</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1-bit Ext</td>
<td>fmerge.ns F9</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(Table 4-68)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>fmerge.se F9</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>fsetc F12</td>
<td>min F8</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>fclrf F13</td>
<td>fmax F8</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>fmin F8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>fmax F8</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>fchrf F14</td>
<td>fcvt.fx F10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>fcvt.fxu F10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>fcvt.fxu.trunc F10</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>fpcvt.fx F10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A</td>
<td>fpcvt.fxu.trunc F10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>fpcvt.fx.trunc F10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>C</td>
<td>fpcvt.fx.trunc F10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>D</td>
<td>fpcvt.fx.trunc F10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>E</td>
<td>fpcvt.fx.trunc F10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>F</td>
<td>fpcvt.fx.trunc F10</td>
<td></td>
</tr>
</tbody>
</table>

### Table 4-61. Opcode 1 Miscellaneous Floating-point 6-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x Bit 33</th>
<th>Bits 30:27</th>
<th>Bits 32:31</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>x6</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>fmerge.s F9</td>
<td>fcmp.eq F8</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>fmerge.ns F9</td>
<td>fcmp.lt F8</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>fmerge.se F9</td>
<td>fcmp.le F8</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>fcmp.unord F8</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>fmin F8</td>
<td>fcmp.neq F8</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>fmax F8</td>
<td>fcmp.nlt F8</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>fmin F8</td>
<td>fcmp.nle F8</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>fmax F8</td>
<td>fcmp.ord F8</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>fcvt.fx F10</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>fcvt.fxu F10</td>
<td></td>
</tr>
<tr>
<td>A</td>
<td></td>
<td>fcvt.fxu.trunc F10</td>
<td></td>
</tr>
<tr>
<td>B</td>
<td></td>
<td>fcvt.fxu.trunc F10</td>
<td></td>
</tr>
<tr>
<td>C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>D</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Most floating-point instructions have a 2-bit opcode extension field in bits 35:34 (sf) which encodes the FPSR status field to be used. Table 4-63 summarizes these assignments.

### Table 4-63. Floating-point Status Field Completer

<table>
<thead>
<tr>
<th>sf Bits 35:34</th>
<th>sf</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>.s0</td>
</tr>
<tr>
<td>1</td>
<td>.s1</td>
</tr>
<tr>
<td>2</td>
<td>.s2</td>
</tr>
<tr>
<td>3</td>
<td>.s3</td>
</tr>
</tbody>
</table>

#### 4.6.1 Arithmetic

The floating-point arithmetic instructions are encoded within major opcodes 8 – D using a 1-bit opcode extension field (x) in bit 36 and a 2-bit opcode extension field (sf) in bits 35:34. The opcode and x assignments are shown in Table 4-64.

### Table 4-64. Floating-point Arithmetic 1-bit Opcode Extensions

<table>
<thead>
<tr>
<th>x Bit 36</th>
<th>Opcode Bits 40:37</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>fma F1</td>
</tr>
<tr>
<td>1</td>
<td>fma.s F1</td>
</tr>
<tr>
<td>0</td>
<td>fma.d F1</td>
</tr>
<tr>
<td>1</td>
<td>fpma F1</td>
</tr>
<tr>
<td>0</td>
<td>fms F1</td>
</tr>
<tr>
<td>1</td>
<td>fpms F1</td>
</tr>
<tr>
<td>0</td>
<td>fms.d F1</td>
</tr>
<tr>
<td>1</td>
<td>fnma F1</td>
</tr>
<tr>
<td>0</td>
<td>fnma.d F1</td>
</tr>
<tr>
<td>1</td>
<td>fnma.s F1</td>
</tr>
</tbody>
</table>

The fixed-point arithmetic and parallel floating-point select instructions are encoded within major opcode E using a 1-bit opcode extension field (x) in bit 36. The fixed-point arithmetic instructions also have a 2-bit opcode extension field (x2) in bits 35:34. These assignments are shown in Table 4-65.

### Table 4-65. Fixed-point Multiply Add and Select Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x Bit 36</th>
<th>x2 Bits 35:34</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>E</td>
<td>0</td>
<td>fselect F3</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>xma.l F2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>xma.hu F2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>xma.h F2</td>
</tr>
</tbody>
</table>
4.6.1.1 Floating-point Multiply Add

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fma.s sf</td>
<td></td>
<td>8</td>
<td>0</td>
</tr>
<tr>
<td>fma.s.s.sf</td>
<td></td>
<td>9</td>
<td>0</td>
</tr>
<tr>
<td>fma.d sf</td>
<td></td>
<td>A</td>
<td>0</td>
</tr>
<tr>
<td>fpm.add</td>
<td></td>
<td>B</td>
<td>0</td>
</tr>
<tr>
<td>fms.s sf</td>
<td></td>
<td>C</td>
<td>0</td>
</tr>
<tr>
<td>fms.s.s.sf</td>
<td></td>
<td>D</td>
<td>0</td>
</tr>
</tbody>
</table>

The predicate setting floating-point compare instructions are encoded within major opcode 4 using three 1-bit opcode extension fields in bits 33 (ra), 36 (rb), and 12 (ta), and a 2-bit opcode extension field (sf) in bits 35:34. The opcode, ra, rb, and ta assignments are shown in Table 4-66. The sf assignments are shown in Table 4-63 on page 4-322.

4.6.2 Fixed-point Multiply Add

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>xma.l</td>
<td></td>
<td>E</td>
<td>0</td>
</tr>
<tr>
<td>xma.h</td>
<td></td>
<td>E</td>
<td>1</td>
</tr>
<tr>
<td>xma.hu</td>
<td></td>
<td>E</td>
<td>2</td>
</tr>
</tbody>
</table>

4.6.2 Parallel Floating-point Select

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fselect</td>
<td></td>
<td>E</td>
<td>0</td>
</tr>
</tbody>
</table>

4.6.3 Compare and Classify

The predicate setting floating-point compare instructions are encoded within major opcode 4 using three 1-bit opcode extension fields in bits 33 (ra), 36 (rb), and 12 (ta), and a 2-bit opcode extension field (sf) in bits 35:34. The opcode, ra, rb, and ta assignments are shown in Table 4-66. The sf assignments are shown in Table 4-63 on page 4-322.
The parallel floating-point compare instructions are described on page 4-326.

**Table 4-66. Floating-point Compare Opcode Extensions**

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>t_a Bit 33</th>
<th>t_b Bit 36</th>
<th>t_a Bit 12</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>fcmp.eq F4</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>fcmp.eq.unc F4</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>fcmp.lt F4</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>fcmp.lt.unc F4</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>fcmp.le F4</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>fcmp.le.unc F4</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>0</td>
<td>fcmp.unord F4</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>1</td>
<td>fcmp.unord.unc F4</td>
</tr>
</tbody>
</table>

The floating-point class instructions are encoded within major opcode 5 using a 1-bit opcode extension field in bit 12 (t_a) as shown in Table 4-67.

**Table 4-67. Floating-point Class 1-bit Opcode Extensions**

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>t_a Bit 12</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>fclass.m F5</td>
</tr>
<tr>
<td></td>
<td>fclass.m.unc F5</td>
</tr>
</tbody>
</table>

### 4.6.3.1 Floating-point Compare

F4

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fcmp.eq.sf</td>
<td></td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>fcmp.lt.sf</td>
<td>p1, p2 = f2, f3</td>
<td>4</td>
<td>0, 0, 1, 0, 1, 0</td>
</tr>
<tr>
<td>fcmp.le.sf</td>
<td></td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>fcmp.unord.sf</td>
<td></td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>fcmp.eq.unc.sf</td>
<td></td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>fcmp.lt.unc.sf</td>
<td></td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>fcmp.le.unc.sf</td>
<td></td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>fcmp.unord.unc.sf</td>
<td></td>
<td>4</td>
<td></td>
</tr>
</tbody>
</table>

### 4.6.3.2 Floating-point Class

F5

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fclass.m</td>
<td></td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>fclass.m.unc</td>
<td></td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

See Table 4-63 on page 4-322
4.6.4 Approximation

4.6.4.1 Floating-point Reciprocal Approximation

There are two Reciprocal Approximation instructions. The first, in major op 0, encodes the full register variant. The second, in major op 1, encodes the parallel variant.

```
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>frcprca.sf</td>
<td>f1, p2 = f2, f3</td>
<td>0 1</td>
<td>x q sf</td>
</tr>
<tr>
<td>fprcprca.sf</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

See Table 4-63 on page 4-322.

4.6.4.2 Floating-point Reciprocal Square Root Approximation

There are two Reciprocal Square Root Approximation instructions. The first, in major op 0, encodes the full register variant. The second, in major op 1, encodes the parallel variant.

```
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>frsqrta.sf</td>
<td>f1, p2 = f3</td>
<td>0 1</td>
<td>x q sf</td>
</tr>
<tr>
<td>fprsqrta.sf</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

See Table 4-63 on page 4-322.
4.6.5 Minimum/Maximum and Parallel Compare

There are two groups of Minimum/Maximum instructions. The first group, in major op 0, encodes the full register variants. The second group, in major op 1, encodes the parallel variants. The parallel compare instructions are all encoded in major op 1.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fmin.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>0</td>
<td>14</td>
</tr>
<tr>
<td>fmax.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>0</td>
<td>15</td>
</tr>
<tr>
<td>famin.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td>famax.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>0</td>
<td>17</td>
</tr>
<tr>
<td>fpmin.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>0</td>
<td>14</td>
</tr>
<tr>
<td>fpmax.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>0</td>
<td>15</td>
</tr>
<tr>
<td>fpamin.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>0</td>
<td>16</td>
</tr>
<tr>
<td>fpamax.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>0</td>
<td>17</td>
</tr>
<tr>
<td>fpcmp.eq.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>1</td>
<td>30</td>
</tr>
<tr>
<td>fpcmp.lt.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>1</td>
<td>31</td>
</tr>
<tr>
<td>fpcmp.le.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>1</td>
<td>32</td>
</tr>
<tr>
<td>fpcmp.unord.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>1</td>
<td>33</td>
</tr>
<tr>
<td>fpcmp.neq.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>1</td>
<td>34</td>
</tr>
<tr>
<td>fpcmp.nlt.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>1</td>
<td>35</td>
</tr>
<tr>
<td>fpcmp.nle.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>1</td>
<td>36</td>
</tr>
<tr>
<td>fpcmp.ord.sf</td>
<td>$f_i = f_2, f_3$</td>
<td>1</td>
<td>37</td>
</tr>
</tbody>
</table>

See Table 4-63 on page 4-322.
### 4.6.6 Merge and Logical

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fmerge.s</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fmerge.ns</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fmerge.se</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fmix.lr</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fmix.r</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fmix.l</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fsxt.r</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fsxt.l</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fpack</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fswap</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fswap.nl</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fswap.nr</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fand</td>
<td></td>
<td></td>
<td>0</td>
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<tr>
<td>fandcm</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>for</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fxor</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fpmerge.s</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fpmerge.ns</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fpmerge.se</td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

### 4.6.7 Conversion

#### 4.6.7.1 Convert Floating-point to Fixed-point

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fcvt.fx.sf</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fcvt.fsu.sf</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fcvt.fx.trunc.sf</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fcvt.fxu.trunc.sf</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fpfcvt.fx.sf</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fpfcvt.fsu.sf</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fpfcvt.fx.trunc.sf</td>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>fpfcvt.fxu.trunc.sf</td>
<td></td>
<td></td>
<td>0</td>
</tr>
</tbody>
</table>

See Table 4-63 on page 4-322.
4.6.7.2 Convert Fixed-point to Floating-point

- **F11**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fcvtxf</td>
<td>x x_9</td>
<td>f_2</td>
<td>f_1 qp</td>
</tr>
</tbody>
</table>

  - $f_1 = f_2$

4.6.8 Status Field Manipulation

4.6.8.1 Floating-point Set Controls

- **F12**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fsetc.sf</td>
<td>x x_9 amask_7c amask_7b</td>
<td>0 0</td>
<td>04</td>
</tr>
</tbody>
</table>

  - See Table 4-63 on page 4-322

4.6.8.2 Floating-point Clear Flags

- **F13**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fclr.fsf</td>
<td>0 0</td>
<td>05</td>
</tr>
</tbody>
</table>

  - See Table 4-63 on page 4-322

4.6.8.3 Floating-point Check Flags

- **F14**

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>fchkf.sf</td>
<td>x_9 target_125</td>
<td>0 0</td>
<td>08</td>
</tr>
</tbody>
</table>

  - See Table 4-63 on page 4-322
4.6.9 Miscellaneous F-Unit Instructions

4.6.9.1 Break (F-Unit)

F-unit nop and hint instructions are encoded within major opcode 0 using a 3-bit opcode extension field in bits 35:33 (x3), a 6-bit opcode extension field in bits 32:27 (x6), and a 1-bit opcode extension field in bit 26 (y), as shown in Table 4-46.

4.6.9.2 Nop/Hint (F-Unit)

F-unit nop and hint instructions are encoded within major opcode 0 using a 3-bit opcode extension field in bits 35:33 (x3), a 6-bit opcode extension field in bits 32:27 (x6), and a 1-bit opcode extension field in bit 26 (y), as shown in Table 4-46.

Table 4-68. Misc F-Unit 1-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x Bit:33</th>
<th>y Bit:27</th>
<th>y Bit 26</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

4.7 X-Unit Instruction Encodings

The X-unit instructions occupy two instruction slots, L+X. The major opcode, opcode extensions and hints, qp, and small immediate fields occupy the X instruction slot. For movl, break.x, and nop.x, the imm4:1 field occupies the L instruction slot. For brl, the imm39 field and a 2-bit Ignored field occupy the L instruction slot.

4.7.1 Miscellaneous X-Unit Instructions

The miscellaneous X-unit instructions are encoded in major opcode 0 using a 3-bit opcode extension field (x3) in bits 35:33 and a 6-bit opcode extension field (x6) in bits 32:27. Table 4-69 shows the 3-bit assignments and Table 4-70 summarizes the 6-bit assignments. These instructions are executed by an I-unit.
4.7.1.1 Break (X-Unit)

**Table 4-69. Misc X-Unit 3-bit Opcode Extensions**

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x₃ Bits 35:33</th>
<th>6-bit Ext (Table 4-70)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>7</td>
<td></td>
</tr>
</tbody>
</table>

**Table 4-70. Misc X-Unit 6-bit Opcode Extensions**

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x₃ Bits 35:33</th>
<th>x₆ Bits 32:31</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1-bit Ext</td>
</tr>
<tr>
<td>0</td>
<td>2</td>
<td>(Table 4-73)</td>
</tr>
<tr>
<td>0</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>9</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>B</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>C</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>D</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>E</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>F</td>
<td></td>
</tr>
</tbody>
</table>

4.7.2 Move Long Immediate₆₄

The move long immediate instruction is encoded within major opcode 6 using a 1-bit reserved opcode extension in bit 20 (v₉) as shown in Table 4-71. This instruction is executed by an I-unit.
4.7.3 Long Branches

Long branches are executed by a B-unit. Opcode C is used for long branch and opcode D for long call.

The long branch instructions encoded within major opcode C use a 3-bit opcode extension field in bits 8:6 (btype) to distinguish the branch types as shown in Table 4-72.

Table 4-72. Long Branch Types

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>btype Bits 8:6</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>7</td>
</tr>
</tbody>
</table>

The long branch instructions have the same opcode hint fields in bit 12 (p), bits 34:33 (wh), and bit 35 (d) as normal IP-relative branches. These are shown in Table 4-51 on page 4-315, Table 4-52 on page 4-315, and Table 4-54 on page 4-316.

4.7.3.1 Long Branch

Table 4-71. Move Long 1-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
</tr>
</tbody>
</table>

Table 4-72. Long Branch Types

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>movl $X2$</td>
<td>$r_j = imm_{64}$</td>
<td>6</td>
<td>0</td>
</tr>
</tbody>
</table>

See Table 4-51 on page 4-315

See Table 4-52 on page 4-315

See Table 4-54 on page 4-316
4.7.3.2 Long Call

X4

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>brl.call.bwh.ph.dh</td>
<td>h_1 = target_64</td>
<td>D</td>
<td>See Table 4-51 on page 4-315</td>
</tr>
</tbody>
</table>

4.7.4 Nop/Hint (X-Unit)

X-unit nop and hint instructions are encoded within major opcode 0 using a 3-bit opcode extension field in bits 35:33 (x_3), a 6-bit opcode extension field in bits 32:27 (x_6), and a 1-bit opcode extension field in bit 26 (y), as shown in Table 4-73. These instructions are executed by an I-unit.

Table 4-73. Misc X-Unit 1-bit Opcode Extensions

<table>
<thead>
<tr>
<th>Opcode Bits 40:37</th>
<th>x_3 Bits 35:33</th>
<th>x_6 Bits 32:27</th>
<th>y Bit 26</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>01</td>
<td>0</td>
<td>nop.m</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>hint.m</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Operands</th>
<th>Opcode</th>
<th>Extension</th>
</tr>
</thead>
<tbody>
<tr>
<td>nop.x</td>
<td>imm_62</td>
<td>0</td>
<td>x_3 x_6 y</td>
</tr>
<tr>
<td>hint.x</td>
<td></td>
<td>0</td>
<td>0 0 1 0</td>
</tr>
</tbody>
</table>

4.8 Immediate Formation

Table 4-74 shows, for each instruction format that has one or more immediates, how those immediates are formed. In each equation, the symbol to the left of the equals is the assembly language name for the immediate. The symbols to the right are the field names in the instruction encoding.

Table 4-74. Immediate Formation

<table>
<thead>
<tr>
<th>Instruction Format</th>
<th>Immediate Formation</th>
</tr>
</thead>
<tbody>
<tr>
<td>A2</td>
<td>count_2 = ct_2d + 1</td>
</tr>
<tr>
<td>A3 A8 I27 M30</td>
<td>imm_8 = sign_ext(s &lt;&lt; 7</td>
</tr>
<tr>
<td>A4</td>
<td>imm_14 = sign_ext(s &lt;&lt; 13</td>
</tr>
<tr>
<td>A5</td>
<td>imm_22 = sign_ext(s &lt;&lt; 21</td>
</tr>
<tr>
<td>A10</td>
<td>count_2 = (ct_2d &gt; 2) ? reservedOP : ct_2d + 1</td>
</tr>
<tr>
<td>I1</td>
<td>count_2 = (ct_2d == 0) ? 0 : (ct_2d == 1) ? 7 : (ct_2d == 2) ? 15 : 16</td>
</tr>
<tr>
<td>Instruction Format</td>
<td>Immediate Formation</td>
</tr>
<tr>
<td>-------------------</td>
<td>---------------------</td>
</tr>
<tr>
<td>mbtype4 = (mbt4c == 0) ? @brst : (mbt4c == 8) ? @mix : (mbt4c == 9) ? @shuf : (mbt4c == 0xA) ? @alt : (mbt4c == 0xB) ? @rev : reservedQP³³</td>
<td></td>
</tr>
<tr>
<td>mhtype8 = mht8c</td>
<td></td>
</tr>
<tr>
<td>count5 = count5b</td>
<td></td>
</tr>
<tr>
<td>count5 = 31 – ccount5c</td>
<td></td>
</tr>
<tr>
<td>count6 = count6d</td>
<td></td>
</tr>
<tr>
<td>len6 = len6d + 1</td>
<td></td>
</tr>
<tr>
<td>pos6 = pos6b</td>
<td></td>
</tr>
<tr>
<td>len6 = len6d + 1</td>
<td></td>
</tr>
<tr>
<td>pos6 = 63 – cpos6c</td>
<td></td>
</tr>
<tr>
<td>len6 = len6d + 1</td>
<td></td>
</tr>
<tr>
<td>pos6 = 63 – cpos6c</td>
<td></td>
</tr>
<tr>
<td>len6 = len6d + 1</td>
<td></td>
</tr>
<tr>
<td>pos6 = 63 – cpos6c</td>
<td></td>
</tr>
<tr>
<td>len6 = len6d + 1</td>
<td></td>
</tr>
<tr>
<td>pos6 = 63 – cpos6d</td>
<td></td>
</tr>
<tr>
<td>len6 = len6d + 1</td>
<td></td>
</tr>
<tr>
<td>pos6 = 63 – cpos6d</td>
<td></td>
</tr>
<tr>
<td>len6 = len6d + 1</td>
<td></td>
</tr>
<tr>
<td>pos6 = pos6b</td>
<td></td>
</tr>
<tr>
<td>imm8 = sign_ext(s &lt;&lt; 7</td>
<td>imm7b, 8)</td>
</tr>
<tr>
<td>len6 = len6d + 1</td>
<td></td>
</tr>
<tr>
<td>pos6 = 63 – cpos6b</td>
<td></td>
</tr>
<tr>
<td>imm1 = sign_ext(s, 1)</td>
<td></td>
</tr>
<tr>
<td>len6 = len6d + 1</td>
<td></td>
</tr>
<tr>
<td>pos6 = 63 – cpos6d</td>
<td></td>
</tr>
<tr>
<td>pos6 = pos6b</td>
<td></td>
</tr>
<tr>
<td>tag13 = IP + (sign_ext(timm9c, 9) &lt;&lt; 4)</td>
<td></td>
</tr>
<tr>
<td>mask17 = sign_ext(s &lt;&lt; 16</td>
<td>mask8c &lt;&lt; 8</td>
</tr>
<tr>
<td>imm4d = sign_ext(s &lt;&lt; 43</td>
<td>imm27a &lt;&lt; 16, 44)</td>
</tr>
<tr>
<td>M3 M8 M15</td>
<td></td>
</tr>
<tr>
<td>imm9 = sign_ext(s &lt;&lt; 8</td>
<td>i &lt;&lt; 7</td>
</tr>
<tr>
<td>M5 M10</td>
<td></td>
</tr>
<tr>
<td>imm9 = sign_ext(s &lt;&lt; 8</td>
<td>i &lt;&lt; 7</td>
</tr>
<tr>
<td>M17</td>
<td></td>
</tr>
<tr>
<td>inc3 = sign_ext(((s) ? –1 : 1) * ((i2b == 3) ? 1 : 1 &lt;&lt; (4 – i2b)), 6)</td>
<td></td>
</tr>
<tr>
<td>M22 M23</td>
<td></td>
</tr>
<tr>
<td>target25 = IP + (sign_ext(s &lt;&lt; 20</td>
<td>imm13c &lt;&lt; 7</td>
</tr>
<tr>
<td>M34</td>
<td></td>
</tr>
<tr>
<td>il = sol</td>
<td></td>
</tr>
<tr>
<td>o = sof – sol</td>
<td></td>
</tr>
<tr>
<td>r = sor &lt;&lt; 3</td>
<td></td>
</tr>
<tr>
<td>M39 M40</td>
<td></td>
</tr>
<tr>
<td>imm2 = i2b</td>
<td></td>
</tr>
<tr>
<td>M44</td>
<td></td>
</tr>
<tr>
<td>imm24 = i &lt;&lt; 23</td>
<td>l2d &lt;&lt; 21</td>
</tr>
<tr>
<td>B1 B2 B3</td>
<td></td>
</tr>
<tr>
<td>target25 = IP + (sign_ext(s &lt;&lt; 20</td>
<td>imm20b-21) &lt;&lt; 4)</td>
</tr>
<tr>
<td>B6</td>
<td></td>
</tr>
<tr>
<td>target25 = IP + (sign_ext(s &lt;&lt; 20</td>
<td>imm20b-21) &lt;&lt; 4)</td>
</tr>
<tr>
<td>tag13 = IP + (sign_ext(t2e &lt;&lt; 7</td>
<td>timm7a, 9) &lt;&lt; 4)</td>
</tr>
<tr>
<td>B7</td>
<td></td>
</tr>
<tr>
<td>tag13 = IP + (sign_ext(t2e &lt;&lt; 7</td>
<td>timm7a, 9) &lt;&lt; 4)</td>
</tr>
<tr>
<td>B9</td>
<td></td>
</tr>
<tr>
<td>imm21 = i &lt;&lt; 20</td>
<td>imm20a</td>
</tr>
<tr>
<td>F5</td>
<td></td>
</tr>
<tr>
<td>fclass9 = fclass7c &lt;&lt; 2</td>
<td>fc2</td>
</tr>
<tr>
<td>F12</td>
<td></td>
</tr>
<tr>
<td>amask7 = amask7b</td>
<td></td>
</tr>
<tr>
<td>omask7 = omask7c</td>
<td></td>
</tr>
<tr>
<td>F14</td>
<td></td>
</tr>
<tr>
<td>target25 = IP + (sign_ext(s &lt;&lt; 20</td>
<td>imm20a-21) &lt;&lt; 4)</td>
</tr>
<tr>
<td>F15 F16</td>
<td></td>
</tr>
<tr>
<td>imm21 = i &lt;&lt; 20</td>
<td>imm20a</td>
</tr>
<tr>
<td>X1 X5</td>
<td></td>
</tr>
<tr>
<td>imm62 = imm41 &lt;&lt; 21</td>
<td>i &lt;&lt; 20</td>
</tr>
<tr>
<td>X2</td>
<td></td>
</tr>
<tr>
<td>imm6d = i &lt;&lt; 63</td>
<td>imm41 &lt;&lt; 22</td>
</tr>
<tr>
<td>X3 X4</td>
<td></td>
</tr>
<tr>
<td>target6d = IP + (l &lt;&lt; 59</td>
<td>imm39 &lt;&lt; 20</td>
</tr>
</tbody>
</table>

a. This encoding causes an Illegal Operation fault if the value of the qualifying predicate is 1.
5.1 Reading and Writing Resources

An Itanium instruction is said to be a **reader** of a resource if the instruction’s qualifying predicate is 1 or it has no qualifying predicate or is one of the instructions that reads a resource even when its qualifying predicate is 0, and the execution of the instruction depends on that resource.

An Itanium instruction is said to be a **writer** of a resource if the instruction’s qualifying predicate is 1 or it has no qualifying predicate or writes the resource even when the qualifying predicate is 0, and the execution of the instruction writes that resource.

An Itanium instruction is said to be a reader or writer of a resource even if it only sometimes depends on that resource and it cannot be determined statically whether the resource will be read or written. For example, **cover** only writes CR[IFS] when PSR.ic is 0, but for purposes of dependency, it is treated as if it always writes the resource since this condition cannot be determined statically. On the other hand, **rsm** conditionally writes several bits in the PSR depending on a mask which is encoded as an immediate in the instruction. Since the PSR bits to be written can be determined by examining the encoded instruction, the instruction is treated as only writing those bits which have a corresponding mask bit set. All exceptions to these general rules are described in this appendix.

5.2 Dependencies and Serialization

A **RAW** (Read-After-Write) dependency is a sequence of two events where the first is a writer of a resource and the second is a reader of the same resource. Events may be instructions, interruptions, or other ‘uses’ of the resource such as instruction stream fetches and VHPT walks. **Table 5-2** covers only dependencies based on instruction readers and writers.

A **WAW** (Write-After-Write) dependency is a sequence of two events where both events write the resource in question. Events may be instructions, interruptions, or other ‘updates’ of the resource. **Table 5-3** covers only dependencies based on instruction writers.

A **WAR** (Write-After-Read) dependency is a sequence of two instructions, where the first is a reader of a resource and the second is a writer of the same resource. Such dependencies are always allowed except as indicated in **Table 5-4** and only those related to instruction readers and writers are included.

A **RAR** (Read-After-Read) dependency is a sequence of two instructions where both are readers of the same resource. Such dependencies are always allowed.

RAW and WAW dependencies are generally not allowed without some type of serialization event (an implied, data, or instruction serialization after the first writing instruction. (See Section 3.2, “Serialization” on page 2:13 for details on serialization.) The tables and associated rules in this appendix provide a comprehensive list of readers and writers of resources and describe the
serialization required for the dependency to be observed and possible outcomes if the required serialization is not met. Even when targeting code for machines which do not check for particular disallowed dependencies, such code sequences are considered architecturally undefined and may cause code to behave differently across processors, operating systems, or even separate executions of the code sequence during the same program run. In some cases, different serializations may yield different, but well-defined results.

The serialization of application level (non-privileged) resources is always implied. This means that if a writer of that resource and a subsequent read of that same resource are in different instruction groups, then the reader will see the value written. In addition, for dependencies on PRs and BRs, where the writer is a non-branch instruction and the reader is a branch instruction, the writer and reader may be in the same instruction group.

System resources generally require explicit serialization, i.e., the use of a srlz.i or srlz.d instruction, between the writing and the reading of that resource. Note that RAW accesses to CRs are not exceptional - they require explicit data or instruction serialization. However, in some cases (other than CRs) where pairs of instructions explicitly encode the same resource, serialization is implied.

There are cases where it is architecturally allowed to omit a serialization, and that the response from the CPU must be atomic (act as if either the old or the new state were fully in place). The tables in this appendix indicate dependency requirements under the assumption that the desired result is for the dependency to always be observed. In some such cases, the programmer may not care if the old or new state is used; such situations are allowed, but the value seen is not deterministic.

On the other hand, if an impliedF dependency is violated, then the program is incorrectly coded and the processor's behavior is undefined.

5.3 Resource and Dependency Table Format Notes

• The “Writers” and “Readers” columns of the dependency tables contain instruction class names and instruction mnemonic prefixes as given in the format section of each instruction page. To avoid ambiguity, instruction classes are shown in bold, while instruction mnemonic prefixes are in regular font. For instruction mnemonic prefixes, all instructions that exactly match the name specified or those that begin with the specified text and are followed by a ‘.’ and then followed by any other text will match.

• The dependency on a listed instruction is in effect no matter what values are encoded in the instruction or what dynamic values occur in operands, unless a superscript is present or one of the special case instruction rules in Section 5.3.1 applies. Instructions listed are still subject to rules regarding qualifying predicates.

• Instruction classes are groups of related instructions. Such names appear in boldface for clarity. The list of all instruction classes is contained in Table 5-5. Note that an instruction may appear in multiple instruction classes, instruction classes may expand to contain other classes, and that when fully expanded, a set of classes (e.g., the readers of some resource) may contain the same instruction multiple times.
• The syntax ‘\(x \backslash y\)’ where \(x\) and \(y\) are both instruction classes, indicates an unnamed instruction class that includes all instructions in instruction class \(x\) but that are not in instruction class \(y\). Similarly, the notation ‘\(x \backslash y \backslash z\)’ means all instructions in instruction class \(x\), but that are not in either instruction class \(y\) or instruction class \(z\).

• Resources on separate rows of a table are independent resources. This means that there are no serialization requirements for an event which references one of them followed by an event which uses a different resource. In cases where resources are broken into subrows, dependencies only apply between instructions within a subrow. Instructions that do not appear in a subrow together have no dependencies (reader/writer or writer/writer dependencies) for the resource in question, although they may still have dependencies on some other resource.

• The dependencies listed for pairs of instructions on each resource are not unique -- the same pair of instructions might also have a dependency on some other resource with a different semantics of dependency. In cases where there are multiple resource dependencies for the same pair of instructions, the most stringent semantics are assumed: instr overrides data which overrides implied which overrides impliedF which overrides none.

• Arrays of numbered resources are represented in a single row of a table using the % notation as a substitute for the number of the resource. In such cases, the semantics of the table are as if each numbered resource had its own row in that table and is thus an independent resource. The range of values that the % can take are given in the “Resource Name” column.

• An asterisk ‘*’ in the “Resource Name” column indicates that this resource may not have a physical resource associated with it, but is added to enforce special dependencies.

• A pound sign ‘#’ in the “Resource Name” column indicates that this resource is an array of resources that are indexed by a value in a GR. The number of individual elements in the array is described in the detailed description of each resource.

• The “Semantics of Dependency” column describes the outcome given various serialization and instruction group boundary conditions. The exact definition for each keyword is given in Table 5-1.

### Table 5-1. Semantics of Dependency Codes

<table>
<thead>
<tr>
<th>Semantics of Dependency Code</th>
<th>Serialization Type Required</th>
<th>Effects of Serialization Violation</th>
</tr>
</thead>
<tbody>
<tr>
<td>instr</td>
<td>Instruction Serialization (See &quot;Instruction Serialization&quot; on page 2:14).</td>
<td>Atomic: Any attempt to read a resource after one or more insufficiently serialized writes is either the value previously in the register (before any of the una serialized writes) or the value of one of any unserialized writes. Which value is returned is unpredictable and multiple insufficiently serialized reads may see different results. No fault will be caused by the insufficient serialization.</td>
</tr>
<tr>
<td>data</td>
<td>Data Serialization (See &quot;Data Serialization&quot; on page 2:14)</td>
<td></td>
</tr>
<tr>
<td>implied</td>
<td>Instruction Group Break. Writer and reader must be in separate instruction groups. (See &quot;Instruction Sequencing Considerations&quot; on page 1:33).</td>
<td>An undefined value is returned, or an Illegal Operation fault may be taken. If no fault is taken, the value returned is unpredictable, and may be unrelated to past writes, but will not be data which could not be accessed by the current process (e.g., if PSR.cpl != 0, the undefined value to return cannot be read from some control register).</td>
</tr>
<tr>
<td>impliedF</td>
<td>Instruction Group Break (same as above).</td>
<td></td>
</tr>
<tr>
<td>stop</td>
<td>Stop. Writer and reader must be separated by a stop.</td>
<td></td>
</tr>
<tr>
<td>none</td>
<td>None</td>
<td>N/A</td>
</tr>
<tr>
<td>specific</td>
<td>Implementation Specific</td>
<td></td>
</tr>
<tr>
<td>SC</td>
<td>Special Case</td>
<td>Described elsewhere in book, see referenced section in the entry.</td>
</tr>
</tbody>
</table>
5.3.1 Special Case Instruction Rules

The following rules apply to the specified instructions when they appear in Table 5-2, Table 5-3, Table 5-4, or Table 5-5:

- An instruction always reads a given resource if its qualifying predicate is 1 and it appears in the “Reader” column of the table (except as noted). An instruction always writes a given resource if its qualifying predicate is 1 and it appears in the “Writer” column of the table (except as noted). An instruction never reads or writes the specified resource if its qualifying predicate is 0 (except as noted). These rules include branches and their qualifying predicate. Instructions in the unpredicatable-instructions class have no qualifying predicate and thus always read or write their resources (except as noted).

- An instruction of type mov-from-PR reads all PRs if its PR[qp] is true. If the PR[qp] is false, then only the PR[qp] is read.

- An instruction of type mov-to-PR writes only those PRs as indicated by the immediate mask encoded in the instruction.

- A st8.spill only writes AR[UNAT]{X} where X equals the value in bits 8:3 of the store’s data address. A ld8.fill instruction only reads AR[UNAT]{Y} where Y equals the value in bits 8:3 of the load’s data address.

- Instructions of type mod-sched-brs always read AR[EC] and the rotating register base registers in CFM, and always write AR[EC], the rotating register bases in CFM, and PR[63] even if they do not change their values or if their PR[qp] is false.

- Instructions of type mod-sched-brs-counted always read and write AR[LC], even if they do not change its value.

- Instructions of type pr-or-writers or pr-and-writers, if their completer is or.andcm, then only the first target predicate is an or-compare and the second target predicate is an and-compare. Similarly, if their completer is and.orcm, then only the second target predicate is an or-compare and the first target predicate is an and-compare.

- rum and sum only read PSR.sp when the bit corresponding to PSR.up (bit 2) is set in the immediate field of the instruction.

5.3.2 RAW Dependency Table

Table 5-2 architecturally defines the following information:

- A list of all architecturally-defined, independently-writable resources in the Itanium architecture. Each row represents an ‘atomic’ resource. Thus, for each row in the table, hardware will probably require a separate write-enable control signal.

- For each resource, a complete list of readers and writers.

- For each instruction, a complete list of all resources read and written. Such a list can be obtained by taking the union of all the rows in which each instruction appears.
<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Readers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALAT</td>
<td>chk.a.clr, mem-readers-alat, mem-writers, invala-all</td>
<td>mem-readers-alat, mem-writers, chk-a, invala.e</td>
<td>none</td>
</tr>
<tr>
<td>AR[BSP]</td>
<td>br.call, brl.call, br.ret, cover, mov-to-AR-BSPSTORE, rfi</td>
<td>br.call, brl.call, br.ret, cover, flushrs, loadsrs, mov-from-AR-BSP, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[BSPSTORE]</td>
<td>alloc, loadrs, flushrs, mov-to-AR-BSPSTORE</td>
<td>alloc, br.ia, flushrs, mov-from-AR-BSPSTORE</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[CCV]</td>
<td>mov-to-AR-CCV</td>
<td>br.ia, cmpxchg, mov-from-AR-CCV</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[CFLG]</td>
<td>mov-to-AR-CFLG</td>
<td>br.ia, mov-from-AR-CFLG</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[CSD]</td>
<td>ld16, mov-to-AR-CSD</td>
<td>br.ia, cmp8xchg16, mov-from-AR-CSD, st16</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[EC]</td>
<td>mod-sched-brs, br.ret, mov-to-AR-EC</td>
<td>br.call, brl.call, br.ia, mod-sched-brs, mov-from-AR-EC</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[EFLAG]</td>
<td>mov-to-AR-EFLAG</td>
<td>br.ia, mov-from-AR-EFLAG</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FCR]</td>
<td>mov-to-AR-FCR</td>
<td>br.ia, mov-from-AR-FCR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FDR]</td>
<td>mov-to-AR-FDR</td>
<td>br.ia, mov-from-AR-FDR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FIR]</td>
<td>mov-to-AR-FIR</td>
<td>br.ia, mov-from-AR-FIR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf0.controls</td>
<td>mov-to-AR-FPSR, fsetc.s0</td>
<td>br.ia, fp-arith-s0, fcmp-s0, fpcmp-s0, fsetc, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf1.controls</td>
<td>mov-to-AR-FPSR, fsetc.s1</td>
<td>br.ia, fp-arith-s1, fcmp-s1, fpcmp-s1, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf2.controls</td>
<td>mov-to-AR-FPSR, fsetc.s2</td>
<td>br.ia, fp-arith-s2, fcmp-s2, fpcmp-s2, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf3.controls</td>
<td>mov-to-AR-FPSR, fsetc.s3</td>
<td>br.ia, fp-arith-s3, fcmp-s3, fpcmp-s3, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf0.flags</td>
<td>fp-arith-s0, fclrf.s0, fcmp-s0, fpcmp-s0, mov-to-AR-FPSR</td>
<td>br.ia, fchkf, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf1.flags</td>
<td>fp-arith-s1, fclrf.s1, fcmp-s1, fpcmp-s1, mov-to-AR-FPSR</td>
<td>br.ia, fchkf.s1, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf2.flags</td>
<td>fp-arith-s2, fclrf.s2, fcmp-s2, fpcmp-s2, mov-to-AR-FPSR</td>
<td>br.ia, fchkf.s2, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf3.flags</td>
<td>fp-arith-s3, fclrf.s3, fcmp-s3, fpcmp-s3, mov-to-AR-FPSR</td>
<td>br.ia, fchkf.s3, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].traps</td>
<td>mov-to-AR-FPSR</td>
<td>br.ia, fp-arith, fchkf, fcmp, fpcmp, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].rv</td>
<td>mov-to-AR-FPSR</td>
<td>br.ia, fp-arith, fchkf, fcmp, fpcmp, mov-from-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FSR]</td>
<td>mov-to-AR-FSR</td>
<td>br.ia, mov-from-AR-FSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[ITC]</td>
<td>mov-to-AR-ITC</td>
<td>br.ia, mov-from-AR-ITC</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[K%], % in 0 - 7</td>
<td>mov-to-AR-K</td>
<td>br.ia, mov-from-AR-K</td>
<td>impliedF</td>
</tr>
</tbody>
</table>
Table 5-2. RAW Dependencies Organized by Resource (Continued)

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Readers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>AR[PFS]</td>
<td>br.call, brl.call</td>
<td>alloc, br.i.a, br.ret, epc,</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>mov-to-AR-PFS</td>
<td>mov-from-AR-PFS</td>
<td></td>
</tr>
<tr>
<td></td>
<td>alloc, br.i.a, epc,</td>
<td>mov-from-AR-PFS</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[RNAT]</td>
<td>alloc, flushrs, loadrs,</td>
<td>alloc, br.i.a, flushrs, loadrs,</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>mov-to-AR-RNAT, mov-to-AR-BSPSTORE</td>
<td>mov-from-AR-RNAT</td>
<td></td>
</tr>
<tr>
<td>AR[RSC]</td>
<td>mov-to-AR-RSC</td>
<td>alloc, flushrs, loadrs,</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>mov-from-AR-RSC, mov-from-AR-BSPSTORE</td>
<td>mov-from-AR-RNAT, mov-to-AR-RNAT</td>
<td></td>
</tr>
<tr>
<td>AR[SSD]</td>
<td>mov-to-AR-SSD</td>
<td>br.i.a, mov-from-AR-SSD</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[UNAT]{%},</td>
<td>mov-to-AR-UNAT, st8.spill</td>
<td>br.i.a, ld8.fill,</td>
<td>impliedF</td>
</tr>
<tr>
<td>% in 0 - 63</td>
<td></td>
<td>mov-from-AR-UNAT</td>
<td></td>
</tr>
<tr>
<td>AR%, % in 8-15, 20, 22-23, 31, 33-35, 37-39, 41-43, 45-47, 67-111</td>
<td>none</td>
<td>br.i.a, mov-from-AR-rv(^1)</td>
<td>none</td>
</tr>
<tr>
<td>AR%, % in 48-63, 112-127</td>
<td>mov-to-AR-ig(^1)</td>
<td>br.i.a, mov-from-AR-ig(^1)</td>
<td>impliedF</td>
</tr>
<tr>
<td>BR%, % in 0 - 7</td>
<td>br.call(^1), brl.call(^1)</td>
<td>indirect-brs(^1), indirect-brp(^1),</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>mov-to-BR(^1)</td>
<td>mov-from-BR(^1)</td>
<td></td>
</tr>
<tr>
<td>CFM</td>
<td>mod-sched-brs</td>
<td>mod-sched-brs</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>cover, alloc, rfi, loadrs, br.ret, br.call,</td>
<td>mov-from-BR(^1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>br.call</td>
<td>cfm-readers(^2)</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>br.call, brl.call, br.ret, clmb, cover, rfi</td>
<td>cfm-readers</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>alloc</td>
<td>cfm-readers</td>
<td>none</td>
</tr>
<tr>
<td>CPUID#</td>
<td>none</td>
<td>mov-from-IND-CPUID(^3)</td>
<td>specific</td>
</tr>
<tr>
<td>CR[EOI]</td>
<td>mov-to-CR-EOI</td>
<td>none</td>
<td>SC Section 5.8.3.4 on page 2.106</td>
</tr>
<tr>
<td>CR[IFA]</td>
<td>mov-to-CR-IFA</td>
<td>ifl.i, ifl.c, ltr.i, ltr.d</td>
<td>implied</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov-from-CR-IFA</td>
<td>data</td>
</tr>
</tbody>
</table>
Table 5-2. RAW Dependencies Organized by Resource (Continued)

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Readers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>CR[IFS]</td>
<td>mov-to-CR-IFS</td>
<td>mov-from-CR-IFS</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td></td>
<td>rfi, mov-from-CR-IFS</td>
<td>implied</td>
</tr>
<tr>
<td></td>
<td></td>
<td>cover</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>rfi</td>
<td>implied</td>
</tr>
<tr>
<td>CR[IRR%], % in 0 - 3</td>
<td>mov-from-CR-IVR</td>
<td>mov-from-CR-IRR</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td></td>
<td>itc.i, itc.d, itr.i, itr.d</td>
<td>implied</td>
</tr>
<tr>
<td>CR[IVR]</td>
<td>none</td>
<td>mov-from-CR-IVR</td>
<td>SC Section 5.8.3.2 on page 2:105</td>
</tr>
<tr>
<td>CR[LID]</td>
<td>mov-to-CR-LID</td>
<td>mov-from-CR-LID</td>
<td>SC Section 5.8.3.1 on page 2:104</td>
</tr>
<tr>
<td>CR[LRR%], % in 0 - 1</td>
<td>mov-to-CR-LRR</td>
<td>mov-from-CR-LRR</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov-to-PSR-l, rfi, rsm, ssm</td>
<td>SC Section 5.8.3.3 on page 2:105</td>
</tr>
<tr>
<td>CR%&gt;, % in 3-7, 10-15, 18, 26-63, 75-79, 82-127</td>
<td>none</td>
<td>mov-from-CR-rv</td>
<td>none</td>
</tr>
<tr>
<td>DBR#</td>
<td>mov-to-IND-DBR3</td>
<td>mov-from-IND-DBR3</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>probe-all, Ifetch-all, mem-readers, mem-writers</td>
<td>data</td>
</tr>
<tr>
<td>DTC</td>
<td>ptc.e, ptc.g, ptc.ga, ptc.l, ptr.i, ptr.d, itc.i, itc.d, itr.i, itr.d</td>
<td>mem-readers, mem-writers, fc, probe-all, tak, lpa</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td></td>
<td>itc.i, itc.d, itr.i, itr.d</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ptc.e, ptc.g, ptc.ga, ptc.l, ptr.i, ptr.d, itc.i, itc.d, itr.i, itr.d</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ptc.e, ptc.g, ptc.ga</td>
<td>ptc.e, ptc.g, ptc.l, ptr.i, ptr.d, itc.i, itc.d, itr.i, itr.d</td>
</tr>
<tr>
<td>DTC_LIMIT*</td>
<td>ptc.g, ptc.ga</td>
<td>ptc.g, ptc.ga</td>
<td>impliedF</td>
</tr>
<tr>
<td>Resource Name</td>
<td>Writers</td>
<td>Readers</td>
<td>Semantics of Dependency</td>
</tr>
<tr>
<td>---------------</td>
<td>---------</td>
<td>---------</td>
<td>-------------------------</td>
</tr>
<tr>
<td>DTR</td>
<td>ltr.d</td>
<td>mem-readers, mem-writers, fc, probe-all, tak, tpa</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ptc.g, ptc.ga, ptc.l, ptr.d, ltr.d</td>
<td>impliedF</td>
</tr>
<tr>
<td>ptr.d</td>
<td>mem-readers, mem-writers, fc, probe-all, tak, tpa</td>
<td>data</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ptc.g, ptc.ga, ptc.l, ptr.d</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ltr.d, ltc.d</td>
<td>impliedF</td>
</tr>
<tr>
<td>FR%, % in 0 - 1</td>
<td>none</td>
<td>fr-readers [^1]</td>
<td>none</td>
</tr>
<tr>
<td>FR%, % in 2 - 127</td>
<td>fr-readers</td>
<td>ldf-c [^1]</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ldpf-c [^1]</td>
<td>impliedF</td>
</tr>
<tr>
<td>GR0</td>
<td>none</td>
<td>gr-readers [^1]</td>
<td>none</td>
</tr>
<tr>
<td>GR%, % in 1 - 127</td>
<td>gr-readers</td>
<td>ldf-c [^1,13]</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ldpf-c [^1,13]</td>
<td>none</td>
</tr>
<tr>
<td>IBR[^#]</td>
<td>mov-to-IND-IBR [^3]</td>
<td>mov-from-IND-IBR [^3]</td>
<td>impliedF</td>
</tr>
<tr>
<td>InService[^*]</td>
<td>mov-to-CR-EOI</td>
<td>mov-from-CR-IVR</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td>mov-from-CR-IVR</td>
<td>mov-to-CR-EOI</td>
<td>impliedF</td>
</tr>
<tr>
<td>IP</td>
<td>all</td>
<td>all</td>
<td>none</td>
</tr>
<tr>
<td>ITC</td>
<td>ptc.e, ptc.g, ptc.ga, ptc.l, ptr.i, ptr.d</td>
<td>epc</td>
<td>instr</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ltc.i, ltc.d, ltr.i, ltr.d</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ptr.i, ptr.d, ptc.e, ptc.g, ptc.ga, ptc.l</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td></td>
<td>epc</td>
<td>instr</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ltc.d, ltc.i, ltr.d, ltr.i, ptr.d, ptr.i, ptc.g, ptc.ga, ptc.l</td>
<td>impliedF</td>
</tr>
<tr>
<td>ITC[^LIMIT[^*]]</td>
<td>ptc.g, ptc.ga</td>
<td>ptc.g, ptc.ga</td>
<td>impliedF</td>
</tr>
<tr>
<td>ITR</td>
<td>ltr.i</td>
<td>ltr.i, ltc.i, ptc.g, ptc.ga, ptc.l, ptr.i</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>epc</td>
<td>instr</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ltc.i, ltr.i</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ptc.g, ptc.ga, ptc.l, ptr.i</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td></td>
<td>epc</td>
<td>instr</td>
</tr>
<tr>
<td>memory</td>
<td>mem-readers</td>
<td>mem-readers</td>
<td>none</td>
</tr>
<tr>
<td>PKR[^#]</td>
<td>mov-to-IND-PKR [^3]</td>
<td>mem-readers, mem-writers, mov-from-IND-PKR [^4], probe-all</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov-to-IND-PKR [^3]</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov-from-IND-PKR [^3]</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov-to-IND-PKR [^3]</td>
<td>impliedF</td>
</tr>
<tr>
<td>PMC[^#]</td>
<td>mov-to-IND-PMC [^3]</td>
<td>mov-from-IND-PMC [^3]</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov-from-IND-PMC [^3]</td>
<td>impliedF</td>
</tr>
<tr>
<td>PMD[^#]</td>
<td>mov-to-IND-PMD [^3]</td>
<td>mov-from-IND-PMD [^3]</td>
<td>impliedF</td>
</tr>
<tr>
<td>PR0</td>
<td>pr-readers [^1]</td>
<td>pr-readers-br [^1], pr-readers-nobr-nomovpr [^1], mov-from-PR [^12], mov-to-PR [^12]</td>
<td>none</td>
</tr>
</tbody>
</table>
Table 5-2. RAW Dependencies Organized by Resource (Continued)

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Readers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>PR%, % in 1 - 15</td>
<td>pr-writers$^1$, mov-to-PR-allreg$^7$</td>
<td>pr-readers-nobr-nomovpr$^1$, mov-from-PR, mov-to-PR$^{12}$</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>pr-writers-fp$^1$</td>
<td>pr-readers-br$^1$</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>pr-writers-int$^1$, mov-to-PR-allreg$^7$</td>
<td>pr-readers-br$^1$</td>
<td>none</td>
</tr>
<tr>
<td>PR%, % in 16 - 62</td>
<td>pr-writers$^1$, mov-to-PR-allreg$^7$, mov-to-PR-rotreg</td>
<td>pr-readers-nobr-nomovpr$^1$, mov-from-PR, mov-to-PR$^{12}$</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>pr-writers-fp$^1$, mod-sched-brs</td>
<td>pr-readers-br$^1$</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>pr-writers-int$^1$, mov-to-PR-allreg$^7$, mov-to-PR-rotreg</td>
<td>pr-readers-br$^1$</td>
<td>none</td>
</tr>
<tr>
<td>PR63</td>
<td>mod-sched-brs, pr-writers$^1$, mov-to-PR-allreg$^7$, mov-to-PR-rotreg</td>
<td>pr-readers-nobr-nomovpr$^1$, mov-from-PR, mov-to-PR$^{12}$</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>pr-writers-fp$^1$, mod-sched-brs</td>
<td>pr-readers-br$^1$</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>pr-writers-int$^1$, mov-to-PR-allreg$^7$, mov-to-PR-rotreg</td>
<td>pr-readers-br$^1$</td>
<td>none</td>
</tr>
<tr>
<td>PSR.ac</td>
<td>user-mask-writers-partial$^7$, mov-to-PSR-um</td>
<td>mem-readers, mem-writers</td>
<td>implied</td>
</tr>
<tr>
<td></td>
<td>user-mask-writers-partial$^7$, mov-to-PSR-um, rfi</td>
<td>mem-readers, mem-writers</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td>sys-mask-writers-partial$^7$, mov-to-PSR-l, rfi</td>
<td>mem-readers, mem-writers</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.be</td>
<td>user-mask-writers-partial$^7$, mov-to-PSR-um</td>
<td>mem-readers, mem-writers</td>
<td>implied</td>
</tr>
<tr>
<td></td>
<td>sys-mask-writers-partial$^7$, mov-to-PSR-l, rfi</td>
<td>mem-readers, mem-writers</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td>user-mask-writers-partial$^7$, mov-to-PSR-um, sys-mask-writers-partial$^7$, mov-to-PSR-l, rfi</td>
<td>mov-from-PSR, mov-from-PSR-um</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.bn</td>
<td>bsw, rfi</td>
<td>gr-readers$^{10}$, gr-writers$^{10}$</td>
<td>impliedF</td>
</tr>
</tbody>
</table>
Table 5-2. RAW Dependencies Organized by Resource (Continued)

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Readers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSR.da</td>
<td>rfi</td>
<td>mem-readers, ifetch-fault, mem-writers, probe-fault</td>
<td>data</td>
</tr>
<tr>
<td>PSR.db</td>
<td>mov-to-PSR-I</td>
<td>mem-readers, mem-writers, probe-fault</td>
<td>data</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov-from-PSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.dd</td>
<td>rfi</td>
<td>mem-readers, probe-fault, mem-writers, ifetch-fault</td>
<td>data</td>
</tr>
<tr>
<td>PSR.dfh</td>
<td>sys-mask-writers-partial, mov-to-PSR-I, rfi</td>
<td>fr-readers, fr-writers, mov-from-PSR</td>
<td>data</td>
</tr>
<tr>
<td>PSR.dfl</td>
<td>sys-mask-writers-partial, mov-to-PSR-I, rfi</td>
<td>fr-writers, fr-readers, mov-from-PSR</td>
<td>data</td>
</tr>
<tr>
<td>PSR.di</td>
<td>sys-mask-writers-partial, mov-to-PSR-I, rfi</td>
<td>br.ia, mov-from-PSR</td>
<td>data</td>
</tr>
<tr>
<td>PSR.dt</td>
<td>sys-mask-writers-partial, mov-to-PSR-I, rfi</td>
<td>mem-readers, mem-writers</td>
<td>data</td>
</tr>
<tr>
<td>PSR.ed</td>
<td>rfi</td>
<td>ifetch-all, mem-readers-spec</td>
<td>data</td>
</tr>
<tr>
<td>PSR.i</td>
<td>sys-mask-writers-partial, mov-to-PSR-I</td>
<td>mov-from-PSR</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>rfi</td>
<td>mov-from-PSR</td>
<td>data</td>
</tr>
<tr>
<td>PSR.ia</td>
<td>rfi</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>PSR.ic</td>
<td>sys-mask-writers-partial, mov-to-PSR-I, rfi</td>
<td>mov-from-PSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.id</td>
<td>rfi</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>PSR.is</td>
<td>br.ia, rfi</td>
<td>none</td>
<td>none</td>
</tr>
</tbody>
</table>
Table 5-2. RAW Dependencies Organized by Resource (Continued)

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Readers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSR.it</td>
<td>rfi</td>
<td>branches, mov-from-PSR, chk, epc, fchkf</td>
<td>data</td>
</tr>
<tr>
<td>PSR.lp</td>
<td>mov-to-PSR-I</td>
<td>mov-from-PSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.mc</td>
<td>rfi</td>
<td>mov-from-PSR, br.ret</td>
<td>data</td>
</tr>
<tr>
<td>PSR.mfh</td>
<td>fr-writers(^7), user-mask-writers-partial(^7), mov-to-PSR-um, sys-mask-writers-partial(^7), mov-to-PSR-I, rfi</td>
<td>mov-from-PSR-um, mov-from-PSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.mfl</td>
<td>fr-writers(^7), user-mask-writers-partial(^7), mov-to-PSR-um, sys-mask-writers-partial(^7), mov-to-PSR-I, rfi</td>
<td>mov-from-PSR-um, mov-from-PSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.pk</td>
<td>sys-mask-writers-partial(^7), mov-to-PSR-I, rfi</td>
<td>mem-readers, mem-writers, probe-all</td>
<td>data</td>
</tr>
<tr>
<td>PSR.pp</td>
<td>sys-mask-writers-partial(^7), mov-to-PSR-I, rfi</td>
<td>mov-from-PSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.ri</td>
<td>rfi</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>PSR.rt</td>
<td>mov-to-PSR-I</td>
<td>alloc, flushrs, loadrs</td>
<td>data</td>
</tr>
<tr>
<td>PSR.si</td>
<td>sys-mask-writers-partial(^7), mov-to-PSR-I, rfi</td>
<td>mov-from-PSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.sp</td>
<td>sys-mask-writers-partial(^7), mov-to-PSR-I, rfi</td>
<td>mov-from-PSR</td>
<td>data</td>
</tr>
<tr>
<td>PSR.ss</td>
<td>rfi</td>
<td>all</td>
<td>data</td>
</tr>
<tr>
<td>PSR.tb</td>
<td>mov-to-PSR-I, rfi</td>
<td>branches, chk, fchkf</td>
<td>data</td>
</tr>
<tr>
<td>PSR.up</td>
<td>user-mask-writers-partial(^7), mov-to-PSR-um, sys-mask-writers-partial(^7), mov-to-PSR-I, rfi</td>
<td>mov-from-PSR-um, mov-from-PSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>RR#</td>
<td>mov-to-IND-RR(^5)</td>
<td>mem-readers, mem-writers, itc.i, itc.d, itri, itr.d, probe-all, ptc.g, ptc.ga, ptc.l, ptr.i, ptr.d, tak, thash, tpa, ttag, mov-from-IND-RR(^5)</td>
<td>data</td>
</tr>
<tr>
<td>RSE</td>
<td>rse-writers(^14)</td>
<td>rse-readers(^14)</td>
<td>impliedF</td>
</tr>
</tbody>
</table>
### 5.3.3 WAW Dependency Table

General rules specific to the WAW table:
- All resources require at most an instruction group break to provide sequential behavior.
- Some resources require no instruction group break to provide sequential behavior.
- There are a few special cases that are described in greater detail elsewhere in the manual and are indicated with an SC (special case) result.
- Each sub-row of writers represents a group of instructions that when taken in pairs in any combination has the dependency result indicated. If the column is split in sub-columns, then the dependency semantics apply to any pair of instructions where one is chosen from left sub-column and one is chosen from the right sub-column.

#### Table 5-3. WAW Dependencies Organized by Resource

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALAT</td>
<td>mem-readers-alat, mem-writers, chk.a.clr, invala-all</td>
<td>none</td>
</tr>
<tr>
<td>AR[BSP]</td>
<td>br.call, brl.call, br_ret, cover, mov-to-AR-BSPSTORE, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[BSPSTORE]</td>
<td>alloc, loadrs, flushrs, mov-to-AR-BSPSTORE</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[CCV]</td>
<td>mov-to-AR-CCV</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[CFLG]</td>
<td>mov-to-AR-CFLG</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[CSD]</td>
<td>ld16, mov-to-AR-CSD</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[EC]</td>
<td>br_ret, mod_sched-brs, mov-to-AR-EC</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[EFLAG]</td>
<td>mov-to-AR-EFLAG</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FCR]</td>
<td>mov-to-AR-FCR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FDR]</td>
<td>mov-to-AR-FDR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FIR]</td>
<td>mov-to-AR-FIR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf0.controls</td>
<td>mov-to-AR-FPSR, fsetc.s0</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf1.controls</td>
<td>mov-to-AR-FPSR, fsetc.s1</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf2.controls</td>
<td>mov-to-AR-FPSR, fsetc.s2</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf3.controls</td>
<td>mov-to-AR-FPSR, fsetc.s3</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].sf0.flags</td>
<td>fclrf.s0, fcmp-s0, fp-arith-s0, fcmp-s0, mov-to-AR-FPSR</td>
<td>fcclrf.s0, mov-to-AR-FPSR</td>
</tr>
<tr>
<td>AR[FPSR].sf1.flags</td>
<td>fp-arith-s1, fcmp-s1, fp-arith-s1, fpcmp-s1, mov-to-AR-FPSR</td>
<td>fcclrf.s1, mov-to-AR-FPSR</td>
</tr>
<tr>
<td>AR[FPSR].sf2.flags</td>
<td>fp-arith-s2, fcmp-s2, fpcmp-s2</td>
<td>fcclrf.s2, mov-to-AR-FPSR</td>
</tr>
<tr>
<td>AR[FPSR].sf3.flags</td>
<td>fp-arith-s3, fcmp-s3, fpcmp-s3</td>
<td>fcclrf.s3, mov-to-AR-FPSR</td>
</tr>
<tr>
<td>AR[FPSR].rv</td>
<td>mov-to-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FPSR].traps</td>
<td>mov-to-AR-FPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[FSR]</td>
<td>mov-to-AR-FSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[ITC]</td>
<td>mov-to-AR-ITC</td>
<td>impliedF</td>
</tr>
</tbody>
</table>
Table 5-3. WAW Dependencies Organized by Resource (Continued)

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>AR[K%], % in 0 - 7</td>
<td>mov-to-AR-K&lt;sup&gt;1&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[LC]</td>
<td>mod-sched-brs-counted, mov-to-AR-LC</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[PFS]</td>
<td>br.call, brcall</td>
<td>none</td>
</tr>
<tr>
<td>AR[RNAT]</td>
<td>alloc, flushrs, loadrs, mov-to-AR-RNAT, mov-to-AR-BSPSTORE</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[RSC]</td>
<td>mov-to-AR-RSC</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[SSD]</td>
<td>mov-to-AR-SSD</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR[UNAT][%], % in 0 - 63</td>
<td>mov-to-AR-UNAT, st8.spill</td>
<td>impliedF</td>
</tr>
<tr>
<td>AR%, % in 48 - 63, 112-127</td>
<td>mov-to-AR-ig&lt;sup&gt;1&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>BR%, % in 0 - 7</td>
<td>br.call&lt;sup&gt;1&lt;/sup&gt;, brcall&lt;sup&gt;1&lt;/sup&gt;</td>
<td>mov-to-BR&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td>CFM</td>
<td>mod-sched-brs, br.call, brcall, br.ret, alloc, clrbb, cover, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>CPUID#</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>CR[CMCV]</td>
<td>mov-to-CR-CMCV</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[DCR]</td>
<td>mov-to-CR-DCR</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[EOI]</td>
<td>mov-to-CR-EOI</td>
<td>SC Section 5.8.3.4 on page 2:106</td>
</tr>
<tr>
<td>CR[GPTA]</td>
<td>mov-to-CR-GPTA</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IFA]</td>
<td>mov-to-CR-IFA</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IFS]</td>
<td>mov-to-CR-IFS, cover</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IHA]</td>
<td>mov-to-CR-IHA</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IIM]</td>
<td>mov-to-CR-IIM</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IIP]</td>
<td>mov-to-CR-IIP</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IIPA]</td>
<td>mov-to-CR-IIPA</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IPSR]</td>
<td>mov-to-CR-IPSR</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IRR%], % in 0 - 3</td>
<td>mov-from-CR-IVR</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[ISR]</td>
<td>mov-to-CR-ISR</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[ITIR]</td>
<td>mov-to-CR-ITIR</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[ITM]</td>
<td>mov-to-CR-ITM</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[ITV]</td>
<td>mov-to-CR-ITV</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IVA]</td>
<td>mov-to-CR-IVA</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[IIV]</td>
<td>none</td>
<td>SC</td>
</tr>
<tr>
<td>CR[LID]</td>
<td>mov-to-CR-LID</td>
<td>SC</td>
</tr>
</tbody>
</table>
### Table 5-3. WAW Dependencies Organized by Resource (Continued)

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>CR(LRR%), % in 0 - 1</td>
<td>mov-to-CR-LRR&lt;sup&gt;1&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR(PMV)</td>
<td>mov-to-CR-PMV</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR(PTA)</td>
<td>mov-to-CR-PTA</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR[TPR]</td>
<td>mov-to-CR-TPR</td>
<td>impliedF</td>
</tr>
<tr>
<td>CR%, % in 3-7, 10-15, 18, 26-63, 75-79, 82-127</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>DBR#</td>
<td>mov-to-IND-DBR&lt;sup&gt;3&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>DTC</td>
<td>ptc.e, ptc.g, itc.i, itc.d, ptc.l, ptr.i, ptr.d</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>ptc.e, ptc.g, ptc.ga, ptc.l, ptr.i, ptr.d, itc.i, itc.d, itr.i, itr.d</td>
<td>impliedF</td>
</tr>
<tr>
<td>DTC_LIMIT*</td>
<td>ptc.g, ptc.ga</td>
<td>impliedF</td>
</tr>
<tr>
<td>DTR</td>
<td>itr.d</td>
<td>impliedF</td>
</tr>
<tr>
<td></td>
<td>itr.d</td>
<td>ptr.d</td>
</tr>
<tr>
<td></td>
<td>ptr.d</td>
<td>none</td>
</tr>
<tr>
<td>FR%, % in 0 - 1</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>FR%, % in 2 - 127</td>
<td>fr-writers&lt;sup&gt;1, 1df-c&lt;sup&gt;1&lt;/sup&gt;, ldfp-c&lt;sup&gt;1&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>GR0</td>
<td>none</td>
<td>none</td>
</tr>
<tr>
<td>GR%, % in 1 - 127</td>
<td>ld-c&lt;sup&gt;1&lt;/sup&gt;, gr-writers&lt;sup&gt;1&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>IBR#</td>
<td>mov-to-IND-IBR&lt;sup&gt;3&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>InService*</td>
<td>mov-to-CR-EOI, mov-from-CR-IVR</td>
<td>SC</td>
</tr>
<tr>
<td>IP</td>
<td>all</td>
<td>none</td>
</tr>
<tr>
<td>ITC</td>
<td>ptc.e, ptc.g, ptc.ga, ptc.l, ptr.i, ptr.d</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>ptc.e, ptc.g, ptc.ga, ptc.l, ptr.i, ptr.d, itc.i, itc.d, itr.i, itr.d</td>
<td>impliedF</td>
</tr>
<tr>
<td>ITR</td>
<td>itr.i</td>
<td>itr.i, ptr.i</td>
</tr>
<tr>
<td></td>
<td>ptr.i</td>
<td>none</td>
</tr>
<tr>
<td>memory</td>
<td>mem-writers</td>
<td>none</td>
</tr>
<tr>
<td>PKR#</td>
<td>mov-to-IND-PKR&lt;sup&gt;3&lt;/sup&gt;</td>
<td>mov-to-IND-PKR&lt;sup&gt;4&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>mov-to-IND-PKR&lt;sup&gt;3&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>PMC#</td>
<td>mov-to-IND-PMC&lt;sup&gt;3&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>PMD#</td>
<td>mov-to-IND-PMD&lt;sup&gt;3&lt;/sup&gt;</td>
<td>impliedF</td>
</tr>
<tr>
<td>PR0</td>
<td>pr-writers&lt;sup&gt;1&lt;/sup&gt;</td>
<td>none</td>
</tr>
<tr>
<td>PR%, % in 1 - 15</td>
<td>pr-and-writers&lt;sup&gt;1&lt;/sup&gt;</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>pr-or-writers&lt;sup&gt;1&lt;/sup&gt;</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>pr-unc-writers-fp&lt;sup&gt;1&lt;/sup&gt;</td>
<td>pr-unc-writers-fp&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>pr-unc-writers-int&lt;sup&gt;1&lt;/sup&gt;</td>
<td>pr-unc-writers-int&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>pr-norm-writers-fp&lt;sup&gt;1&lt;/sup&gt;</td>
<td>pr-norm-writers-fp&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>pr-norm-writers-int&lt;sup&gt;1&lt;/sup&gt;</td>
<td>pr-norm-writers-int&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>pr-and-writers&lt;sup&gt;1&lt;/sup&gt;</td>
<td>pr-and-writers&lt;sup&gt;1&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>mov-to-PR-allreg&lt;sup&gt;7&lt;/sup&gt;</td>
<td>mov-to-PR-allreg&lt;sup&gt;7&lt;/sup&gt;</td>
</tr>
</tbody>
</table>
Table 5-3. WAW Dependencies Organized by Resource (Continued)

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Writers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>PR%*, % in 16 - 62</td>
<td>pr-and-writers¹</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>pr-or-writers¹</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>pr-unc-writers-fp¹</td>
<td>pr-unc-writers-fp¹</td>
</tr>
<tr>
<td></td>
<td>pr-unc-writers-int¹</td>
<td>pr-unc-writers-int¹</td>
</tr>
<tr>
<td></td>
<td>pr-norm-writers-fp¹</td>
<td>pr-norm-writers-fp¹</td>
</tr>
<tr>
<td></td>
<td>pr-norm-writers-int¹</td>
<td>pr-norm-writers-int¹</td>
</tr>
<tr>
<td></td>
<td>pr-and-writers¹</td>
<td>pr-or-writers¹</td>
</tr>
<tr>
<td></td>
<td>mov-to-PR-allreg⁷</td>
<td>mov-to-PR-allreg⁷</td>
</tr>
<tr>
<td></td>
<td>mov-to-PR-rotreg</td>
<td>mov-to-PR-rotreg</td>
</tr>
<tr>
<td>PR63</td>
<td>pr-and-writers¹</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>pr-or-writers¹</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>mod-sched-brs,</td>
<td>mod-sched-brs,</td>
</tr>
<tr>
<td></td>
<td>pr-unc-writers-fp¹</td>
<td>pr-unc-writers-fp¹</td>
</tr>
<tr>
<td></td>
<td>pr-unc-writers-int¹</td>
<td>pr-unc-writers-int¹</td>
</tr>
<tr>
<td></td>
<td>pr-norm-writers-fp¹</td>
<td>pr-norm-writers-fp¹</td>
</tr>
<tr>
<td></td>
<td>pr-norm-writers-int¹</td>
<td>pr-norm-writers-int¹</td>
</tr>
<tr>
<td></td>
<td>pr-and-writers¹</td>
<td>pr-or-writers¹</td>
</tr>
<tr>
<td></td>
<td>mov-to-PR-allreg⁷</td>
<td>mov-to-PR-allreg⁷</td>
</tr>
<tr>
<td></td>
<td>mov-to-PR-rotreg</td>
<td>mov-to-PR-rotreg</td>
</tr>
<tr>
<td>PSR.ac</td>
<td>user-mask-writers-partial⁷, mov-to-PSR-um, sys-mask-writers-partial⁷, mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.be</td>
<td>user-mask-writers-partial⁷, mov-to-PSR-um, sys-mask-writers-partial⁷, mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.bn</td>
<td>bsw, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.cpl</td>
<td>epc, br.ret, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.da</td>
<td>rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.db</td>
<td>mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.dd</td>
<td>rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.dfh</td>
<td>sys-mask-writers-partial⁷, mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSRdff</td>
<td>sys-mask-writers-partial⁷, mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.di</td>
<td>sys-mask-writers-partial⁷, mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.dt</td>
<td>sys-mask-writers-partial⁷, mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.ed</td>
<td>rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.i</td>
<td>sys-mask-writers-partial⁷, mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.ia</td>
<td>rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.ic</td>
<td>sys-mask-writers-partial⁷, mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.id</td>
<td>rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.is</td>
<td>br.ia, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.it</td>
<td>rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.lp</td>
<td>mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.mc</td>
<td>rfi</td>
<td>impliedF</td>
</tr>
<tr>
<td>PSR.mfh</td>
<td>fr-writers⁹</td>
<td>none</td>
</tr>
<tr>
<td></td>
<td>user-mask-writers-partial⁷, mov-to-PSR-um, sys-mask-writers-partial⁷, mov-to-PSR-I, rfi</td>
<td>impliedF</td>
</tr>
</tbody>
</table>

"Volume 3: Resource and Dependency Semantics" 3:349
5.3.4 WAR Dependency Table

A general rule specific to the WAR table:

1. WAR dependencies are always allowed within instruction groups except for the entry in Table 5-4 below. The readers and subsequent writers specified must be separated by a stop in order to have defined behavior.

Table 5-4. WAR Dependencies Organized by Resource

<table>
<thead>
<tr>
<th>Resource Name</th>
<th>Readers</th>
<th>Writers</th>
<th>Semantics of Dependency</th>
</tr>
</thead>
<tbody>
<tr>
<td>PR63</td>
<td>pr-readers-br\textsuperscript{1}</td>
<td>mod-sched-brs</td>
<td>stop</td>
</tr>
</tbody>
</table>

5.3.5 Listing of Rules Referenced in Dependency Tables

The following rules restrict the specific instances in which some of the instructions in the tables cause a dependency and must be applied where referenced to correctly interpret those entries. Rules only apply to the instance of the instruction class, or instruction mnemonic prefix where the rule is referenced as a superscript. If the rule is referenced in Table 5-5 where instruction classes are defined, then it applies to all instances of the instruction class.

Rule 1. These instructions only write a register when that register’s number is explicitly encoded as a target of the instruction and is only read when it is encoded as a source of the instruction (or encoded as its PR[qp]).

Rule 2. These instructions only read CFM when they access a rotating GR, FR, or PR. mov-to-PR and mov-from-PR only access CFM when their qualifying predicate is in the rotating region.
Rule 3. These instructions use a general register value to determine the specific indirect register accessed. These instructions only access the register resource specified by the value in bits \(7:0\) of the dynamic value of the index register.

Rule 4. These instructions only read the given resource when bits \(7:0\) of the indirect index register value does not match the register number of the resource.

Rule 5. All rules are implementation specific.

Rule 6. There is a dependency only when both the index specified by the reader and the index specified by the writer have the same value in bits \(63:61\).

Rule 7. These instructions access the specified resource only when the corresponding mask bit is set.

Rule 8. PSR.dtpf is only read when these instructions reference FR32-127. PSR.dfl is only read when these instructions reference FR2-31.

Rule 9. PSR.mfl is only written when these instructions write FR2-31. PSR.mfh is only written when these instructions write FR32-127.

Rule 10. The PSR.bn bit is only accessed when one of GR16-31 is specified in the instruction.

Rule 11. The target predicates are written independently of PR[qp], but source registers are only read if PR[qp] is true.

Rule 12. This instruction only reads the specified predicate register when that register is the PR[qp].

Rule 13. This reference to ld-c only applies to the GR whose value is loaded with data returned from memory, not the post-incremented address register. Thus, a stop is still required between a post-incrementing ld-c and a consumer that reads the post-incremented GR.

Rule 14. The RSE resource includes implementation-specific internal state. At least one (and possibly more) of these resources are read by each instruction listed in the rse-readers class. At least one (and possibly more) of these resources are written by each instruction listed in the rse-writers class. To determine exactly which instructions read or write each individual resource, see the corresponding instruction pages.

Rule 15. This class represents all instructions marked as Reserved if PR[qp] is 1 B-type instructions as described in “Format Summary” on page 3:256.

Rule 16. This class represents all instructions marked as Reserved if PR[qp] is 1 instructions as described in “Format Summary” on page 3:256.
### 5.4 Support Tables

**Table 5-5. Instruction Classes**

<table>
<thead>
<tr>
<th>Class</th>
<th>Events/Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>all</td>
<td>predicatable-instructions, unpredicatable-instructions</td>
</tr>
<tr>
<td>branches</td>
<td>indirect-brs, ip-rel-brs</td>
</tr>
<tr>
<td>cfm-readers</td>
<td>fr-readers, fr-writers, gr-readers, gr-writers, mod-sched-brs,</td>
</tr>
<tr>
<td></td>
<td>predicatable-instructions, pr-writers, alloc, br.call, brl.call, br.ret, cover, loadrs, rfi, chk-a, invala.e</td>
</tr>
<tr>
<td>chk-a</td>
<td>chk.a.clr, chk.a.nc</td>
</tr>
<tr>
<td>cmpxchg</td>
<td>cmpxchg1, cmpxchg2, cmpxchg4, cmpxchg8, cmp8xchg16</td>
</tr>
<tr>
<td>czx</td>
<td>czx1, czx2</td>
</tr>
<tr>
<td>fcmp-s0</td>
<td>fcmp[Field(sf)==s0]</td>
</tr>
<tr>
<td>fcmp-s1</td>
<td>fcmp[Field(sf)==s1]</td>
</tr>
<tr>
<td>fcmp-s2</td>
<td>fcmp[Field(sf)==s2]</td>
</tr>
<tr>
<td>fcmp-s3</td>
<td>fcmp[Field(sf)==s3]</td>
</tr>
<tr>
<td>fetchadd</td>
<td>fetchadd4, fetchadd8</td>
</tr>
<tr>
<td>fp-arith</td>
<td>fadd, famax, famin, fcvt.fx, fcvt.fux, fcvt.xuf, fma, fmax, fmin, fmpy, fms, fnma, fnmcp, fnmpy, fnorm, fpmx, fpmin, fpfms, fpmx, fnma, fpmnp, fnmpy, fprcpa, fprcta, frcpa, frsqrta, fsub</td>
</tr>
<tr>
<td></td>
<td>fp-arith-s0, fp-arith-s1, fp-arith-s2, fp-arith-s3</td>
</tr>
<tr>
<td>fp-non-arith</td>
<td>fabs, fand, fandcm, fclass, fcvt.xf, fmerge, fnix, fneg, fnegabs, for, fpabs, fmerge, fpack, fneg, fnegabs, fselect, fswap, fsxt, fxor, xma</td>
</tr>
<tr>
<td></td>
<td>fpcmp-s0, fpcmp-s1, fpcmp-s2, fpcmp-s3</td>
</tr>
<tr>
<td>fr-readers</td>
<td>fp-arith, fp-non-arith, pr-writers-fp, chk.a[Format in {M21}], getf</td>
</tr>
<tr>
<td>fr-writers</td>
<td>fp-arith, fp-non-arith, gr-readers-writers-fp, mem-readers-fp, setf</td>
</tr>
<tr>
<td>gr-readers</td>
<td>gr-readers-writers, mem-readers, mem-writers, chk.s, cmp, cmp4, fc, ilc.i, ilc.d, ilr.i, ilr.d, mov-to-AR-gr, mov-to-BR, mov-to-CR, mov-to-IND, mov-from-IND, mov-to-PR-allreg, mov-to-PSR-I, mov-to-PSR-um, probe-all, ptc.e, ptc.g, ptc.ga, ptc.l, ptr.i, ptr.d, setf, tbit, trtl</td>
</tr>
<tr>
<td>gr-readers-writers</td>
<td>mov-to-IND, add, addi, adddp4, adds, and, andcm, czx, dep</td>
</tr>
<tr>
<td>gr-writers</td>
<td>alloc, dep, getf, gr-readers-writers, mem-readers-int, mov-to-AR, mov-to-BR, mov-to-PR, mov-to-PSR, mov-to-PSR-um, mov-ip, movl</td>
</tr>
<tr>
<td>indirect-bp</td>
<td>brp[Format in {B7}]</td>
</tr>
<tr>
<td>indirect-brs</td>
<td>br.call[Format in {B6}], br.cond[Format in {B4}], br.i, br.ret</td>
</tr>
<tr>
<td>invala-all</td>
<td>invala[Format in {M24}], invala.e</td>
</tr>
<tr>
<td>ip-rel-brs</td>
<td>mod-sched-brs, br.call[Format in {B3}], br.call, brl.call, brl.cond, br.cond[Format in {B1}], br.cloop</td>
</tr>
<tr>
<td>ld</td>
<td>ld1, ld2, ld4, ld8, ld8.fill, ld16</td>
</tr>
<tr>
<td>ld-a</td>
<td>ld1.a, ld2.a, ld4.a, ld8.a</td>
</tr>
<tr>
<td>ld-all-postinc</td>
<td>ld[Format in {M2 M3}], ldfp[Format in {M12}], ld[Format in {M7 M8}]</td>
</tr>
<tr>
<td>ld-c</td>
<td>ld-c-nc, ld-c-clr</td>
</tr>
</tbody>
</table>
Table 5-5. Instruction Classes (Continued)

<table>
<thead>
<tr>
<th>Class</th>
<th>Events/Instructions</th>
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<tr>
<td>ld-c-clr</td>
<td>ld1.c.clr, ld2.c.clr, ld4.c.clr, ld8.c.clr, ld-c-clr-acq</td>
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<td>ld1.sa, ld2.sa, ld4.sa, ld8.sa</td>
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<td>ldfs, ldfd, ldfe, ld8, ld.fili</td>
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<td>ld-f-c-nc, ld-f-c-clr</td>
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<td>ld-fp-sa</td>
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<td>lfetch-all</td>
<td>lfetch</td>
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<td>lfetch-fault</td>
<td>lfetch[Field(lftype)==fault]</td>
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<td>lfetch-nofault</td>
<td>lfetch[Field(lftype)==]</td>
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<td>lfetch-postinc</td>
<td>lfetch[Format in { M14 M15}]</td>
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<td>mem-readers-fp, mem-readers-int</td>
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<td>mem-readers-alat</td>
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<td>mix1, mix2, mix4</td>
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<td>br.cexil, br.ctop, br.wexil, br.wtop</td>
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<td>mod-sched-brs-counted</td>
<td>br.cexil, br.cloop, br.ctop</td>
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<td>mov-from-AR-BSP</td>
<td>mov-from-AR-M[Field(ar3) == BSP]</td>
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<td>mov-from-AR-BSPSTORE</td>
<td>mov-from-AR-M[Field(ar3) == BSPSTORE]</td>
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<td>mov-from-AR-M[Field(ar3) == CCV]</td>
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<td>mov-from-AR-M[Field(ar3) == CFLG]</td>
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<td>mov-from-AR-M[Field(ar3) == CSD]</td>
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<td>mov-from-AR-M[Field(ar3) == EC]</td>
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<td>mov-from-AR-M[Field(ar3) == EFLAG]</td>
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<td>mov-from-AR-FCR</td>
<td>mov-from-AR-M[Field(ar3) == FCR]</td>
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<td>mov-from-AR-FDR</td>
<td>mov-from-AR-M[Field(ar3) == FDR]</td>
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<td>mov-from-AR-FIR</td>
<td>mov-from-AR-M[Field(ar3) == FIR]</td>
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<td>mov-from-AR-FPSR</td>
<td>mov-from-AR-M[Field(ar3) == FPSR]</td>
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<tr>
<td>mov-from-AR-FSR</td>
<td>mov-from-AR-M[Field(ar3) == FSR]</td>
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Table 5-5. Instruction Classes (Continued)

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<th>Events/Instructions</th>
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<td>mov-from-AR-I</td>
<td>mov_ar[Format in {I28}]</td>
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<td>mov-from-AR-ig</td>
<td>mov-from-AR-IM[Field(ar3) in {48-63 112-127}]</td>
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<td>mov-from-AR-IM</td>
<td>mov_ar[Format in {I28 M31}]</td>
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<td>mov-from-AR-ITC</td>
<td>mov-from-AR-M[Field(ar3) == ITC]</td>
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<td>mov-from-AR-K</td>
<td>mov-from-AR-M[Field(ar3) in {K0 K1 K2 K3 K4 K5 K6 K7}]</td>
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<tr>
<td>mov-from-AR-LC</td>
<td>mov-from-AR-I[Field(ar3) == LC]</td>
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<td>mov-from-AR-M</td>
<td>mov_ar[Format in {M31}]</td>
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<td>mov-from-AR-PFS</td>
<td>mov-from-AR-I[Field(ar3) == PFS]</td>
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<tr>
<td>mov-from-AR-RNAT</td>
<td>mov-from-AR-M[Field(ar3) == RNAT]</td>
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<tr>
<td>mov-from-AR-RSC</td>
<td>mov-from-AR-M[Field(ar3) == RSC]</td>
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<tr>
<td>mov-from-AR-rv</td>
<td>none</td>
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<tr>
<td>mov-from-AR-SSD</td>
<td>mov-from-AR-M[Field(ar3) == SSD]</td>
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<td>mov-from-AR-UNAT</td>
<td>mov-from-AR-M[Field(ar3) == UNAT]</td>
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<td>mov-from-BR</td>
<td>mov_br[Format in {I22}]</td>
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<td>mov-from-CR</td>
<td>mov_cr[Format in {M33}]</td>
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<td>mov-from-CR-CMCV</td>
<td>mov-from-CR[Field(cr3) == CMCV]</td>
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<td>mov-from-CR-DCR</td>
<td>mov-from-CR[Field(cr3) == DCR]</td>
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<tr>
<td>mov-from-CR-EOI</td>
<td>mov-from-CR[Field(cr3) == EOI]</td>
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<tr>
<td>mov-from-CR-GPTA</td>
<td>mov-from-CR[Field(cr3) == GPTA]</td>
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<tr>
<td>mov-from-CR-IFA</td>
<td>mov-from-CR[Field(cr3) == IFA]</td>
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<tr>
<td>mov-from-CR-IFS</td>
<td>mov-from-CR[Field(cr3) == IFS]</td>
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<td>mov-from-CR-IHA</td>
<td>mov-from-CR[Field(cr3) == IHA]</td>
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<tr>
<td>mov-from-CR-IIM</td>
<td>mov-from-CR[Field(cr3) == IIM]</td>
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<td>mov-from-CR-IIP</td>
<td>mov-from-CR[Field(cr3) == IIP]</td>
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<tr>
<td>mov-from-CR-IIPA</td>
<td>mov-from-CR[Field(cr3) == IIPA]</td>
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<tr>
<td>mov-from-CR-IPSR</td>
<td>mov-from-CR[Field(cr3) == IPSR]</td>
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<tr>
<td>mov-from-CR-IRR</td>
<td>mov-from-CR[Field(cr3) in {IRR0 IRR1 IRR2 IRR3}]</td>
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<td>mov-from-CR-ISR</td>
<td>mov-from-CR[Field(cr3) == ISR]</td>
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<td>mov-from-CR-ITIR</td>
<td>mov-from-CR[Field(cr3) == ITIR]</td>
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<td>mov-from-CR-ITM</td>
<td>mov-from-CR[Field(cr3) == ITM]</td>
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<td>mov-from-CR-IVR</td>
<td>mov-from-CR[Field(cr3) == IVR]</td>
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<td>mov-from-CR-LID</td>
<td>mov-from-CR[Field(cr3) == LID]</td>
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<tr>
<td>mov-from-CR-LRR</td>
<td>mov-from-CR[Field(cr3) in {LRR0 LRR1}]</td>
</tr>
<tr>
<td>mov-from-CR-PMV</td>
<td>mov-from-CR[Field(cr3) == PMV]</td>
</tr>
<tr>
<td>mov-from-CR-PTA</td>
<td>mov-from-CR[Field(cr3) == PTA]</td>
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<tr>
<td>mov-from-CR-rv</td>
<td>none</td>
</tr>
<tr>
<td>mov-from-CR-TPR</td>
<td>mov-from-CR[Field(cr3) == TPR]</td>
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<td>mov-from-IND</td>
<td>mov_indirect[Format in {M43}]</td>
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<tr>
<td>mov-from-IND-CPUID</td>
<td>mov-from-IND[Field(reg) == cpuid]</td>
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<tr>
<td>mov-from-IND-DBR</td>
<td>mov-from-IND[Field(reg) == dbr]</td>
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<tr>
<td>mov-from-IND-IBR</td>
<td>mov-from-IND[Field(reg) == ibr]</td>
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<tr>
<td>mov-from-IND-PKR</td>
<td>mov-from-IND[Field(reg) == pkr]</td>
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<tr>
<td>mov-from-IND-PMC</td>
<td>mov-from-IND[Field(reg) == pmc]</td>
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<tr>
<td>mov-from-IND-PMD</td>
<td>mov-from-IND[Field(reg) == pmd]</td>
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<tr>
<td>mov-from-IND-priv</td>
<td>mov-from-IND[Field(reg) in {dbr ibr pkr pmc rr}]</td>
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</table>
### Table 5-5. Instruction Classes (Continued)

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<tr>
<th>Class</th>
<th>Events/Instructions</th>
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<td>mov-from-IND-RR</td>
<td>mov-from-IND[Field(reg) == rr]</td>
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<td>mov-from-PR</td>
<td>mov_.pr[Format in {I25}]</td>
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<td>mov-from-PSR</td>
<td>mov_.psr[Format in {M36}]</td>
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<tr>
<td>mov-from-PSR-um</td>
<td>mov_.um[Format in {M36}]</td>
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<td>mov-ip</td>
<td>mov_.ip[Format in {I25}]</td>
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<td>mov-to-AR</td>
<td>mov-to-AR-M, mov-to-AR-I</td>
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<td>mov-to-AR-BSP</td>
<td>mov-to-AR-M[Field(ar3) == BSP]</td>
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<td>mov-to-AR-BSPSTORE</td>
<td>mov-to-AR-M[Field(ar3) == BSPSTORE]</td>
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<td>mov-to-AR-M[Field(ar3) == CSD]</td>
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<td>mov-to-AR-gr</td>
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<td>mov_ar[Format in {I26 I27}]</td>
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<td>mov_ar[Format in {I26 I27 M29 M30}]</td>
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<td>mov-to-CR[Field(cr3) in {IRR0 IRR1 IRR2 IRR3}]</td>
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<td>mov-to-CR[Field(cr3) in {LRR0, LRR1}]</td>
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<td>mov-to-CR[Field(cr3) == PMV]</td>
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<td>mov-to-CR[Field(cr3) == PTA]</td>
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<td>mov-to-CR[Field(cr3) == TPR]</td>
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<td>mov-to-IND[Field(reg) == rr]</td>
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<td>mov-to-PR-allreg, mov_to-PR-rotreg</td>
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<td>mov_pr[Format in {I23}]</td>
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<td>mov_pr[Format in {I24}]</td>
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<td>mov_psr[Field in {M35}]</td>
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<tr>
<td>padd</td>
<td>padd1, padd2, padd4</td>
</tr>
<tr>
<td>pavg</td>
<td>pavg1, pavg2</td>
</tr>
<tr>
<td>pavgsub</td>
<td>pavgsub1, pavgsub2</td>
</tr>
<tr>
<td>pcmp</td>
<td>pcmp1, pcmp2, pcmp4</td>
</tr>
<tr>
<td>pmax</td>
<td>pmax1, pmax2</td>
</tr>
<tr>
<td>pmin</td>
<td>pmin1, pmin2</td>
</tr>
<tr>
<td>pmpy</td>
<td>pmpy2</td>
</tr>
<tr>
<td>pmpyshr</td>
<td>pmpyshr2</td>
</tr>
<tr>
<td>pr-and-writers</td>
<td>pr-gen-direct-writers-int[Field(ctype) in {and, andcm}],</td>
</tr>
<tr>
<td></td>
<td>pr-gen-direct-writers-int[Field(ctype) in {or, orcm}]</td>
</tr>
<tr>
<td>pr-gen-writers-fp</td>
<td>fclass, fcmp</td>
</tr>
<tr>
<td>pr-gen-writers-fp</td>
<td>pr-gen-writers-fp[Field(ctype) in {and, andcm}],</td>
</tr>
<tr>
<td>pr-gen-writers-fp</td>
<td>pr-gen-writers-fp[Field(ctype) in {or, orcm}]</td>
</tr>
<tr>
<td>pr-norm-writers-int</td>
<td>pr-gen-direct-writers-fp[Field(ctype) in {and, andcm}],</td>
</tr>
<tr>
<td>pr-norm-writers-int</td>
<td>pr-gen-direct-writers-fp[Field(ctype) in {or, orcm}]</td>
</tr>
<tr>
<td>pr-or-writers</td>
<td>pr-gen-writers-int[Field(ctype) in {or, orcm}]</td>
</tr>
<tr>
<td>pr-readers-br</td>
<td>br.call, br.cond, bcall, bret, btop, break.b, nop.b, ReservedBQP</td>
</tr>
</tbody>
</table>
### Table 5-5. Instruction Classes (Continued)

<table>
<thead>
<tr>
<th>Class</th>
<th>Events/Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>pr-unc-writers-fp</td>
<td>pr-gen-writers-fp[Field(ctype)==unc]11, fprcpa11, fprsqrta11, frcpa11, frsqrta11</td>
</tr>
<tr>
<td>pr-unc-writers-int</td>
<td>pr-gen-writers-int[Field(ctype)==unc]11</td>
</tr>
<tr>
<td>pr-writers</td>
<td>pr-writers-fp, pr-writers-int</td>
</tr>
<tr>
<td>pr-writers-fp</td>
<td>pr-gen-writers-fp, pr-unc-writers-fp</td>
</tr>
<tr>
<td>pr-writers-int</td>
<td>pr-gen-writers-int, pr-unc-writers-int, pr-and-writers, pr-or-writers</td>
</tr>
<tr>
<td>predicable-instructions</td>
<td>mov-from-PR, mov-to-PR, pr-readers-br, pr-readers-nobr-nomovpr</td>
</tr>
<tr>
<td>probe-all</td>
<td>probe-fault, probe-nofault</td>
</tr>
<tr>
<td>probe-fault</td>
<td>probe[Format in {M40}]</td>
</tr>
<tr>
<td>probe-nofault</td>
<td>probe[Format in {M38 M39}]</td>
</tr>
<tr>
<td>psad</td>
<td>psad1</td>
</tr>
<tr>
<td>pshl</td>
<td>pshl2, pshl4</td>
</tr>
<tr>
<td>pshladd</td>
<td>pshladd2</td>
</tr>
<tr>
<td>pshr</td>
<td>pshr2, pshr4</td>
</tr>
<tr>
<td>pshrad</td>
<td>pshrad2</td>
</tr>
<tr>
<td>psub</td>
<td>psub1, psub2, psub4</td>
</tr>
<tr>
<td>ReservedBQP</td>
<td>-15</td>
</tr>
<tr>
<td>ReservedQP</td>
<td>-16</td>
</tr>
<tr>
<td>rse-readers</td>
<td>alloc, br.call, br.ia, br.ret, bret, cover, flushrs, loadrs, mov-from-AR-BSP, mov-from-AR-RNAT, mov-from-AR-BSPTSTORE, mov-to-AR-BSPTSTORE, mov-from-AR-RNAT, mov-to-AR-BSPTSTORE, rfi</td>
</tr>
<tr>
<td>rse-writers</td>
<td>alloc, br.call, br.ia, br.ret, bret, cover, flushrs, loadrs, mov-to-AR-BSPTSTORE, rfi</td>
</tr>
<tr>
<td>st</td>
<td>s1, s2, s4, s8, st8, sp, st16</td>
</tr>
<tr>
<td>st-postinc</td>
<td>stf[Format in {M10}], st[Format in {M5}]</td>
</tr>
<tr>
<td>stf</td>
<td>stfs, stfd, stfe, stf8, stf.spill</td>
</tr>
<tr>
<td>sxt</td>
<td>sxt1, sxt2, sxt4</td>
</tr>
<tr>
<td>sys-mask-writers-partial</td>
<td>rum, rum, ssm</td>
</tr>
<tr>
<td>unpack</td>
<td>unpack1, unpack2, unpack3</td>
</tr>
<tr>
<td>unpredicable-instructions</td>
<td>alloc, br.cloop, br.cr, br.cexit, br.ia, brp, bsw, clr.rb, cover, epc, flushrs, loadrs, rfi</td>
</tr>
<tr>
<td>user-mask-writers-partial</td>
<td>rum, rum, ssm</td>
</tr>
<tr>
<td>xchg</td>
<td>xchg1, xchg2, xchg4, xchg8</td>
</tr>
<tr>
<td>zxt</td>
<td>zxt1, zxt2, zxt4</td>
</tr>
</tbody>
</table>
Part II: IA-32 Instruction Set Descriptions
This section lists all IA-32 instructions and their behavior in the Itanium System Environment and IA-32 System Environments on a processor based on the Itanium architecture. Unless noted otherwise all IA-32 and MMX and Streaming SIMD Extension instructions operate as defined in the *IA-32 Intel® Architecture Software Developer’s Manual*.

This volume describes the complete IA-32 architecture instruction set, including the integer, floating-point, MMX technology and Streaming SIMD Extension technology, and system instructions. The instruction descriptions are arranged in alphabetical order. For each instruction, the forms are given for each operand combination, including the opcode, operands required, and a description. Also given for each instruction are a description of the instruction and its operands, an operational description, a description of the effect of the instructions on flags in the EFLAGS register, and a summary of the exceptions that can be generated.

For all IA-32 the following relationships hold:

- **Writes** – Writes of any IA-32 general purpose, floating-point or Streaming SIMD Extension, MMX technology registers by IA-32 instructions are reflected in the Itanium registers defined to hold that IA-32 state when IA-32 instruction set completes execution.

- **Reads** – Reads of any IA-32 general purpose, floating-point or Streaming SIMD Extension, MMX technology registers by IA-32 instructions see the state of the Itanium registers defined to hold the IA-32 state after entering the IA-32 instruction set.

- **State mappings** – IA-32 numeric instructions are controlled by and reflect their status in FCW, FSW, FTW, FCS, FIP, FOP, FDS and FEA. On exit from the IA-32 instruction set, Itanium numeric status and control resources defined to hold IA-32 state reflect the results of all IA-32 prior numeric instructions in FCR, FSR, FIR and FDR. Itanium numeric status and control resources defined to hold IA-32 state are honored by IA-32 numeric instructions when entering the IA-32 instruction set.

### 1.1 Additional Intel® Itanium® Faults

The following fault behavior is defined for all IA-32 instructions in the Itanium System Environment:

- **IA-32 Faults** – All IA-32 faults are performed as defined in the *IA-32 Intel® Architecture Software Developer’s Manual*, unless otherwise noted. IA-32 faults are delivered on the IA-32_Exception interruption vector.

- **IA-32 GPFault** – Null segments are signified by the segment descriptor register’s P-bit being set to zero. IA-32 memory references through DSD, ESD, FSD, and GSD with the P-bit set to zero result in an IA-32 GPFault.

- **Itanium Low FP Reg Fault** – If PSR.dfl is 1, execution of any IA-32 MMX technology, Streaming SIMD Extension or floating-point instructions results in a Disabled FP Register fault (regardless of whether FR2-31 is referenced).
• **Itanium High FP Reg Fault** – If PSR.dfh is 1, execution of the first target IA-32 instruction following an br.ia or rfi results in a Disabled FP Register fault (regardless of whether FR32-127 is referenced).

• **Itanium Instruction Mem Faults** – The following additional Itanium memory faults can be generated on each virtual page referenced when fetching IA-32 or MMX or Streaming SIMD Extension instructions for execution:
  - Alternative instruction TLB fault
  - VHPT instruction fault
  - Instruction TLB fault
  - Instruction Page Not Present fault
  - Instruction NaT Page Consumption Abort
  - Instruction Key Miss fault
  - Instruction Key Permission fault
  - Instruction Access Rights fault
  - Instruction Access Bit fault

• **Itanium Data Mem Faults** – The following additional Itanium memory faults can be generated on each virtual page touched when reading or writing memory operands from the IA-32 instruction set including MMX and Streaming SIMD Extension instructions:
  - Nested TLB fault
  - Alternative data TLB fault
  - VHPT data fault
  - Data TLB fault
  - Data Page Not Present fault
  - Data NaT Page Consumption Abort
  - Data Key Miss fault
  - Data Key Permission fault
  - Data Access Rights fault
  - Data Dirty bit fault
  - Data Access bit fault

### 1.2 Interpreting the IA-32 Instruction Reference Pages

This section describes the information contained in the various sections of the instruction reference pages that make up the majority of this chapter. It also explains the notational conventions and abbreviations used in these sections.

#### 1.2.1 IA-32 Instruction Format

The following is an example of the format used for each Intel architecture instruction description in this chapter.
CMC—Complement Carry Flag

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F5</td>
<td>CMC</td>
<td>Complement carry flag</td>
</tr>
</tbody>
</table>

### 1.2.1.1 Opcode Column

The “Opcode” column gives the complete object code produced for each form of the instruction. When possible, the codes are given as hexadecimal bytes, in the same order in which they appear in memory. Definitions of entries other than hexadecimal bytes are as follows:

- `/digit` – A digit between 0 and 7 indicates that the ModR/M byte of the instruction uses only the r/m (register or memory) operand. The reg field contains the digit that provides an extension to the instruction's opcode.
- `/r` – Indicates that the ModR/M byte of the instruction contains both a register operand and an r/m operand.
- `cb, cw, cd, cp` – A 1-byte (cb), 2-byte (cw), 4-byte (cd), or 6-byte (cp) value following the opcode that is used to specify a code offset and possibly a new value for the code segment register.
- `ib, iw, id` – A 1-byte (ib), 2-byte (iw), or 4-byte (id) immediate operand to the instruction that follows the opcode, ModR/M bytes or scale-indexing bytes. The opcode determines if the operand is a signed value. All words and doublewords are given with the low-order byte first.
- `+rb, +rw, +rd` – A register code, from 0 through 7, added to the hexadecimal byte given at the left of the plus sign to form a single opcode byte. The register codes are given in Table 1-1.
- `/i` – A number used in floating-point instructions when one of the operands is ST(i) from the FPU register stack. The number i (which can range from 0 to 7) is added to the hexadecimal byte given at the left of the plus sign to form a single opcode byte.

### 1.2.1.2 Instruction Column

The “Instruction” column gives the syntax of the instruction statement as it would appear in an ASM386 program. The following is a list of the symbols used to represent operands in the instruction statements:

- `rel8` – A relative address in the range from 128 bytes before the end of the instruction to 127 bytes after the end of the instruction.
- `rel16` and `rel32` – A relative address within the same code segment as the instruction assembled. The rel16 symbol applies to instructions with an operand-size attribute of 16 bits; the rel32 symbol applies to instructions with an operand-size attribute of 32 bits.

#### Table 1-1. Register Encodings Associated with the +rb, +rw, and +rd Nomenclature

<table>
<thead>
<tr>
<th>rb</th>
<th>rw</th>
<th>rd</th>
</tr>
</thead>
<tbody>
<tr>
<td>AL = 0</td>
<td>AX = 0</td>
<td>EAX = 0</td>
</tr>
<tr>
<td>CL = 1</td>
<td>CX = 1</td>
<td>ECX = 1</td>
</tr>
<tr>
<td>DL = 2</td>
<td>DX = 2</td>
<td>EDX = 2</td>
</tr>
<tr>
<td>BL = 3</td>
<td>BX = 3</td>
<td>EBX = 3</td>
</tr>
<tr>
<td>AH = 4</td>
<td>SP = 4</td>
<td>ESP = 4</td>
</tr>
<tr>
<td>CH = 5</td>
<td>BP = 5</td>
<td>EBP = 5</td>
</tr>
<tr>
<td>DH = 6</td>
<td>SI = 6</td>
<td>ESI = 6</td>
</tr>
<tr>
<td>BH = 7</td>
<td>DI = 7</td>
<td>EDI = 7</td>
</tr>
</tbody>
</table>
• **ptr16:16 and ptr16:32** – A far pointer, typically in a code segment different from that of the instruction. The notation _ptr16:16_ indicates that the value of the pointer has two parts. The value to the left of the colon is a 16-bit selector or value destined for the code segment register. The value to the right corresponds to the offset within the destination segment. The _ptr16:16_ symbol is used when the instruction's operand-size attribute is 16 bits; the _ptr16:32_ symbol is used when the operand-size attribute is 32 bits.

• **r8** – One of the byte general-purpose registers AL, CL, DL, BL, AH, CH, DH, or BH.

• **r16** – One of the word general-purpose registers AX, CX, DX, BX, SP, BP, SI, or DI.

• **r32** – One of the doubleword general-purpose registers EAX, ECX, EDX, EBX, ESP, EBP, ESI, or EDI.

• **imm8** – An immediate byte value. The _imm8_ symbol is a signed number between –128 and +127 inclusive. For instructions in which _imm8_ is combined with a word or doubleword operand, the immediate value is sign-extended to form a word or doubleword. The upper byte of the word is filled with the topmost bit of the immediate value.

• **imm16** – An immediate word value used for instructions whose operand-size attribute is 16 bits. This is a number between –32,768 and +32,767 inclusive.

• **imm32** – An immediate doubleword value used for instructions whose operand-size attribute is 32 bits. It allows the use of a number between +2,147,483,647 and –2,147,483,648 inclusive.

• **r/m8** – A byte operand that is either the contents of a byte general-purpose register (AL, BL, CL, DL, AH, BH, CH, and DH), or a byte from memory.

• **r/m16** – A word general-purpose register or memory operand used for instructions whose operand-size attribute is 16 bits. The word general-purpose registers are: AX, BX, CX, DX, SP, BP, SI, and DI. The contents of memory are found at the address provided by the effective address computation.

• **r/m32** – A doubleword general-purpose register or memory operand used for instructions whose operand-size attribute is 32 bits. The doubleword general-purpose registers are: EAX, EBX, ECX, EDX, ESP, EBP, ESI, and EDI. The contents of memory are found at the address provided by the effective address computation.

• **m** – A 16- or 32-bit operand in memory.

• **m8** – A byte operand in memory, usually expressed as a variable or array name, but pointed to by the DS:(E)SI or ES:(E)DI registers. This nomenclature is used only with the string instructions and the XLAT instruction.

• **m16** – A word operand in memory, usually expressed as a variable or array name, but pointed to by the DS:(E)SI or ES:(E)DI registers. This nomenclature is used only with the string instructions.

• **m32** – A doubleword operand in memory, usually expressed as a variable or array name, but pointed to by the DS:(E)SI or ES:(E)DI registers. This nomenclature is used only with the string instructions.

• **m64** – A memory quadword operand in memory. This nomenclature is used only with the CMPXCHG8B instruction.

• **m16:16, m16:32** – A memory operand containing a far pointer composed of two numbers. The number to the left of the colon corresponds to the pointer's segment selector. The number to the right corresponds to its offset.

• **m16&amp;16, m32&amp;32** – A memory operand consisting of data item pairs whose sizes are indicated on the left and the right side of the ampersand. All memory addressing modes are allowed. The m16&amp;16 and m32&amp;32 operands are used by the BOUND instruction to provide
an operand containing an upper and lower bounds for array indices. The m16&32 operand is used by LIDT and LGDT to provide a word with which to load the limit field, and a doubleword with which to load the base field of the corresponding GDTR and IDTR registers.

- **moffs8, moffs16, moffs32** – A simple memory variable (memory offset) of type byte, word, or doubleword used by some variants of the MOV instruction. The actual address is given by a simple offset relative to the segment base. No ModR/M byte is used in the instruction. The number shown with moffs indicates its size, which is determined by the address-size attribute of the instruction.

- **Sreg** – A segment register. The segment register bit assignments are ES=0, CS=1, SS=2, DS=3, FS=4, and GS=5.

- **m32real, m64real, m80real** – A single-, double-, and extended-real (respectively) floating-point operand in memory.

- **m16int, m32int, m64int** – A word-, short-, and long-integer (respectively) floating-point operand in memory.

- **ST or ST(0)** – The top element of the FPU register stack.

- **ST(i)** – The i\(^{th}\) element from the top of the FPU register stack. \((i = 0 \text{ through } 7)\).

- **mm** – An MMX technology register. The 64-bit MMX technology registers are: MM0 through MM7.

- **mm/m32** – The low order 32 bits of an MMX technology register or a 32-bit memory operand. The 64-bit MMX technology registers are: MM0 through MM7. The contents of memory are found at the address provided by the effective address computation.

- **mm/m64** – An MMX technology register or a 64-bit memory operand. The 64-bit MMX technology registers are: MM0 through MM7. The contents of memory are found at the address provided by the effective address computation.

### 1.2.1.3 Description Column

The “Description” column following the “Instruction” column briefly explains the various forms of the instruction. The following “Description” and “Operation” sections contain more details of the instruction's operation.

### 1.2.1.4 Description

The “Description” section describes the purpose of the instructions and the required operands. It also discusses the effect of the instruction on flags.

### 1.2.2 Operation

The “Operation” section contains an algorithmic description (written in pseudo-code) of the instruction. The pseudo-code uses a notation similar to the Algol or Pascal language. The algorithms are composed of the following elements:

- Comments are enclosed within the symbol pairs “(*” and “*)”.

- Compound statements are enclosed in keywords, such as IF, THEN, ELSE, and FI for an if statement, DO and OD for a do statement, or CASE... OF and ESAC for a case statement.

- A register name implies the contents of the register. A register name enclosed in brackets implies the contents of the location whose address is contained in that register. For example,
ES:[DI] indicates the contents of the location whose ES segment relative address is in register DI. [SI] indicates the contents of the address contained in register SI relative to SI’s default segment (DS) or overridden segment.

- Parentheses around the “E” in a general-purpose register name, such as (E)SI, indicates that an offset is read from the SI register if the current address-size attribute is 16 or is read from the ESI register if the address-size attribute is 32.
- Brackets are also used for memory operands, where they mean that the contents of the memory location is a segment-relative offset. For example, [SRC] indicates that the contents of the source operand is a segment-relative offset.
- A ← B; indicates that the value of B is assigned to A.
- The symbols =, ≠, ≥, and ≤ are relational operators used to compare two values, meaning equal, not equal, greater or equal, less or equal, respectively. A relational expression such as A = B is TRUE if the value of A is equal to B; otherwise it is FALSE.
- The expression “<< COUNT” and “>> COUNT” indicates that the destination operand should be shifted left or right, respectively, by the number of bits indicated by the count operand.

The following identifiers are used in the algorithmic descriptions:

- **OperandSize and AddressSize** – The OperandSize identifier represents the operand-size attribute of the instruction, which is either 16 or 32 bits. The AddressSize identifier represents the address-size attribute, which is either 16 or 32 bits. For example, the following pseudo-code indicates that the operand-size attribute depends on the form of the CMPS instruction used.

```plaintext
IF instruction = CMPSW
   THEN OperandSize ← 16;
ELSE
   IF instruction = CMPSD
      THEN OperandSize ← 32;
   FI;
FI;
```

See “Operand-Size and Address-Size Attributes” in Chapter 3 of the *IA-32 Intel® Architecture Software Developer’s Manual, Volume 1*, for general guidelines on how these attributes are determined.

- **StackAddrSize** – Represents the stack address-size attribute associated with the instruction, which has a value of 16 or 32 bits (see “Address-Size Attribute for Stack” in Chapter 4 of the *IA-32 Intel® Architecture Software Developer’s Manual, Volume 1*).

- **SRC** – Represents the source operand.

- **DEST** – Represents the destination operand.

The following functions are used in the algorithmic descriptions:

- **ZeroExtend(value)** – Returns a value zero-extended to the operand-size attribute of the instruction. For example, if the operand-size attribute is 32, zero extending a byte value of –10 converts the byte from F6H to a doubleword value of 000000F6H. If the value passed to the ZeroExtend function and the operand-size attribute are the same size, ZeroExtend returns the value unaltered.

- **SignExtend(value)** – Returns a value sign-extended to the operand-size attribute of the instruction. For example, if the operand-size attribute is 32, sign extending a byte containing the value –10 converts the byte from F6H to a doubleword value of FFFFFFF6H. If the value
passed to the SignExtend function and the operand-size attribute are the same size, SignExtend returns the value unaltered.

- **SaturateSignedWordToSignedByte** – Converts a signed 16-bit value to a signed 8-bit value. If the signed 16-bit value is less than \(-128\), it is represented by the saturated value \(-128\) (80H); if it is greater than 127, it is represented by the saturated value 127 (7FH).

- **SaturateSignedDwordToSignedWord** – Converts a signed 32-bit value to a signed 16-bit value. If the signed 32-bit value is less than \(-32768\), it is represented by the saturated value \(-32768\) (8000H); if it is greater than 32767, it is represented by the saturated value 32767 (7FFFH).

- **SaturateSignedWordToUnsignedByte** – Converts a signed 16-bit value to an unsigned 8-bit value. If the signed 16-bit value is less than zero, it is represented by the saturated value zero (00H); if it is greater than 255, it is represented by the saturated value 255 (FFH).

- **SaturateToSignedByte** – Represents the result of an operation as a signed 8-bit value. If the result is less than \(-128\), it is represented by the saturated value \(-128\) (80H); if it is greater than 127, it is represented by the saturated value 127 (7FH).

- **SaturateToSignedWord** – Represents the result of an operation as a signed 16-bit value. If the result is less than \(-32768\), it is represented by the saturated value \(-32768\) (8000H); if it is greater than 32767, it is represented by the saturated value 32767 (7FFFH).

- **SaturateToUnsignedByte** – Represents the result of an operation as a signed 8-bit value. If the result is less than zero it is represented by the saturated value zero (00H); if it is greater than 255, it is represented by the saturated value 255 (FFH).

- **SaturateToUnsignedWord** – Represents the result of an operation as a signed 16-bit value. If the result is less than zero it is represented by the saturated value zero (00H); if it is greater than 65535, it is represented by the saturated value 65535 (FFFFH).

- **LowOrderWord(Dest * Src)** – Multiplies a word operand by a word operand and stores the least significant word of the doubleword result in the destination operand.

- **HighOrderWord(Dest * Src)** – Multiplies a word operand by a word operand and stores the most significant word of the doubleword result in the destination operand.

- **Push(value)** – Pushes a value onto the stack. The number of bytes pushed is determined by the operand-size attribute of the instruction.

- **Pop()** – Removes the value from the top of the stack and returns it. The statement `EAX ← Pop();` assigns to EAX the 32-bit value from the top of the stack. Pop will return either a word or a doubleword depending on the operand-size attribute.

- **PopRegisterStack** – Marks the FPU ST(0) register as empty and increments the FPU register stack pointer (TOP) by 1.

- **Switch-Tasks** – Performs a task switch.

- **Bit(BitBase, BitOffset)** – Returns the value of a bit within a bit string, which is a sequence of bits in memory or a register. Bits are numbered from low-order to high-order within registers and within memory bytes. If the base operand is a register, the offset can be in the range 0..31. This offset addresses a bit within the indicated register. An example, the function `Bit[EAX, 21]` is illustrated in Figure 1-1.

**Figure 1-1. Bit Offset for BIT[EAX,21]**

<table>
<thead>
<tr>
<th>31</th>
<th>21</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>BitOffset = 21</td>
</tr>
</tbody>
</table>
If BitBase is a memory address, BitOffset can range from –2 GBits to 2 GBits. The addressed bit is numbered (Offset MOD 8) within the byte at address (BitBase + (BitOffset DIV 8)), where DIV is signed division with rounding towards negative infinity, and MOD returns a positive number. This operation is illustrated in Figure 1-2.

**Figure 1-2. Memory Bit Indexing**

<table>
<thead>
<tr>
<th>7</th>
<th>5</th>
<th>0</th>
<th>7</th>
<th>0</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BitBase +1</td>
<td>BitBase</td>
<td>BitBase –1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BitOffset = +13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>7</th>
<th>0</th>
<th>7</th>
<th>0</th>
<th>7</th>
<th>5</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>BitBase</td>
<td>BitBase –1</td>
<td>BitBase –2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BitOffset = –11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 1.2.3 Flags Affected

The “Flags Affected” section lists the flags in the EFLAGS register that are affected by the instruction. When a flag is cleared, it is equal to 0; when it is set, it is equal to 1. The arithmetic and logical instructions usually assign values to the status flags in a uniform manner (see Appendix A, EFLAGS Cross-Reference, in the IA-32 Intel® Architecture Software Developer’s Manual, Volume 1). Non-conventional assignments are described in the “Operation” section. The values of flags listed as undefined may be changed by the instruction in an indeterminate manner. Flags that are not listed are unchanged by the instruction.

### 1.2.4 FPU Flags Affected

The floating-point instructions have an “FPU Flags Affected” section that describes how each instruction can affect the four condition code flags of the FPU status word.

### 1.2.5 Protected Mode Exceptions

The “Protected Mode Exceptions” section lists the exceptions that can occur when the instruction is executed in protected mode and the reasons for the exceptions. Each exception is given a mnemonic that consists of a pound sign (#) followed by two letters and an optional error code in parentheses. For example, #GP(0) denotes a general protection exception with an error code of 0. Table 1-2 associates each two-letter mnemonic with the corresponding interrupt vector number and exception name. See Chapter 5, Interrupt and Exception Handling, in the IA-32 Intel® Architecture Software Developer’s Manual, Volume 3, for a detailed description of the exceptions.

Application programmers should consult the documentation provided with their operating systems to determine the actions taken when exceptions occur.
1.2.6 Real-address Mode Exceptions

The “Real-Address Mode Exceptions” section lists the exceptions that can occur when the instruction is executed in real-address mode.

Table 1-2. Exception Mnemonics, Names, and Vector Numbers

<table>
<thead>
<tr>
<th>Vector No.</th>
<th>Mnemonic</th>
<th>Name</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>#DE</td>
<td>Divide Error</td>
<td>DIV and IDIV instructions.</td>
</tr>
<tr>
<td>1</td>
<td>#DB</td>
<td>Debug</td>
<td>Any code or data reference.</td>
</tr>
<tr>
<td>3</td>
<td>#BP</td>
<td>Breakpoint</td>
<td>INT 3 instruction.</td>
</tr>
<tr>
<td>4</td>
<td>#OF</td>
<td>Overflow</td>
<td>INTO instruction.</td>
</tr>
<tr>
<td>5</td>
<td>#BR</td>
<td>BOUND Range Exceeded</td>
<td>BOUND instruction.</td>
</tr>
<tr>
<td>6</td>
<td>#UD</td>
<td>Invalid Opcode (Undefined Opcode)</td>
<td>UD2 instruction or reserved opcode.a</td>
</tr>
<tr>
<td>7</td>
<td>#NM</td>
<td>Device Not Available (No Math Coprocessor)</td>
<td>Floating-point or WAIT/FWAIT instruction.</td>
</tr>
<tr>
<td>8</td>
<td>#DF</td>
<td>Double Fault</td>
<td>Any instruction that can generate an exception, an NMI, or an INTR.</td>
</tr>
<tr>
<td>10</td>
<td>#TS</td>
<td>Invalid TSS</td>
<td>Task switch or TSS access.</td>
</tr>
<tr>
<td>11</td>
<td>#NP</td>
<td>Segment Not Present</td>
<td>Loading segment registers or accessing system segments.</td>
</tr>
<tr>
<td>12</td>
<td>#SS</td>
<td>Stack Segment Fault</td>
<td>Stack operations and SS register loads.</td>
</tr>
<tr>
<td>13</td>
<td>#GP</td>
<td>General Protection</td>
<td>Any memory reference and other protection checks.</td>
</tr>
<tr>
<td>14</td>
<td>#PF</td>
<td>Page Fault</td>
<td>Any memory reference.</td>
</tr>
<tr>
<td>16</td>
<td>#MF</td>
<td>Floating-point Error (Math Fault)</td>
<td>Floating-point or WAIT/FWAIT instruction.</td>
</tr>
<tr>
<td>17</td>
<td>#AC</td>
<td>Alignment Check</td>
<td>Any data reference in memory.b</td>
</tr>
<tr>
<td>18</td>
<td>#MC</td>
<td>Machine Check</td>
<td>Model dependent.c</td>
</tr>
</tbody>
</table>

a. The UD2 instruction was introduced in the Pentium® Pro processor.
b. This exception was introduced in the Intel® 486 processor.
c. This exception was introduced in the Pentium processor and enhanced in the Pentium Pro processor.

1.2.7 Virtual-8086 Mode Exceptions

The “Virtual-8086 Mode Exceptions” section lists the exceptions that can occur when the instruction is executed in virtual-8086 mode.

1.2.8 Floating-point Exceptions

The “Floating-point Exceptions” section lists additional exceptions that can occur when a floating-point instruction is executed in any mode. All of these exception conditions result in a floating-point error exception (#MF, vector number 16) being generated. Table 1-3 associates each one- or two-letter mnemonic with the corresponding exception name. See “Floating-Point Exception Conditions” in Chapter 7 of the IA-32 Intel® Architecture Software Developer’s Manual, Volume 1, for a detailed description of these exceptions.
1.3 IA-32 Base Instruction Reference

The remainder of this chapter provides detailed descriptions of each of the Intel architecture instructions.

Table 1-3. Floating-point Exception Mnemonics and Names

<table>
<thead>
<tr>
<th>Vector No.</th>
<th>Mnemonic</th>
<th>Name</th>
<th>Source</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>#IS</td>
<td>Floating-point invalid operation:</td>
<td>- FPU stack overflow or underflow</td>
</tr>
<tr>
<td>16</td>
<td>#IA</td>
<td></td>
<td>- Invalid FPU arithmetic operation</td>
</tr>
<tr>
<td>16</td>
<td>#Z</td>
<td>Floating-point divide-by-zero</td>
<td>FPU divide-by-zero</td>
</tr>
<tr>
<td>16</td>
<td>#D</td>
<td>Floating-point denormalized operation</td>
<td>Attempting to operate on a denormal number</td>
</tr>
<tr>
<td>16</td>
<td>#O</td>
<td>Floating-point numeric overflow</td>
<td>FPU numeric overflow</td>
</tr>
<tr>
<td>16</td>
<td>#U</td>
<td>Floating-point numeric underflow</td>
<td>FPU numeric underflow</td>
</tr>
<tr>
<td>16</td>
<td>#P</td>
<td>Floating-point inexact result (precision)</td>
<td>Inexact result (precision)</td>
</tr>
</tbody>
</table>
AAA—ASCII Adjust After Addition

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>37</td>
<td>AAA</td>
<td>ASCII adjust AL after addition</td>
</tr>
</tbody>
</table>

**Description**

Adjusts the sum of two unpacked BCD values to create an unpacked BCD result. The AL register is the implied source and destination operand for this instruction. The AAA instruction is only useful when it follows an ADD instruction that adds (binary addition) two unpacked BCD values and stores a byte result in the AL register. The AAA instruction then adjusts the contents of the AL register to contain the correct 1-digit unpacked BCD result.

If the addition produces a decimal carry, the AH register is incremented by 1, and the CF and AF flags are set. If there was no decimal carry, the CF and AF flags are cleared and the AH register is unchanged. In either case, bits 4 through 7 of the AL register are cleared to 0.

**Operation**

IF ((AL AND FH) > 9) OR (AF = 1) THEN
  AL ← (AL + 6);
  AH ← AH + 1;
  AF ← 1;
  CF ← 1;
ELSE
  AF ← 0;
  CF ← 0;
FI;
AL ← AL AND FH;

**Flags Affected**

The AF and CF flags are set to 1 if the adjustment results in a decimal carry; otherwise they are cleared to 0. The OF, SF, ZF, and PF flags are undefined.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults NaT Register Consumption Abort.

**Exceptions (All Operating Modes)**

None.
AAD—ASCII Adjust AX Before Division

Description

Adjusts two unpacked BCD digits (the least-significant digit in the AL register and the most-significant digit in the AH register) so that a division operation performed on the result will yield a correct unpacked BCD value. The AAD instruction is only useful when it precedes a DIV instruction that divides (binary division) the adjusted value in the AL register by an unpacked BCD value.

The AAD instruction sets the value in the AL register to \((AL + (10 \times AH))\), and then clears the AH register to 00H. The value in the AX register is then equal to the binary equivalent of the original unpacked two-digit number in registers AH and AL.

Operation

\[
\begin{align*}
\text{tempAL} & \leftarrow AL; \\
\text{tempAH} & \leftarrow AH; \\
AL & \leftarrow (\text{tempAL} + (\text{tempAH} \times \text{imm8})) \text{ AND FFH}; \\
AH & \leftarrow 0
\end{align*}
\]

The immediate value \((\text{imm8})\) is taken from the second byte of the instruction, which under normal assembly is 0AH (10 decimal). However, this immediate value can be changed to produce a different result.

Flags Affected

The SF, ZF, and PF flags are set according to the result; the OF, AF, and CF flags are undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults NaT Register Consumption Abort.

Exceptions (All Operating Modes)

None.
AAM—ASCII Adjust AX After Multiply

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D4 0A</td>
<td>AAM</td>
<td>ASCII adjust AX after multiply</td>
</tr>
</tbody>
</table>

Description

Adjusts the result of the multiplication of two unpacked BCD values to create a pair of unpacked BCD values. The AX register is the implied source and destination operand for this instruction. The AAM instruction is only useful when it follows an MUL instruction that multiplies (binary multiplication) two unpacked BCD values and stores a word result in the AX register. The AAM instruction then adjusts the contents of the AX register to contain the correct 2-digit unpacked BCD result.

Operation

\[
tempAL \leftarrow AL;  \\
AH \leftarrow tempAL / imm8;  \\
AL \leftarrow tempAL \text{ MOD } imm8;  \\
\]

The immediate value (\(imm8\)) is taken from the second byte of the instruction, which under normal assembly is 0AH (10 decimal). However, this immediate value can be changed to produce a different result.

Flags Affected

The SF, ZF, and PF flags are set according to the result. The OF, AF, and CF flags are undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.

Exceptions (All Operating Modes)

None.
AAS—ASCII Adjust AL After Subtraction

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3F</td>
<td>AAS</td>
<td>ASCII adjust AL after subtraction</td>
</tr>
</tbody>
</table>

**Description**

Adjusts the result of the subtraction of two unpacked BCD values to create a unpacked BCD result. The AL register is the implied source and destination operand for this instruction. The AAS instruction is only useful when it follows a SUB instruction that subtracts (binary subtraction) one unpacked BCD value from another and stores a byte result in the AL register. The AAA instruction then adjusts the contents of the AL register to contain the correct 1-digit unpacked BCD result.

If the subtraction produced a decimal carry, the AH register is decremented by 1, and the CF and AF flags are set. If no decimal carry occurred, the CF and AF flags are cleared, and the AH register is unchanged. In either case, the AL register is left with its top nibble set to 0.

**Operation**

IF ((AL AND FH) > 9) OR (AF = 1)
THEN
  AL ← AL - 6;
  AH ← AH - 1;
  AF ← 1;
  CF ← 1;
ELSE
  CF ← 0;
  AF ← 0;
FI;
AL ← AL AND FH;

**Flags Affected**

The AF and CF flags are set to 1 if there is a decimal borrow; otherwise, they are cleared to 0. The OF, SF, ZF, and PF flags are undefined.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults NaT Register Consumption Abort.

**Exceptions (All Operating Modes)**

None.
ADC—Add with Carry

Description

Adds the destination operand (first operand), the source operand (second operand), and the carry (CF) flag and stores the result in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location. The state of the CF flag represents a carry from a previous addition. When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The ADC instruction does not distinguish between signed or unsigned operands. Instead, the processor evaluates the result for both data types and sets the OF and CF flags to indicate a carry in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

The ADC instruction is usually executed as part of a multibyte or multiword addition in which an ADD instruction is followed by an ADC instruction.

Operation

\[
\text{DEST} \leftarrow \text{DEST} + \text{SRC} + \text{CF};
\]

Flags Affected

The OF, SF, ZF, AF, CF, and PF flags are set according to the result.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>NaT Register Consumption Abort.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>
ADC—Add with Carry (Continued)

Protected Mode Exceptions

#GP(0) If the destination is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
ADD—Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>04 ib</td>
<td>ADD AL, imm8</td>
<td>Add imm8 to AL</td>
</tr>
<tr>
<td>05 iw</td>
<td>ADD AX, imm16</td>
<td>Add imm16 to AX</td>
</tr>
<tr>
<td>05 id</td>
<td>ADD EAX, imm32</td>
<td>Add imm32 to EAX</td>
</tr>
<tr>
<td>80 /0 ib</td>
<td>ADD r/m8, imm8</td>
<td>Add imm8 to r/m8</td>
</tr>
<tr>
<td>81 /0 iw</td>
<td>ADD r/m16, imm16</td>
<td>Add imm16 to r/m16</td>
</tr>
<tr>
<td>81 /0 id</td>
<td>ADD r/m32, imm32</td>
<td>Add imm32 to r/m32</td>
</tr>
<tr>
<td>83 /0 ib</td>
<td>ADD r/m32, imm8</td>
<td>Add sign-extended imm8 to r/m16</td>
</tr>
<tr>
<td>00 /r</td>
<td>ADD r/m8, r8</td>
<td>Add r8 to r/m8</td>
</tr>
<tr>
<td>01 /r</td>
<td>ADD r/m16, r16</td>
<td>Add r16 to r/m16</td>
</tr>
<tr>
<td>01 /r</td>
<td>ADD r/m32, r32</td>
<td>Add r32 to r/m32</td>
</tr>
<tr>
<td>02 /r</td>
<td>ADD r8, r/m8</td>
<td>Add r/m8 to r8</td>
</tr>
<tr>
<td>03 /r</td>
<td>ADD r16, r/m16</td>
<td>Add r/m16 to r16</td>
</tr>
<tr>
<td>03 /r</td>
<td>ADD r32, r/m32</td>
<td>Add r/m32 to r32</td>
</tr>
</tbody>
</table>

**Description**

Adds the first operand (destination operand) and the second operand (source operand) and stores the result in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location. When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The ADD instruction does not distinguish between signed or unsigned operands. Instead, the processor evaluates the result for both data types and sets the OF and CF flags to indicate a carry in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

**Operation**

DEST ← DEST + SRC;

**Flags Affected**

The OF, SF, ZF, AF, CF, and PF flags are set according to the result.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault.
ADD—Add (Continued)

Protected Mode Exceptions

#GP(0)  If the destination is located in a nonwritable segment.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.

If the DS, ES, FS, or GS register is used to access memory and it contains a
null segment selector.

#SS(0)If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made
while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
AND—Logical AND

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24 ib</td>
<td>AND AL, imm8</td>
<td>AL AND imm8</td>
</tr>
<tr>
<td>25 iw</td>
<td>AND AX, imm16</td>
<td>AX AND imm16</td>
</tr>
<tr>
<td>25 id</td>
<td>AND EAX, imm32</td>
<td>EAX AND imm32</td>
</tr>
<tr>
<td>80 /4 ib</td>
<td>AND r/m8, imm8</td>
<td>r/m8 AND imm8</td>
</tr>
<tr>
<td>81 /4 iw</td>
<td>AND r/m16, imm16</td>
<td>r/m16 AND imm16</td>
</tr>
<tr>
<td>81 /4 id</td>
<td>AND r/m32, imm32</td>
<td>r/m32 AND imm32</td>
</tr>
<tr>
<td>83 /4 ib</td>
<td>AND r/m16, imm8</td>
<td>r/m16 AND imm8</td>
</tr>
<tr>
<td>83 /4 ib</td>
<td>AND r/m32, imm8</td>
<td>r/m32 AND imm8</td>
</tr>
<tr>
<td>20 /r</td>
<td>AND r/m8, r8</td>
<td>r/m8 AND r8</td>
</tr>
<tr>
<td>21 /r</td>
<td>AND r/m16, r16</td>
<td>r/m16 AND r16</td>
</tr>
<tr>
<td>21 /r</td>
<td>AND r/m32, r32</td>
<td>r/m32 AND r32</td>
</tr>
<tr>
<td>22 /r</td>
<td>AND r8, r/m8</td>
<td>r8 AND r/m8</td>
</tr>
<tr>
<td>23 /r</td>
<td>AND r16, r/m16</td>
<td>r16 AND r/m16</td>
</tr>
<tr>
<td>23 /r</td>
<td>AND r32, r/m32</td>
<td>r32 AND r/m32</td>
</tr>
</tbody>
</table>

Description

Performs a bitwise AND operation on the destination (first) and source (second) operands and stores the result in the destination operand location. The source operand can be an immediate, a register, or a memory location; the destination operand can be a register or a memory location.

Operation

DEST ← DEST AND SRC;

Flags Affected

The OF and CF flags are cleared; the SF, ZF, and PF flags are set according to the result. The state of the AF flag is undefined.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>NaT Register Consumption Abort.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>

Protected Mode Exceptions

#GP(0) If the destination operand points to a nonwritable segment.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.
AND—Logical AND (Continued)

#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
ARPL—Adjust RPL Field of Segment Selector

**Opcode** | **Instruction** | **Description**
---|---|---
63 /r | ARPL r/m16,r16 | Adjust RPL of r/m16 to not less than RPL of r16

**Description**

Compares the RPL fields of two segment selectors. The first operand (the destination operand) contains one segment selector and the second operand (source operand) contains the other. (The RPL field is located in bits 0 and 1 of each operand.) If the RPL field of the destination operand is less than the RPL field of the source operand, the ZF flag is set and the RPL field of the destination operand is increased to match that of the source operand. Otherwise, the ZF flag is cleared and no change is made to the destination operand. (The destination operand can be a word register or a memory location; the source operand must be a word register.)

The ARPL instruction is provided for use by operating-system procedures (however, it can also be used by applications). It is generally used to adjust the RPL of a segment selector that has been passed to the operating system by an application program to match the privilege level of the application program. Here the segment selector passed to the operating system is placed in the destination operand and segment selector for the application program’s code segment is placed in the source operand. (The RPL field in the source operand represents the privilege level of the application program.) Execution of the ARPL instruction then insures that the RPL of the segment selector received by the operating system is no lower (does not have a higher privilege) than the privilege level of the application program. (The segment selector for the application program’s code segment can be read from the procedure stack following a procedure call.)

See the *IA-32 Intel® Architecture Software Developer’s Manual, Volume 3* for more information about the use of this instruction.

**Operation**

IF DEST(RPL) < SRC(RPL)
 THEN
    ZF ← 1;
    DEST(RPL) ← SRC(RPL);
ELSE
    ZF ← 0;
FI;

**Flags Affected**

The ZF flag is set to 1 if the RPL field of the destination operand is less than that of the source operand; otherwise, is cleared to 0.

**Additional Itanium® System Environment Exceptions**

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>Itanium Mem Faults</th>
</tr>
</thead>
<tbody>
<tr>
<td>NaT Register Consumption Abort.</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>
ARPL—Adjust RPL Field of Segment Selector (Continued)

**Protected Mode Exceptions**

#GP(0)  
If the destination is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0)  
If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  
If a page fault occurs.

#AC(0)  
If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real Address Mode Exceptions**

#UD  
The ARPL instruction is not recognized in real address mode.

**Virtual 8086 Mode Exceptions**

#UD  
The ARPL instruction is not recognized in virtual 8086 mode.
BOUND—Check Array Index Against Bounds

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>62 /r</td>
<td>BOUND r16,m16&amp;16</td>
<td>Check if r16 (array index) is within bounds specified by m16&amp;16</td>
</tr>
<tr>
<td>62 /r</td>
<td>BOUND r32,m32&amp;32</td>
<td>Check if r32 (array index) is within bounds specified by m16&amp;16</td>
</tr>
</tbody>
</table>

Description

Determines if the first operand (array index) is within the bounds of an array specified the second operand (bounds operand). The array index is a signed integer located in a register. The bounds operand is a memory location that points to a pair of signed doubleword-integers (when the operand-size attribute is 32) or a pair of signed word-integers (when the operand-size attribute is 16). The first doubleword (or word) is the lower bound of the array and the second doubleword (or word) is the upper bound of the array. The array index must be greater than or equal to the lower bound and less than or equal to the upper bound plus the operand size in bytes. If the index is not within bounds, a BOUND range exceeded exception (#BR) is signaled. (When a this exception is generated, the saved return instruction pointer points to the BOUND instruction.)

The bounds limit data structure (two words or doublewords containing the lower and upper limits of the array) is usually placed just before the array itself, making the limits addressable via a constant offset from the beginning of the array. Because the address of the array already will be present in a register, this practice avoids extra bus cycles to obtain the effective address of the array bounds.

Operation

If \( \text{ArrayIndex} < \text{LowerBound OR ArrayIndex} > (\text{UpperBound} + \text{OperandSize}/8) \) (* Below lower bound or above upper bound *)

Then

\#BR;

Else:

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.

Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
BOUND—Check Array Index Against Bounds (Continued)

Protected Mode Exceptions

#BR          If the bounds test fails.
#UD          If second operand is not a memory location.
#GP(0)       If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
              If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0)       If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0)       If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#BR          If the bounds test fails.
#GP          If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS          If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#BR          If the bounds test fails.
#GP(0)       If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)       If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0)       If alignment checking is enabled and an unaligned memory reference is made.
BSF—Bit Scan Forward

**Description**

Searches the source operand (second operand) for the least significant set bit (1 bit). If a least significant 1 bit is found, its bit index is stored in the destination operand (first operand). The source operand can be a register or a memory location; the destination operand is a register. The bit index is an unsigned offset from bit 0 of the source operand. If the contents source operand are 0, the contents of the destination operand is undefined.

**Operation**

IF SRC = 0  
THEN  
    ZF ← 1;  
    DEST is undefined;  
ELSE  
    ZF ← 0;  
    temp ← 0;  
    WHILE Bit(SRC, temp) = 0  
    DO  
        temp ← temp + 1;  
        DEST ← temp;  
    OD;  
FI;

**Flags Affected**

The ZF flag is set to 1 if all the source operand is 0; otherwise, the ZF flag is cleared. The CF, OF, SF, AF, and PF, flags are undefined.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults       NaT Register Consumption Abort.
Itanium Mem Faults       VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F BC</td>
<td>BSF r16,r/m16</td>
<td>Bit scan forward on r/m16</td>
</tr>
<tr>
<td>0F BC</td>
<td>BSF r32,r/m32</td>
<td>Bit scan forward on r/m32</td>
</tr>
</tbody>
</table>
BSF—Bit Scan Forward (Continued)

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
BSR—Bit Scan Reverse

**Description**

Searches the source operand (second operand) for the most significant set bit (1 bit). If a most significant 1 bit is found, its bit index is stored in the destination operand (first operand). The source operand can be a register or a memory location; the destination operand is a register. The bit index is an unsigned offset from bit 0 of the source operand. If the contents source operand are 0, the contents of the destination operand is undefined.

**Operation**

\[
\begin{align*}
\text{IF SRC} &= 0 \\
& \quad \text{THEN} \\
& \quad \text{ZF} \leftarrow 1; \\
& \quad \text{DEST is undefined;} \\
& \text{ELSE} \\
& \quad \text{ZF} \leftarrow 0; \\
& \quad \text{temp} \leftarrow \text{OperandSize} - 1; \\
& \quad \text{WHILE Bit(SRC, temp) = 0} \\
& \quad \quad \text{temp} \leftarrow \text{temp} - 1; \\
& \quad \quad \text{DEST} \leftarrow \text{temp}; \\
& \quad \quad \text{OD}; \\
& \text{FI}; \\
\end{align*}
\]

**Flags Affected**

The ZF flag is set to 1 if all the source operand is 0; otherwise, the ZF flag is cleared. The CF, OF, SF, AF, and PF, flags are undefined.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
BSR—Bit Scan Reverse (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
BSWAP—Byte Swap

Description
Reverses the byte order of a 32-bit (destination) register: bits 0 through 7 are swapped with bits 24 through 31, and bits 8 through 15 are swapped with bits 16 through 23. This instruction is provided for converting little-endian values to big-endian format and vice versa.

To swap bytes in a word value (16-bit register), use the XCHG instruction. When the BSWAP instruction references a 16-bit register, the result is undefined.

Operation

\[
\begin{align*}
\text{TEMP} & \leftarrow \text{DEST} \\
\text{DEST}(7..0) & \leftarrow \text{TEMP}(31..24) \\
\text{DEST}(15..8) & \leftarrow \text{TEMP}(23..16) \\
\text{DEST}(23..16) & \leftarrow \text{TEMP}(15..8) \\
\text{DEST}(31..24) & \leftarrow \text{TEMP}(7..0)
\end{align*}
\]

Flags Affected
None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.

Exceptions (All Operating Modes)
None.

Intel® Architecture Compatibility Information

The BSWAP instruction is not supported on Intel architecture processors earlier than the Intel486™ processor family. For compatibility with this instruction, include functionally-equivalent code for execution on Intel processors earlier than the Intel486 processor family.
BT—Bit Test

**Description**

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand) and stores the value of the bit in the CF flag. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value. If the bit base operand specifies a register, the instruction takes the modulo 16 or 32 (depending on the register size) of the bit offset operand, allowing any bit position to be selected in a 16- or 32-bit register, respectively. If the bit base operand specifies a memory location, it represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The offset operand then selects a position within the range \(-2^{31}\) to \(2^{31} - 1\) for a register offset and 0 to 31 for an immediate offset.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. In this case, the low-order 3 or 5 bits (3 for 16-bit operands, 5 for 32-bit operands) of the immediate bit offset are stored in the immediate bit offset field, and the high-order bits are shifted and combined with the byte displacement in the addressing mode by the assembler. The processor will ignore the high order bits if they are not zero.

When accessing a bit in memory, the processor may access 4 bytes starting from the memory address for a 32-bit operand size, using by the following relationship:

\[
\text{Effective Address} + (4 \times (\text{BitOffset} \div 32))
\]

Or, it may access 2 bytes starting from the memory address for a 16-bit operand, using this relationship:

\[
\text{Effective Address} + (2 \times (\text{BitOffset} \div 16))
\]

It may do so even when only a single byte needs to be accessed to reach the given bit. When using this bit addressing mechanism, software should avoid referencing areas of memory close to address space holes. In particular, it should avoid references to memory-mapped I/O registers. Instead, software should use the MOV instructions to load from or store to these addresses, and use the register form of these instructions to manipulate the data.

**Operation**

\[
\text{CF} \leftarrow \text{Bit(BitBase, BitOffset)}
\]

**Flags Affected**

The CF flag contains the value of the selected bit. The OF, SF, ZF, AF, and PF flags are undefined.
BT—Bit Test (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
BTC—Bit Test and Complement

<table>
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<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F BB</td>
<td>BTC r/m16,r16</td>
<td>Store selected bit in CF flag and complement</td>
</tr>
<tr>
<td>0F BB</td>
<td>BTC r/m32,r32</td>
<td>Store selected bit in CF flag and complement</td>
</tr>
<tr>
<td>0F BA /7 ib</td>
<td>BTC r/m16,imm8</td>
<td>Store selected bit in CF flag and complement</td>
</tr>
<tr>
<td>0F BA /7 ib</td>
<td>BTC r/m32,imm8</td>
<td>Store selected bit in CF flag and complement</td>
</tr>
</tbody>
</table>

**Description**

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand), stores the value of the bit in the CF flag, and complements the selected bit in the bit string. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value. If the bit base operand specifies a register, the instruction takes the modulo 16 or 32 (depending on the register size) of the bit offset operand, allowing any bit position to be selected in a 16- or 32-bit register, respectively. If the bit base operand specifies a memory location, it represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The offset operand then selects a bit position within the range \(-2^{31}\) to \(2^{31} - 1\) for a register offset and 0 to 31 for an immediate offset.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. See “BT—Bit Test” on page 3:390 for more information on this addressing mechanism.

**Operation**

\[
\begin{align*}
\text{CF} & \leftarrow \text{Bit(BitBase, BitOffset)} \\
\text{Bit(BitBase, BitOffset)} & \leftarrow \text{NOT Bit(BitBase, BitOffset)};
\end{align*}
\]

**Flags Affected**

The CF flag contains the value of the selected bit before it is complemented. The OF, SF, ZF, AF, and PF flags are undefined.

**Additional Itanium® System Environment Exceptions**

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<th>Itanium Reg Faults</th>
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<td>Itanium Mem Faults</td>
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</tr>
</tbody>
</table>
BTC—Bit Test and Complement (Continued)

Protected Mode Exceptions

#GP(0) If the destination operand points to a non-writable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
BTR—Bit Test and Reset

**Description**

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand), stores the value of the bit in the CF flag, and clears the selected bit in the bit string to 0. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value. If the bit base operand specifies a register, the instruction takes the modulo 16 or 32 (depending on the register size) of the bit offset operand, allowing any bit position to be selected in a 16- or 32-bit register, respectively. If the bit base operand specifies a memory location, it represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The offset operand then selects a bit position within the range $-2^{31}$ to $2^{31} - 1$ for a register offset and 0 to 31 for an immediate offset.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. See “BT—Bit Test” on page 3:390 for more information on this addressing mechanism.

**Operation**

\[
\begin{align*}
  CF &\leftarrow \text{Bit(BitBase, BitOffset)} \\
  \text{Bit(BitBase, BitOffset)} &\leftarrow 0;
\end{align*}
\]

**Flags Affected**

The CF flag contains the value of the selected bit before it is cleared. The OF, SF, ZF, AF, and PF flags are undefined.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
BTR—Bit Test and Reset (Continued)

**Protected Mode Exceptions**

- **#GP(0)**
  - If the destination operand points to a nonwritable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.

- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real Address Mode Exceptions**

- **#GP**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS**
  - If a memory operand effective address is outside the SS segment limit.

**Virtual 8086 Mode Exceptions**

- **#GP(0)**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made.
BTS—Bit Test and Set

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
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<tbody>
<tr>
<td>0F AB</td>
<td>BTS r/m16,r16</td>
<td>Store selected bit in CF flag and set</td>
</tr>
<tr>
<td>0F AB</td>
<td>BTS r/m32,r32</td>
<td>Store selected bit in CF flag and set</td>
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<tr>
<td>0F BA /5 ib</td>
<td>BTS r/m16,imm8</td>
<td>Store selected bit in CF flag and set</td>
</tr>
<tr>
<td>0F BA /5 ib</td>
<td>BTS r/m32,imm8</td>
<td>Store selected bit in CF flag and set</td>
</tr>
</tbody>
</table>

**Description**

Selects the bit in a bit string (specified with the first operand, called the bit base) at the bit-position designated by the bit offset operand (second operand), stores the value of the bit in the CF flag, and sets the selected bit in the bit string to 1. The bit base operand can be a register or a memory location; the bit offset operand can be a register or an immediate value. If the bit base operand specifies a register, the instruction takes the modulo 16 or 32 (depending on the register size) of the bit offset operand, allowing any bit position to be selected in a 16- or 32-bit register, respectively. If the bit base operand specifies a memory location, it represents the address of the byte in memory that contains the bit base (bit 0 of the specified byte) of the bit string. The offset operand then selects a bit position within the range $-2^{31}$ to $2^{31} - 1$ for a register offset and 0 to 31 for an immediate offset.

Some assemblers support immediate bit offsets larger than 31 by using the immediate bit offset field in combination with the displacement field of the memory operand. See “BT—Bit Test” on page 3:390 for more information on this addressing mechanism.

**Operation**

$$CF \leftarrow \text{Bit(BitBase, BitOffset)}$$

$$\text{Bit(BitBase, BitOffset)} \leftarrow 1;$$

**Flags Affected**

The CF flag contains the value of the selected bit before it is set. The OF, SF, ZF, AF, and PF flags are undefined.

**Additional Itanium® System Environment Exceptions**

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</tr>
</tbody>
</table>
BTS—Bit Test and Set (Continued)

**Protected Mode Exceptions**

#GP(0)  
If the destination operand points to a nonwritable segment.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0)  
If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  
If a page fault occurs.

#AC(0)  
If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real Address Mode Exceptions**

#GP  
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  
If a memory operand effective address is outside the SS segment limit.

**Virtual 8086 Mode Exceptions**

#GP  
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  
If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  
If a page fault occurs.

#AC(0)  
If alignment checking is enabled and an unaligned memory reference is made.
CALL—Call Procedure

<table>
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<tbody>
<tr>
<td>E8 cd</td>
<td>CALL rel16</td>
<td>Call near, displacement relative to next instruction</td>
</tr>
<tr>
<td>E8 cd</td>
<td>CALL rel32</td>
<td>Call near, displacement relative to next instruction</td>
</tr>
<tr>
<td>FF /2</td>
<td>CALL r/m16</td>
<td>Call near, r/m16 indirect</td>
</tr>
<tr>
<td>FF /2</td>
<td>CALL r/m32</td>
<td>Call near, r/m32 indirect</td>
</tr>
<tr>
<td>9A cd</td>
<td>CALL ptr16:16</td>
<td>Call far, to full pointer given</td>
</tr>
<tr>
<td>9A cp</td>
<td>CALL ptr16:32</td>
<td>Call far, to full pointer given</td>
</tr>
<tr>
<td>FF /3</td>
<td>CALL m16:16</td>
<td>Call far, address at r/m16</td>
</tr>
<tr>
<td>FF /3</td>
<td>CALL m16:32</td>
<td>Call far, address at r/m32</td>
</tr>
</tbody>
</table>

Description

Saves procedure linking information on the procedure stack and jumps to the procedure (called procedure) specified with the destination (target) operand. The target operand specifies the address of the first instruction in the called procedure. This operand can be an immediate value, a general-purpose register, or a memory location.

This instruction can be used to execute four different types of calls:

- Near call – A call to a procedure within the current code segment (the segment currently pointed to by the CS register), sometimes referred to as an intrasegment call.
- Far call – A call to a procedure located in a different segment than the current code segment, sometimes referred to as an intersegment call.
- Inter-privilege-level far call – A far call to a procedure in a segment at a different privilege level than that of the currently executing program or procedure. **Results in an IA-32_Intercept(Gate) in Itanium System Environment.**
- Task switch – A call to a procedure located in a different task. **Results in an IA-32_Intercept(Gate) in Itanium System Environment.**

The latter two call types (inter-privilege-level call and task switch) can only be executed in protected mode. See Chapter 6 in the *IA-32 Intel® Architecture Software Developer's Manual, Volume 3* for information on task switching with the CALL instruction.

When executing a near call, the processor pushes the value of the EIP register (which contains the address of the instruction following the CALL instruction) onto the procedure stack (for use later as a return-instruction pointer). The processor then jumps to the address specified with the target operand for the called procedure. The target operand specifies either an absolute address in the code segment (that is an offset from the base of the code segment) or a relative offset (a signed offset relative to the current value of the instruction pointer in the EIP register, which points to the instruction following the call). An absolute address is specified directly in a register or indirectly in a memory location (r/m16 or r/m32 target-operand form). (When accessing an absolute address indirectly using the stack pointer (ESP) as a base register, the base value used is the value of the ESP before the instruction executes.) A relative offset (rel16 or rel32) is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed, 16- or 32-bit immediate value, which is added to the instruction pointer.
CALL—Call Procedure (Continued)

When executing a near call, the operand-size attribute determines the size of the target operand (16 or 32 bits) for absolute addresses. Absolute addresses are loaded directly into the EIP register. When a relative offset is specified, it is added to the value of the EIP register. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared to 0s, resulting in a maximum instruction pointer size of 16 bits. The CS register is not changed on near calls.

When executing a far call, the processor pushes the current value of both the CS and EIP registers onto the procedure stack for use as a return-instruction pointer. The processor then performs a far jump to the code segment and address specified with the target operand for the called procedure. Here the target operand specifies an absolute far address either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32). With the pointer method, the segment and address of the called procedure is encoded in the instruction using a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address immediate. With the indirect method, the target operand specifies a memory location that contains a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address. The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The far address is loaded directly into the CS and EIP registers. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared to 0s.

Any far call from a 32-bit code segment to a 16-bit code segment should be made from the first 64 Kbytes of the 32-bit code segment, because the operand-size attribute of the instruction is set to 16, allowing only a 16-bit return address offset to be saved. Also, the call should be made using a 16-bit call gate so that 16-bit values will be pushed on the stack.

When the processor is operating in protected mode, a far call can also be used to access a code segment at a different privilege level or to switch tasks. Here, the processor uses the segment selector part of the far address to access the segment descriptor for the segment being jumped to. Depending on the value of the type and access rights information in the segment selector, the CALL instruction can perform:

• A far call to the same privilege level (described in the previous paragraph).
• An far call to a different privilege level. Results in an IA-32 Intercept(Gate) in Itanium System Environment.
• A task switch. Results in an IA-32 Intercept(Gate) in Itanium System Environment.

When executing an inter-privilege-level far call, the code segment for the procedure being called is accessed through a call gate. The segment selector specified by the target operand identifies the call gate. In executing a call through a call gate where a change of privilege level occurs, the processor switches to the stack for the privilege level of the called procedure, pushes the current values of the CS and EIP registers and the SS and ESP values for the old stack onto the new stack, then performs a far jump to the new code segment. The new code segment is specified in the call gate descriptor; the new stack segment is specified in the TSS for the currently running task. The jump to the new code segment occurs after the stack switch. On the new stack, the processor pushes the segment selector and stack pointer for the calling procedure’s stack, a set of parameters from the calling procedures stack, and the segment selector and instruction pointer for the calling procedure’s code segment. (A value in the call gate descriptor determines how many parameters to copy to the new stack.)

Finally, the processor jumps to the address of the procedure being called within the new code segment. The procedure address is the offset specified by the target operand. Here again, the target operand can specify the far address of the call gate and procedure either directly with a pointer (ptr16:16 or ptr16:32) or indirectly with a memory location (m16:16 or m16:32).
CALL—Call Procedure (Continued)

Executing a task switch with the CALL instruction, is similar to executing a call through a call gate. Here the target operand specifies the segment selector of the task gate for the task being switched to and the address of the procedure being called in the task. The task gate in turn points to the TSS for the task, which contains the segment selectors for the task’s code and stack segments. The CALL instruction can also specify the segment selector of the TSS directly. See the IA-32 Intel® Architecture Software Developer’s Manual, Volume 3 the for detailed information on the mechanics of a task switch.

Operation

IF near call
THEN IF near relative call
IF the instruction pointer is not within code segment limit THEN #GP(0); FI;
THEN IF OperandSize = 32
    THEN
        IF stack not large enough for a 4-byte return address THEN #SS(0); FI;
        Push(EIP);
        EIP ← EIP + DEST; (* DEST is rel32 *)
    ELSE (* OperandSize = 16 *)
        IF stack not large enough for a 2-byte return address THEN #SS(0); FI;
        Push(IP);
        EIP ← (EIP + DEST) AND 0000FFFFH; (* DEST is rel16 *)
    FI;
FI;
ELSE (* near absolute call *)
    IF the instruction pointer is not within code segment limit THEN #GP(0); FI;
    IF OperandSize = 32
        THEN
            IF stack not large enough for a 4-byte return address THEN #SS(0); FI;
            Push(EIP);
            EIP ← DEST; (* DEST is r/m32 *)
        ELSE (* OperandSize = 16 *)
            IF stack not large enough for a 2-byte return address THEN #SS(0); FI;
            Push(IP);
            EIP ← DEST AND 0000FFFFH; (* DEST is r/m16 *)
        FI;
    FI:
    IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
    FI;
    IF far call AND (PE = 0 OR (PE = 1 AND VM = 1)) (* real address or virtual 8086 mode *)
    THEN
        IF OperandSize = 32
            THEN
                IF stack not large enough for a 6-byte return address THEN #SS(0); FI;
                IF the instruction pointer is not within code segment limit THEN #GP(0); FI;
                Push(CS); (* padded with 16 high-order bits *)
                Push(EIP);
                CS ← DEST[47:32]; (* DEST is ptr16:32 or [m16:32] *)
                EIP ← DEST[31:0]; (* DEST is ptr16:32 or [m16:32] *)
            ELSE (* OperandSize = 16 *)
                IF stack not large enough for a 4-byte return address THEN #SS(0); FI;
                IF the instruction pointer is not within code segment limit THEN #GP(0); FI;
                Push(CS);
                Push(IP);
CALL—Call Procedure (Continued)

        CS ← DEST[31:16]; (* DEST is ptr16:16 or [m16:16] *)
        EIP ← DEST[15:0]; (* DEST is ptr16:16 or [m16:16] *)
        EIP ← EIP AND 0000FFFFH; (* clear upper 16 bits *) 
        FI;
        IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
        FI;
        IF far call AND (PE = 1 AND VM = 0) (* Protected mode, not virtual 8086 mode *)
        THEN
        IF segment selector in target operand null THEN #GP(0); FI;
        IF segment selector index not within descriptor table limits 
          THEN #GP(new code selector);
        FI;
        Read type and access rights of selected segment descriptor;
        IF segment type is not a conforming or nonconforming code segment, call gate, 
          task gate, or TSS THEN #GP(segment selector); FI;
        Depending on type and access rights
          GO TO CONFORMING-CODE-SEGMENT;
          GO TO NONCONFORMING-CODE-SEGMENT;
          GO TO CALL-GATE;
          GO TO TASK-GATE;
          GO TO TASK-STATE-SEGMENT;
        FI;

        CONFORMING-CODE-SEGMENT:
        IF DPL > CPL THEN #GP(new code segment selector); FI;
        IF not present THEN #NP(selector); FI;
        IF OperandSize = 32
          THEN
            IF stack not large enough for a 6-byte return address THEN #SS(0); FI;
            IF the instruction pointer is not within code segment limit THEN #GP(0); FI;
            Push(CS); (* padded with 16 high-order bits *)
            Push(EIP);
            CS ← DEST(NewCodeSegmentSelector);
            (* segment descriptor information also loaded *)
            CS(RPL) ← CPL
            EIP ← DEST(offset);
          ELSE (* OperandSize = 16 *)
            IF stack not large enough for a 4-byte return address THEN #SS(0); FI;
            IF the instruction pointer is not within code segment limit THEN #GP(0); FI;
            Push(CS);
            Push(IP);
            CS ← DEST(NewCodeSegmentSelector);
            (* segment descriptor information also loaded *)
            CS(RPL) ← CPL
            EIP ← DEST(offset) AND 0000FFFFH; (* clear upper 16 bits *)
          FI;
          IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
        END;

        NONCONFORMING-CODE-SEGMENT:
        IF (RPL > CPL) OR (DPL ≠ CPL) THEN #GP(new code segment selector); FI;
        IF stack not large enough for return address THEN #SS(0); FI;
        tempEIP ← DEST(offset)
CALL—Call Procedure (Continued)

IF OperandSize=16
  THEN
    tempEIP ← tempEIP AND 0000FFFFH; (* clear upper 16 bits *)
  FI;
IF tempEIP outside code segment limit THEN #GP(0); FI;
IF OperandSize = 32
  THEN
    Push(CS); (* padded with 16 high-order bits *)
    Push(EIP);
    CS ← DEST(NewCodeSegmentSelector);
    (* segment descriptor information also loaded *)
    CS(RPL) ← CPL;
    EIP ← tempEIP;
  ELSE (* OperandSize = 16 *)
    Push(CS);
    Push(IP);
    CS ← DEST(NewCodeSegmentSelector);
    (* segment descriptor information also loaded *)
    CS(RPL) ← CPL;
    EIP ← tempEIP;
  FI;
IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
END;

CALL-GATE:
IF call gate DPL < CPL or RPL THEN #GP(call gate selector); FI;
IF not present THEN #NP(call gate selector); FI;
IF Itanium System Environment THEN IA-32_Intercept(Gate,CALL);
IF call gate code-segment selector is null THEN #GP(0); FI;
IF call gate code-segment selector index is outside descriptor table limits
  THEN #GP(code segment selector); FI;
Read code segment descriptor;
IF code-segment segment descriptor does not indicate a code segment
  OR code-segment segment descriptor DPL > CPL
  THEN #GP(code segment selector); FI;
IF code segment not present THEN #NP(new code segment selector); FI;
IF code segment is non-conforming AND DPL < CPL
  THEN go to MORE-PRIVILEGE;
  ELSE go to SAME-PRIVILEGE;
FI;
END;

MORE-PRIVILEGE:
IF current TSS is 32-bit TSS
  THEN
    TSSstackAddress ← new code segment (DPL + 8) + 4
    IF (TSSstackAddress + 7) > TSS limit
      THEN #TS(current TSS selector); FI;
    newSS ← TSSstackAddress + 4;
    newESP ← stack address;
  ELSE (* TSS is 16-bit *)
    TSSstackAddress ← new code segment (DPL + 4) + 2
    IF (TSSstackAddress + 4) > TSS limit
      THEN #TS(current TSS selector); FI;
CALL—Call Procedure (Continued)

newESP ← TSSstackAddress;
newSS ← TSSstackAddress + 2;
FI;
IF stack segment selector is null THEN #TS(stack segment selector); FI;
IF stack segment selector index is not within its descriptor table limits
THEN #TS(SS selector); FI
Read code segment descriptor;
IF stack segment selector’s RPL ≠ DPL of code segment
OR stack segment DPL ≠ DPL of code segment
OR stack segment is not a writable data segment
THEN #TS(SS selector); FI
IF stack segment not present THEN #SS(SS selector); FI;
IF CallGateSize = 32
THEN
IF stack does not have room for parameters plus 16 bytes
THEN #SS(SS selector); FI;
IF CallGate(InstructionPointer) not within code segment limit THEN #GP(0); FI;
SS ← newSS;
(* segment descriptor information also loaded *)
ESP ← newESP;
CS:EIP ← CallGate(CS:InstructionPointer);
(* segment descriptor information also loaded *)
Push(oldSS:oldESP); (* from calling procedure *)
temp ← parameter count from call gate, masked to 5 bits;
Push(parameters from calling procedure’s stack, temp)
Push(oldCS:oldEIP); (* return address to calling procedure *)
ELSE (* CallGateSize = 16 *)
IF stack does not have room for parameters plus 8 bytes
THEN #SS(SS selector); FI;
IF (CallGate(InstructionPointer) AND FFFFH) not within code segment limit
THEN #GP(0); FI;
SS ← newSS;
(* segment descriptor information also loaded *)
ESP ← newESP;
CS:IP ← CallGate(CS:InstructionPointer);
(* segment descriptor information also loaded *)
Push(oldSS:oldESP); (* from calling procedure *)
temp ← parameter count from call gate, masked to 5 bits;
Push(parameters from calling procedure’s stack, temp)
Push(oldCS:oldEIP); (* return address to calling procedure *)
ELSE (* CallGateSize = 16 *)
FI;
CPL ← CodeSegment(DPL)
CS(RPL) ← CPL
END;
SAME-PRIVILEGE:
IF CallGateSize = 32
THEN
IF stack does not have room for 8 bytes
THEN #SS(0); FI;
IF EIP not within code segment limit then #GP(0); FI;
CS:EIP ← CallGate(CS:EIP) (* segment descriptor information also loaded *)
Push(oldCS:oldEIP); (* return address to calling procedure *)
ELSE (* CallGateSize = 16 *)
CALL—Call Procedure (Continued)

IF stack does not have room for parameters plus 4 bytes
    THEN SS(0); FI;
IF IP not within code segment limit THEN GP(0); FI;
CS:IP ← CallGate(CS:instruction pointer)
(* segment descriptor information also loaded *)
PUSH(oldCS:oldIP); (* return address to calling procedure *)
FI;
CS(RPL) ← CPL
END;

TASK-GATE:
  IF task gate DPL < CPL or RPL
    THEN GP(task gate selector);
  FI;
  IF task gate not present
    THEN NP(task gate selector);
  FI;
  IF Itanium System Environment THEN IA-32_Intercept(Gate,CALL);
  Read the TSS segment selector in the task-gate descriptor;
  IF TSS segment selector local/global bit is set to local
      OR index not within GDT limits
      THEN GP(TSS selector);
  FI;
  Access TSS descriptor in GDT;
  IF TSS descriptor specifies that the TSS is busy (low-order 5 bits set to 00001)
      THEN GP(TSS selector);
  FI;
  IF TSS not present
      THEN NP(TSS selector);
  FI;
  SWITCH-TASKS (with nesting) to TSS;
  IF EIP not within code segment limit
      THEN GP(0);
  FI;
END;

TASK-STATE-SEGMENT:
  IF TSS DPL < CPL or RPL
      OR TSS segment selector local/global bit is set to local
      OR TSS descriptor indicates TSS not available
      THEN GP(TSS selector);
  FI;
  IF TSS is not present
      THEN NP(TSS selector);
  FI;
  IF Itanium System Environment THEN IA-32_Intercept(Gate,CALL);
  SWITCH-TASKS (with nesting) to TSS
  IF EIP not within code segment limit
      THEN GP(0);
  FI;
END;
CALL—Call Procedure (Continued)

Flags Affected

All flags are affected if a task switch occurs; no flags are affected if a task switch does not occur.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Itanium Mem Faults</th>
<th>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</th>
</tr>
</thead>
<tbody>
<tr>
<td>IA-32_Intercept</td>
<td>Gate Intercept for CALLs through CALL Gates, Task Gates and Task Segments</td>
</tr>
<tr>
<td>IA-32_Exception</td>
<td>Taken Branch Debug Exception if PSR.tb is 1</td>
</tr>
</tbody>
</table>

Protected Mode Exceptions

#GP(0) If target offset in destination operand is beyond the new code segment limit.

If the segment selector in the destination operand is null.

If the code segment selector in the gate is null.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#GP(selector) If code segment or gate or TSS selector index is outside descriptor table limits.

If the segment descriptor pointed to by the segment selector in the destination operand is not for a conforming-code segment, nonconforming-code segment, call gate, task gate, or task state segment.

If the DPL for a nonconforming-code segment is not equal to the CPL or the RPL for the segment’s segment selector is greater than the CPL.

If the DPL for a conforming-code segment is greater than the CPL.

If the DPL from a call-gate, task-gate, or TSS segment descriptor is less than the CPL or than the RPL of the call-gate, task-gate, or TSS’s segment selector.

If the segment descriptor for a segment selector from a call gate does not indicate it is a code segment.

If the segment selector from a call gate is beyond the descriptor table limits.

If the DPL for a code-segment obtained from a call gate is greater than the CPL.

If the segment selector for a TSS has its local/global bit set for local.

If a TSS segment descriptor specifies that the TSS is busy or not available.

#SS(0) If pushing the return address, parameters, or stack segment pointer onto the stack exceeds the bounds of the stack segment, when no stack switch occurs.

If a memory operand effective address is outside the SS segment limit.
CALL—Call Procedure (Continued)

#SS(selector)  If pushing the return address, parameters, or stack segment pointer onto the stack exceeds the bounds of the stack segment, when a stack switch occurs.

If the SS register is being loaded as part of a stack switch and the segment pointed to is marked not present.

If stack segment does not have room for the return address, parameters, or stack segment pointer, when stack switch occurs.

#NP(selector)  If a code segment, data segment, stack segment, call gate, task gate, or TSS is not present.

#TS(selector)  If the new stack segment selector and ESP are beyond the end of the TSS.

If the new stack segment selector is null.

If the RPL of the new stack segment selector in the TSS is not equal to the DPL of the code segment being accessed.

If DPL of the stack segment descriptor for the new stack segment is not equal to the DPL of the code segment descriptor.

If the new stack segment is not a writable data segment.

If segment-selector index for stack segment is outside descriptor table limits.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If an unaligned memory access occurs when the CPL is 3 and alignment checking is enabled.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the target offset is beyond the code segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the target offset is beyond the code segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If an unaligned memory access occurs when alignment checking is enabled.
CBW/CWDE—Convert Byte to Word/Convert Word to Doubleword

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>98</td>
<td>CBW</td>
<td>AX ← sign-extend of AL</td>
</tr>
<tr>
<td>98</td>
<td>CWDE</td>
<td>EAX ← sign-extend of AX</td>
</tr>
</tbody>
</table>

**Description**

Double the size of the source operand by means of sign extension. The CBW (convert byte to word) instruction copies the sign (bit 7) in the source operand into every bit in the AH register. The CWDE (convert word to doubleword) instruction copies the sign (bit 15) of the word in the AX register into the higher 16 bits of the EAX register.

The CBW and CWDE mnemonics reference the same opcode. The CBW instruction is intended for use when the operand-size attribute is 16 and the CWDE instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when CBW is used and to 32 when CWDE is used. Others may treat these mnemonics as synonyms (CBW/CWDE) and use the current setting of the operand-size attribute to determine the size of values to be converted, regardless of the mnemonic used.

The CWDE instruction is different from the CWD (convert word to double) instruction. The CWD instruction uses the DX:AX register pair as a destination operand; whereas, the CWDE instruction uses the EAX register as a destination.

**Operation**

IF OperandSize = 16 (* instruction = CBW *)
THEN AX ← SignExtend(AL);
ELSE (* OperandSize = 32, instruction = CWDE *)
   EAX ← SignExtend(AX);
FI;

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults NaT Register Consumption Abort.

**Exceptions (All Operating Modes)**

None.
CDQ—Convert Double to Quad

See entry for CWD/CDQ — Convert Word to Double/Convert Double to Quad.
CLC—Clear Carry Flag

Description
Clears the CF flag in the EFLAGS register.

Operation
\[ CF \leftarrow 0; \]

Flags Affected
The CF flag is cleared to 0. The OF, ZF, SF, AF, and PF flags are unaffected.

Exceptions (All Operating Modes)
None.
CLD—Clear Direction Flag

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FC</td>
<td>CLD</td>
<td>Clear DF flag</td>
</tr>
</tbody>
</table>

Description

Clears the DF flag in the EFLAGS register. When the DF flag is set to 0, string operations increment the index registers (ESI and/or EDI).

Operation

\[ DF \leftarrow 0; \]

Flags Affected

The DF flag is cleared to 0. The CF, OF, ZF, SF, AF, and PF flags are unaffected.

Exceptions (All Operating Modes)

None.
CLI—Clear Interrupt Flag

Description

Clears the IF flag in the EFLAGS register. No other flags are affected. Clearing the IF flag causes the processor to ignore maskable external interrupts. The IF flag and the CLI and STI instruction have no affect on the generation of exceptions and NMI interrupts. In the Itanium System Environment, external interrupts are enabled for IA-32 instructions if PSR.i and (~CFLG.if or EFLAG.if) is 1 and for Itanium instructions if PSR.i is 1.

The following decision table indicates the action of the CLI instruction (bottom of the table) depending on the processor’s mode of operating and the CPL and IOPL of the currently running program or procedure (top of the table).

<table>
<thead>
<tr>
<th>PE</th>
<th>VM</th>
<th>CPL</th>
<th>IOPL</th>
<th>IF</th>
<th>#GP(0)</th>
<th>#GP(0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>X</td>
<td>&gt; IOPL</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>= 3</td>
<td>X</td>
<td>Y</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>&lt; 3</td>
<td></td>
<td>N</td>
<td>Y</td>
<td>Y</td>
</tr>
</tbody>
</table>

Notes:
X Don’t care.
N Action in column 1 not taken.
Y Action in column 1 taken.

Operation

OLD_IF <- IF;
IF PE = 0 (* Executing in real-address mode *)
THEN
IF <- 0;
ELSE
IF VM = 0 (* Executing in protected mode *)
THEN
IF CR4.PVI = 1
THEN
IF CPL = 3
THEN
IF IOPL<3
THEN #GP(0);
ELSE IF <- 0;
FI;
ELSE (*CPL < 3*)
IF IOPL < CPL
THEN #GP(0);
ELSE IF <- 0;

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FA</td>
<td>CLI</td>
<td>Clear interrupt flag; interrupts disabled when interrupt flag cleared</td>
</tr>
</tbody>
</table>
CLI—Clear Interrupt Flag (Continued)

```
    FI;
    FI;
    ELSE (*CR4.PVI==0 *)
        IF IOPL < CPL
            THEN #GP(0);
        ELSE IF <- 0;
            FI;
    FI;
    ELSE (* Executing in Virtual-8086 mode *)
        IF IOPL = 3
            THEN
                IF <- 0;
            ELSE
                IF CR4.VME= 0
                    THEN #GP(0);
                ELSE VIF <- 0;
                    FI;
            FI;
    FI;
    IF Itanium System Environment AND CFLG.ii AND IF != OLD_IF
        THEN IA-32_Intercept(System_Flag,CLI);
```

Flags Affected

The IF is cleared to 0 if the CPL is equal to or less than the IOPL; otherwise, the it is not affected. The other flags in the EFLAGS register are unaffected.

Additional Itanium® System Environment Exceptions

IA-32_Intercept System Flag Intercept Trap if CFLG.ii is 1 and the IF flag changes state.

Protected Mode Exceptions

#GP(0) If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.

Real Address Mode Exceptions

None.

Virtual 8086 Mode Exceptions

#GP(0) If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.
CLTS—Clear Task-Switched Flag in CR0

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 06</td>
<td>CLTS</td>
<td>Clears TS flag in CR0</td>
</tr>
</tbody>
</table>

**Description**

Clears the task-switched (TS) flag in the CR0 register. This instruction is intended for use in operating-system procedures. It is a privileged instruction that can only be executed at a CPL of 0. It is allowed to be executed in real-address mode to allow initialization for protected mode.

The processor sets the TS flag every time a task switch occurs. The flag is used to synchronize the saving of FPU context in multitasking applications. See the description of the TS flag in the *IA-32 Intel® Architecture Software Developer’s Manual, Volume 3* for more information about this flag.

**Operation**

IF Itanium System Environment THEN IA-32_Intercept(INST,CLTS);

CR0(TS) ← 0;

**Flags Affected**

The TS flag in CR0 register is cleared.

**Additional Itanium® System Environment Exceptions**

IA-32_Intercept  Mandatory Instruction Intercept fault.

**Protected Mode Exceptions**

#GP(0)  If the CPL is greater than 0.

**Real Address Mode Exceptions**

None.

**Virtual 8086 Mode Exceptions**

#GP(0)  If the CPL is greater than 0.
CMC—Complement Carry Flag

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F5</td>
<td>CMC</td>
<td>Complement CF flag</td>
</tr>
</tbody>
</table>

**Description**

Complements the CF flag in the EFLAGS register.

**Operation**

\[ CF \leftarrow \text{NOT CF}; \]

**Flags Affected**

The CF flag contains the complement of its original value. The OF, ZF, SF, AF, and PF flags are unaffected.

**Exceptions (All Operating Modes)**

None.
**CMOVcc—Conditional Move**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 47 cw/cd</td>
<td>CMOVA r16, r/m16</td>
<td>Move if above (CF=0 and ZF=0)</td>
</tr>
<tr>
<td>0F 47 cw/cd</td>
<td>CMOVA r32, r/m32</td>
<td>Move if above (CF=0 and ZF=0)</td>
</tr>
<tr>
<td>0F 43 cw/cd</td>
<td>CMOVAE r16, r/m16</td>
<td>Move if above or equal (CF=0)</td>
</tr>
<tr>
<td>0F 43 cw/cd</td>
<td>CMOVAE r32, r/m32</td>
<td>Move if above or equal (CF=0)</td>
</tr>
<tr>
<td>0F 42 cw/cd</td>
<td>CMOVB r16, r/m16</td>
<td>Move if below (CF=1)</td>
</tr>
<tr>
<td>0F 42 cw/cd</td>
<td>CMOVB r32, r/m32</td>
<td>Move if below (CF=1)</td>
</tr>
<tr>
<td>0F 46 cw/cd</td>
<td>CMOVBE r16, r/m16</td>
<td>Move if below or equal (CF=1 or ZF=1)</td>
</tr>
<tr>
<td>0F 46 cw/cd</td>
<td>CMOVBE r32, r/m32</td>
<td>Move if below or equal (CF=1 or ZF=1)</td>
</tr>
<tr>
<td>0F 42 cw/cd</td>
<td>CMOVCA r16, r/m16</td>
<td>Move if carry (CF=1)</td>
</tr>
<tr>
<td>0F 42 cw/cd</td>
<td>CMOVCA r32, r/m32</td>
<td>Move if carry (CF=1)</td>
</tr>
<tr>
<td>0F 44 cw/cd</td>
<td>CMOVC r16, r/m16</td>
<td>Move if equal (ZF=1)</td>
</tr>
<tr>
<td>0F 44 cw/cd</td>
<td>CMOVC r32, r/m32</td>
<td>Move if equal (ZF=1)</td>
</tr>
<tr>
<td>0F 43 cw/cd</td>
<td>CMOVNB r16, r/m16</td>
<td>Move if not below (CF=0 and ZF=1)</td>
</tr>
<tr>
<td>0F 43 cw/cd</td>
<td>CMOVNB r32, r/m32</td>
<td>Move if not below (CF=0 and ZF=1)</td>
</tr>
<tr>
<td>0F 4E cw/cd</td>
<td>CMOVNE r16, r/m16</td>
<td>Move if not carry (CF=0)</td>
</tr>
<tr>
<td>0F 4E cw/cd</td>
<td>CMOVNE r32, r/m32</td>
<td>Move if not carry (CF=0)</td>
</tr>
<tr>
<td>0F 45 cw/cd</td>
<td>CMOVNE r16, r/m16</td>
<td>Move if not equal (ZF=0)</td>
</tr>
<tr>
<td>0F 45 cw/cd</td>
<td>CMOVNE r32, r/m32</td>
<td>Move if not equal (ZF=0)</td>
</tr>
<tr>
<td>0F 4E cw/cd</td>
<td>CMOVNG r16, r/m16</td>
<td>Move if not greater (ZF=1 or SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 4E cw/cd</td>
<td>CMOVNG r32, r/m32</td>
<td>Move if not greater (ZF=1 or SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 4C cw/cd</td>
<td>CMOVNGE r16, r/m16</td>
<td>Move if not greater or equal (SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 4C cw/cd</td>
<td>CMOVNGE r32, r/m32</td>
<td>Move if not greater or equal (SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 4D cw/cd</td>
<td>CMOVNL r16, r/m16</td>
<td>Move if not less (SF=OF)</td>
</tr>
<tr>
<td>0F 4D cw/cd</td>
<td>CMOVNL r32, r/m32</td>
<td>Move if not less (SF=OF)</td>
</tr>
<tr>
<td>0F 4F cw/cd</td>
<td>CMOVNLE r16, r/m16</td>
<td>Move if not less or equal (ZF=0 and SF=OF)</td>
</tr>
<tr>
<td>0F 4F cw/cd</td>
<td>CMOVNLE r32, r/m32</td>
<td>Move if not less or equal (ZF=0 and SF=OF)</td>
</tr>
</tbody>
</table>
CMOVcc—Conditional Move (Continued)

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 41 cw/cd</td>
<td>CMOVNO r16, r/m16</td>
<td>Move if not overflow (OF=0)</td>
</tr>
<tr>
<td>0F 41 cw/cd</td>
<td>CMOVNO r32, r/m32</td>
<td>Move if not overflow (OF=0)</td>
</tr>
<tr>
<td>0F 4B cw/cd</td>
<td>CMOVNP r16, r/m16</td>
<td>Move if not parity (PF=0)</td>
</tr>
<tr>
<td>0F 4B cw/cd</td>
<td>CMOVNP r32, r/m32</td>
<td>Move if not parity (PF=0)</td>
</tr>
<tr>
<td>0F 49 cw/cd</td>
<td>CMOVNS r16, r/m16</td>
<td>Move if not sign (SF=0)</td>
</tr>
<tr>
<td>0F 49 cw/cd</td>
<td>CMOVNS r32, r/m32</td>
<td>Move if not sign (SF=0)</td>
</tr>
<tr>
<td>0F 45 cw/cd</td>
<td>CMOVNZ r16, r/m16</td>
<td>Move if not zero (ZF=0)</td>
</tr>
<tr>
<td>0F 45 cw/cd</td>
<td>CMOVNZ r32, r/m32</td>
<td>Move if not zero (ZF=0)</td>
</tr>
<tr>
<td>0F 40 cw/cd</td>
<td>CMOVO r16, r/m16</td>
<td>Move if overflow (OF=0)</td>
</tr>
<tr>
<td>0F 40 cw/cd</td>
<td>CMOVO r32, r/m32</td>
<td>Move if overflow (OF=0)</td>
</tr>
<tr>
<td>0F 4A cw/cd</td>
<td>CMOVPE r16, r/m16</td>
<td>Move if parity even (PF=1)</td>
</tr>
<tr>
<td>0F 4A cw/cd</td>
<td>CMOVPE r32, r/m32</td>
<td>Move if parity even (PF=1)</td>
</tr>
<tr>
<td>0F 4B cw/cd</td>
<td>CMOVPO r16, r/m16</td>
<td>Move if parity odd (PF=0)</td>
</tr>
<tr>
<td>0F 4B cw/cd</td>
<td>CMOVPO r32, r/m32</td>
<td>Move if parity odd (PF=0)</td>
</tr>
<tr>
<td>0F 48 cw/cd</td>
<td>CMOVNZ r16, r/m16</td>
<td>Move if sign (SF=1)</td>
</tr>
<tr>
<td>0F 48 cw/cd</td>
<td>CMOVNZ r32, r/m32</td>
<td>Move if sign (SF=1)</td>
</tr>
<tr>
<td>0F 44 cw/cd</td>
<td>CMOVZ r16, r/m16</td>
<td>Move if zero (ZF=1)</td>
</tr>
<tr>
<td>0F 44 cw/cd</td>
<td>CMOVZ r32, r/m32</td>
<td>Move if zero (ZF=1)</td>
</tr>
</tbody>
</table>

Description

The CMOVcc instructions check the state of one or more of the status flags in the EFLAGS register (CF, OF, PF, SF, and ZF) and perform a move operation if the flags are in a specified state (or condition). A condition code (cc) is associated with each instruction to indicate the condition being tested for. If the condition is not satisfied, a move is not performed and execution continues with the instruction following the CMOVcc instruction.

If the condition is false for the memory form, some processor implementations will initiate the load (and discard the loaded data), possible memory faults can be generated. Other processor models will not initiate the load and not generate any faults if the condition is false.

These instructions can move a 16- or 32-bit value from memory to a general-purpose register or from one general-purpose register to another. Conditional moves of 8-bit register operands are not supported.

The conditions for each CMOVcc mnemonic is given in the description column of the above table. The terms “less” and “greater” are used for comparisons of signed integers and the terms “above” and “below” are used for unsigned integers.

Because a particular state of the status flags can sometimes be interpreted in two ways, two mnemonics are defined for some opcodes. For example, the CMOVA (conditional move if above) instruction and the CMOVNBE (conditional move if not below or equal) instruction are alternate mnemonics for the opcode 0F 47H.
CMOVcc—Conditional Move (Continued)

The CMOVcc instructions are new for the Pentium Pro processor family; however, they may not be supported by all the processors in the family. Software can determine if the CMOVcc instructions are supported by checking the processor’s feature information with the CPUID instruction (see “CPUID—CPU Identification” on page 3:428).

Operation

\[
\text{temp} \leftarrow \text{DEST} \\
\text{IF condition TRUE THEN} \\
\quad \text{DEST} \leftarrow \text{SRC} \\
\text{ELSE} \\
\quad \text{DEST} \leftarrow \text{temp} \\
\text{FI;}
\]

Flags Affected

None.

If the condition is false for the memory form, some processor implementations will initiate the load (and discard the loaded data), possible memory faults can be generated. Other processor models will not initiate the load and not generate any faults if the condition is false.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>NaT Register Consumption Abort.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>

Protected Mode Exceptions

- \#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.  
  If the DS, ES, FS, or GS register contains a null segment selector.
- \#SS(0)  If a memory operand effective address is outside the SS segment limit.
- \#PF(fault-code)  If a page fault occurs.
- \#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

- \#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- \#SS  If a memory operand effective address is outside the SS segment limit.
CMOVcc—Conditional Move (Continued)

**Virtual 8086 Mode Exceptions**

<table>
<thead>
<tr>
<th>Exception</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP(0)</td>
<td>If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.</td>
</tr>
<tr>
<td>#SS(0)</td>
<td>If a memory operand effective address is outside the SS segment limit.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#AC(0)</td>
<td>If alignment checking is enabled and an unaligned memory reference is made.</td>
</tr>
</tbody>
</table>
CMP—Compare Two Operands

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>3C ib</td>
<td>CMP AL, imm8</td>
<td>Compare imm8 with AL</td>
</tr>
<tr>
<td>3D iw</td>
<td>CMP AX, imm16</td>
<td>Compare imm16 with AX</td>
</tr>
<tr>
<td>3D id</td>
<td>CMP EAX, imm32</td>
<td>Compare imm32 with EAX</td>
</tr>
<tr>
<td>80 /7 ib</td>
<td>CMP r/m8, imm8</td>
<td>Compare imm8 with r/m8</td>
</tr>
<tr>
<td>81 /7 iw</td>
<td>CMP r/m16, imm16</td>
<td>Compare imm16 with r/m16</td>
</tr>
<tr>
<td>81 /7 id</td>
<td>CMP r/m32,imm32</td>
<td>Compare imm32 with r/m32</td>
</tr>
<tr>
<td>83 /7 ib</td>
<td>CMP r/m16,imm8</td>
<td>Compare imm8 with r/m16</td>
</tr>
<tr>
<td>83 /7 ib</td>
<td>CMP r/m32,imm8</td>
<td>Compare imm8 with r/m32</td>
</tr>
<tr>
<td>38 /r</td>
<td>CMP r/m8,r8</td>
<td>Compare r8 with r/m8</td>
</tr>
<tr>
<td>39 /r</td>
<td>CMP r/m16,r16</td>
<td>Compare r16 with r/m16</td>
</tr>
<tr>
<td>39 /r</td>
<td>CMP r/m32,r32</td>
<td>Compare r32 with r/m32</td>
</tr>
<tr>
<td>3A /r</td>
<td>CMP r8,r/m8</td>
<td>Compare r/m8 with r8</td>
</tr>
<tr>
<td>3B /r</td>
<td>CMP r16,r/m16</td>
<td>Compare r/m16 with r16</td>
</tr>
<tr>
<td>3B /r</td>
<td>CMP r32,r/m32</td>
<td>Compare r/m32 with r32</td>
</tr>
</tbody>
</table>

Description

Compares the first source operand with the second source operand and sets the status flags in the EFLAGS register according to the results. The comparison is performed by subtracting the second operand from the first operand and then setting the status flags in the same manner as the SUB instruction. When an immediate value is used as an operand, it is sign-extended to the length of the first operand.

The CMP instruction is typically used in conjunction with a conditional jump (Jcc), condition move (CMOVcc), or SETcc instruction. The condition codes used by the Jcc, CMOVcc, and SETcc instructions are based on the results of a CMP instruction.

Operation

\[
\text{temp} \leftarrow \text{SRC1} - \text{SignExtend} (\text{SRC2}) ;
\]

ModifyStatusFlags; (* Modify status flags in the same manner as the SUB instruction*)

Flags Affected

The CF, OF, SF, ZF, AF, and PF flags are set according to the result.

Additional Itanium® System Environment Exceptions

- **Itanium Reg Faults**: NaT Register Consumption Abort.
- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
CMP—Compare Two Operands (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
CMPS/CMPSB/CMPSW/CMPSD—Compare String Operands

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A6</td>
<td>CMPS DS:(E)SI, ES:(E)DI</td>
<td>Compares byte at address DS:(E)SI with byte at address ES:(E)DI and sets the status flags accordingly</td>
</tr>
<tr>
<td>A7</td>
<td>CMPS DS:SI, ES:DI</td>
<td>Compares byte at address DS:SI with byte at address ES:DI and sets the status flags accordingly</td>
</tr>
<tr>
<td>A7</td>
<td>CMPS DS:ESI, ES:EDI</td>
<td>Compares byte at address DS:ESI with byte at address ES:EDI and sets the status flags accordingly</td>
</tr>
<tr>
<td>A6</td>
<td>CMPSB</td>
<td>Compares byte at address DS:(E)SI with byte at address ES:(E)DI and sets the status flags accordingly</td>
</tr>
<tr>
<td>A7</td>
<td>CMPSW</td>
<td>Compares byte at address DS:SI with byte at address ES:DI and sets the status flags accordingly</td>
</tr>
<tr>
<td>A7</td>
<td>CMPSD</td>
<td>Compares byte at address DS:ESI with byte at address ES:EDI and sets the status flags accordingly</td>
</tr>
</tbody>
</table>

Description

Compares the byte, word, or double word specified with the first source operand with the byte, word, or double word specified with the second source operand and sets the status flags in the EFLAGS register according to the results. The first source operand specifies the memory location at the address DS:ESI and the second source operand specifies the memory location at address ES:EDI. (When the operand-size attribute is 16, the SI and DI register are used as the source-index and destination-index registers, respectively.) The DS segment may be overridden with a segment override prefix, but the ES segment cannot be overridden.

The CMPSB, CMPSW, and CMPSD mnemonics are synonyms of the byte, word, and doubleword versions of the CMPS instructions. They are simpler to use, but provide no type or segment checking. (For the CMPS instruction, “DS:ESI” and “ES:EDI” must be explicitly specified in the instruction.)

After the comparison, the ESI and EDI registers are incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the ESI and EDI register are incremented; if the DF flag is 1, the ESI and EDI registers are decremented.) The registers are incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The CMPS, CMPSB, CMPSW, and CMPSD instructions can be preceded by the REP prefix for block comparisons of ECX bytes, words, or doublewords. More often, however, these instructions will be used in a LOOP construct that takes some action based on the setting of the status flags before the next comparison is made.
Operation

temp ← SRC1 − SRC2;
SetStatusFlags(temp);
IF (byte comparison)
THEN IF DF = 0
   THEN (E)DI ← 1; (E)SI ← 1;
   ELSE (E)DI ← −1; (E)SI ← −1;
FI;
ELSE IF (word comparison)
THEN IF DF = 0
   THEN DI ← 2; (E)SI ← 2;
   ELSE DI ← −2; (E)SI ← −2;
FI;
ELSE (* doubleword comparison *)
THEN IF DF = 0
   THEN EDI ← 4; (E)SI ← 4;
   ELSE EDI ← −4; (E)SI ← −4;
FI;
FI;
FI;
FI;

Flags Affected

The CF, OF, SF, ZF, AF, and PF flags are set according to the temporary result of the comparison.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
CMPS/CMPSB/CMPSW/CMPSD—Compare String Operands (Continued)

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
CMPXCHG—Compare and Exchange

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F B0/r</td>
<td>CMPXCHG r/m8,r8</td>
<td>Compare AL with r/m8. If equal, ZF is set and r8 is loaded into r/m8. Else, clear ZF and load r/m8 into AL.</td>
</tr>
<tr>
<td>0F B1/r</td>
<td>CMPXCHG r/m16,r16</td>
<td>Compare AX with r/m16. If equal, ZF is set and r16 is loaded into r/m16. Else, clear ZF and load r/m16 into AL.</td>
</tr>
<tr>
<td>0F B1/r</td>
<td>CMPXCHG r/m32,r32</td>
<td>Compare EAX with r/m32. If equal, ZF is set and r32 is loaded into r/m32. Else, clear ZF and load r/m32 into AL.</td>
</tr>
</tbody>
</table>

Description

Compares the value in the AL, AX, or EAX register (depending on the size of the operand) with the first operand (destination operand). If the two values are equal, the second operand (source operand) is loaded into the destination operand. Otherwise, the destination operand is loaded into the AL, AX, or EAX register.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically. To simplify the interface to the processor’s bus, the destination operand receives a write cycle without regard to the result of the comparison. The destination operand is written back if the comparison fails; otherwise, the source operand is written into the destination. (The processor never produces a locked read without also producing a locked write.)

Operation

(* accumulator = AL, AX, or EAX, depending on whether *)
(* a byte, word, or doubleword comparison is being performed*)

IF Itanium System Environment AND External_Atomic_Lock_Required AND DCR.lc
THEN IA-32_Intercept(LOCK,CMPXCHG);
IF accumulator = DEST
THEN
    ZF ← 1
    DEST ← SRC
ELSE
    ZF ← 0
    accumulator ← DEST
FI;

Flags Affected

The ZF flag is set if the values in the destination operand and register AL, AX, or EAX are; otherwise it is cleared. The CF, PF, AF, SF, and OF flags are set according to the results of the comparison operation.
CMPXCHG—Compare and Exchange (Continued)

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
- IA-32_Interceptor: Lock Intercept - If an external atomic bus lock is required to complete this operation and DCR.1c is 1, no atomic transaction occurs, this instruction is faulted and an IA-32_Interceptor(Lock) fault is generated. The software lock handler is responsible for the emulation of this instruction.

Protected Mode Exceptions

- #GP(0): If the destination is located in a nonwritable segment.
- #SS(0): If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code): If a page fault occurs.
- #AC(0): If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

- #GP: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS: If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

- #GP(0): If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0): If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code): If a page fault occurs.
- #AC(0): If alignment checking is enabled and an unaligned memory reference is made.

Intel® Architecture Compatibility

This instruction is not supported on Intel processors earlier than the Intel486 processors.
**CMPXCHG8B—Compare and Exchange 8 Bytes**

**Opcode**  | **Instruction** | **Description**  
---|---|---  
0F C7 /1 m64 | CMPXCHG8B m64 | Compare EDX:EAX with m64. If equal, set ZF and load ECX:EBX into m64. Else, clear ZF and load m64 into EDX:EAX.

**Description**

Compares the 64-bit value in EDX:EAX with the operand (destination operand). If the values are equal, the 64-bit value in ECX:EBX is stored in the destination operand. Otherwise, the value in the destination operand is loaded into EDX:EAX. The destination operand is an 8-byte memory location. For the EDX:EAX and ECX:EBX register pairs, EDX and ECX contain the high-order 32 bits and EAX and EBX contain the low-order 32 bits of a 64-bit value.

This instruction can be used with a LOCK prefix to allow the instruction to be executed atomically. To simplify the interface to the processor’s bus, the destination operand receives a write cycle without regard to the result of the comparison. The destination operand is written back if the comparison fails; otherwise, the source operand is written into the destination. (The processor never produces a locked read without also producing a locked write.)

**Operation**

\[
\begin{align*}
\text{IF Itanium System Environment AND ExternalAtomicLockRequired AND DCR.lc} & \\text{THEN IA-32_Intercept(LOCK,CMPXCHG);} \\
\text{IF (EDX:EAX = DEST)} & \\text{ZF} \leftarrow 1 \\
\text{DEST} & \leftarrow \text{ECX:EBX} \\
\text{ELSE} & \text{ZF} \leftarrow 0 \\
\text{EDX:EAX} & \leftarrow \text{DEST}
\end{align*}
\]

**Flags Affected**

The ZF flag is set if the destination operand and EDX:EAX are equal; otherwise it is cleared. The CF, PF, AF, SF, and OF flags are unaffected.

**Additional Itanium® System Environment Exceptions**

- **Itanium Reg Faults**: NaT Register Consumption Abort.
- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
- **IA-32_Intercept**: Lock Intercept - If an external atomic bus lock is required to complete this operation and DCR.lc is 1, no atomic transaction occurs, this instruction is faulted and an IA-32_Intercept(Lock) fault is generated. The software lock handler is responsible for the emulation of this instruction.
CMPXCHG8B—Compare and Exchange 8 Bytes (Continued)

Protected Mode Exceptions

#UD If the destination operand is not a memory location.
#GP(0) If the destination is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Intel® Architecture Compatibility

This instruction is not supported on Intel processors earlier than the Pentium processors.
CPUID—CPU Identification

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F A2</td>
<td>CPUID</td>
<td>EAX ← Processor identification information</td>
</tr>
</tbody>
</table>

Description

Provides processor identification information in registers EAX, EBX, ECX, and EDX. This information identifies Intel as the vendor, gives the family, model, and stepping of processor, feature information, and cache information. An input value loaded into the EAX register determines what information is returned, as shown in Table 1-4.

Table 1-4. Information Returned by CPUID Instruction

<table>
<thead>
<tr>
<th>Initial EAX Value</th>
<th>Information Provided about the Processor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>EAX Maximum CPUID Input Value</td>
</tr>
<tr>
<td></td>
<td>EBX 756E6547H “Genu” (G in BL)</td>
</tr>
<tr>
<td></td>
<td>ECX 6C65746EH “ntel” (n in CL)</td>
</tr>
<tr>
<td></td>
<td>EDX 49656E69H “ineI” (i in DL)</td>
</tr>
<tr>
<td>1</td>
<td>EAX Version Information (Family, Model, and Stepping ID)</td>
</tr>
<tr>
<td></td>
<td>EBX Reserved</td>
</tr>
<tr>
<td></td>
<td>ECX Reserved</td>
</tr>
<tr>
<td></td>
<td>EDX Feature Information</td>
</tr>
<tr>
<td>2</td>
<td>EAX Cache Information</td>
</tr>
<tr>
<td></td>
<td>EBX Cache Information</td>
</tr>
<tr>
<td></td>
<td>ECX Cache Information</td>
</tr>
<tr>
<td></td>
<td>EDX Cache Information</td>
</tr>
</tbody>
</table>

The CPUID instruction can be executed at any privilege level to serialize instruction execution. Serializing instruction execution guarantees that any modifications to flags, registers, and memory for previous instructions are completed before the next instruction is fetched and executed.

When the input value in register EAX is 0, the processor returns the highest value the CPUID instruction recognizes in the EAX register. For the Itanium processor, the highest recognized value is 2. A vendor identification string is returned in the EBX, EDX, and ECX registers. For Intel processors, the vendor identification string is “GenuIntel” as follows:

EBX ← 756e6547h (* “Genu”, with G in the low nibble of BL *)
EDX ← 49656e69h (* “ineI”, with i in the low nibble of DL *)
ECX ← 6c65746eh (* “ntel”, with n in the low nibble of CL *)

When the input value is 1, the processor returns version information in the EAX register and feature information in the EDX register.
CPUID—CPU Identification (Continued)

The version information consists of an Intel architecture extended family identifier, an extended model identifier, an Intel architecture family identifier, a model identifier and a stepping ID.

See “Intel Application Note 485 — Intel Processor Identification with the CPUID Instruction” for more information on identifying earlier Intel architecture processors. Intel releases information on stepping IDs as needed.

A feature flag set to 1 indicates the corresponding feature is supported. Software should identify Intel as the vendor to properly interpret the feature flags.

**Note:** IA-32 System Environment feature bits may be set in the Itanium System Environment even if that feature cannot be used within the Itanium System Environment.

### Table 1-5. Feature Flags Returned in EDX Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>IA-32 System Environment Feature</th>
<th>Intel® Itanium® System Environment Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>FPU—Floating-point Unit on Chip</td>
<td>Available</td>
<td>Processor contains an FPU and executes the Intel387 instruction set.</td>
</tr>
</tbody>
</table>
| 1   | VME—Virtual 8086 Mode Enhancements | Available                                   | Processor supports the following virtual 8086 mode enhancements:  
• CR4.VME bit enables virtual 8086 mode extensions.  
• CR4.PVI bit enables protected-mode virtual interrupts.  
• Expansion of the TSS with the software indirection bitmap.  
• EFLAGS.VIF bit enables the virtual interrupt flag.  
• EFLAGS.VIP bit enables the virtual interrupt pending flag. |
| 3   | PSE—Page Size Extensions         | Not Available                               | Processor supports 4-MByte pages, including the CR4.PSE bit for enabling page size extensions, the modified bit in page directory entries (PDEs), page directory entries, and page table entries (PTEs). |
| 4   | TSC—Time Stamp Counter           | Available                                   | Processor supports the RDTSC (read time stamp counter) instruction, including the CR4.TSD bit that, along with the CPL, controls whether the time stamp counter can be read. |
| 5   | MSR—Model Specific Registers     | Not Available                               | Processor supports the RDMSR (read model-specific register) and WRMSR (write model-specific register) instructions. |
| 6   | PAE—Physical Address Extension   | Not Available                               | Processor supports physical addresses greater than 32 bits, the extended page-table-entry format, an extra level in the page translation tables, and 2-MByte pages. The CR4.PAE bit enables this feature. The number of address bits is implementation specific. |

Figure 1-3. Version Information in Registers EAX
<table>
<thead>
<tr>
<th>Bit</th>
<th>IA-32 System Environment Feature</th>
<th>Intel® Itanium® System Environment Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>MCE—Machine Check Exception</td>
<td>Not Available. Processor uses PAL defined MCHK architecture.</td>
<td>Processor supports the CR4.MCE bit, enabling machine check exceptions. However, this feature does not define the model-specific implementations of machine-check error logging, reporting, or processor shutdowns. Machine-check exception handlers might have to check the processor version to do model-specific processing of the exception or check for the presence of the machine-check feature.</td>
</tr>
<tr>
<td>8</td>
<td>CX8—CMPXCHG8B Instruction</td>
<td>Available</td>
<td>Processor supports the CMPXCHG8B (compare and exchange 8 bytes) instruction.</td>
</tr>
<tr>
<td>9</td>
<td>APIC</td>
<td>Not Available. Replaced by the Itanium interrupt mechanism.</td>
<td>Processor contains an on-chip Advanced Programmable Interrupt Controller (APIC) and it has been enabled and is available for use.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
<td>Not Available.</td>
<td>returns zero</td>
</tr>
<tr>
<td>12</td>
<td>MTRRR—Memory Type Range Registers</td>
<td>Not Available. Processor utilizes memory attributes from the TLB defined by the Itanium architecture</td>
<td>Processor supports machine-specific memory-type range registers (MTRRs). The MTRRs contains bit fields that indicate the processor’s MTRR capabilities, including which memory types the processor supports, the number of variable MTRRs the processor supports, and whether the processor supports fixed MTRRs.</td>
</tr>
<tr>
<td>13</td>
<td>PGE—PTE Global Flag</td>
<td>Not available. Superceded by virtual regions defined in the Itanium architecture</td>
<td>Processor supports the CR4.PGE flag enabling the global bit in both PTDEs and PTEs. These bits are used to indicate translation lookaside buffer (TLB) entries that are common to different tasks and need not be flushed when control register CR3 is written.</td>
</tr>
<tr>
<td>14</td>
<td>MCA—Machine Check Architecture</td>
<td>Not Available. Processor uses PAL defined MCHK architecture.</td>
<td>Processor supports the MCG_CAP (machine check global capability) MSR. The MCG_CAP register indicates how many banks of error reporting MSRs the processor supports.</td>
</tr>
<tr>
<td>15</td>
<td>CMOV—Conditional Move and Compare Instructions</td>
<td>Available</td>
<td>Processor supports the CMOVCc instruction and, if the FPU feature flag (bit 0) is also set, supports the FCMOVcc and FCOMI instructions.</td>
</tr>
<tr>
<td>16</td>
<td>PSE-36 - 36-bit Page Size Extensions</td>
<td>Not available. The Itanium architecture always supports more than 32-bits of physical addressing</td>
<td>Indicates whether the processor supports 4-Mbyte pages that are capable of addressing physical memory beyond 4GB. This feature indicates that the upper four bits of the physical address of the 4-Mbyte page is encoded by bits 13-16 of the page directory entry.</td>
</tr>
<tr>
<td>17</td>
<td>PAT - Memory Attribute Palette</td>
<td>Not available for paging. Superceded by virtual regions defined in the Intel® Itanium® architecture.</td>
<td>Processors supports the IA-32 physical attribute table</td>
</tr>
<tr>
<td>18</td>
<td>PPN - Physical Processor Number</td>
<td>Not available. The Intel® Itanium® architecture does not support this feature.</td>
<td>Processor supports a Physical Processor Number for each manufactured processor</td>
</tr>
<tr>
<td>23</td>
<td>MMX - Intel® MMX™ Technology</td>
<td>Available</td>
<td>Processor supports the Architecture Intel® MMX™ Technology</td>
</tr>
<tr>
<td>24</td>
<td>FXSR</td>
<td>Available</td>
<td>Processor supports the Streaming SIMD Extension FXRSTOR and FXSAVE instruction</td>
</tr>
<tr>
<td>25</td>
<td>XMM - Streaming SIMD Extension Technology</td>
<td>Available</td>
<td>Processor supports the Intel® architecture Streaming SIMD Extension</td>
</tr>
<tr>
<td>30</td>
<td>Processor based on the Intel® Itanium® architecture</td>
<td>Available</td>
<td>The processor is based on the Intel® Itanium® architecture and is capable of executing the Intel® Itanium® instruction set. IA-32 application level software MUST also check with the running operating system to see if the system can also support Itanium®-based code before switching to the Intel® Itanium® instruction set.</td>
</tr>
</tbody>
</table>
CPUID—CPU Identification (Continued)

When the input value is 2, the processor returns information about the processor’s internal caches and TLBs in the EAX, EBX, ECX, and EDX registers. The encoding of these registers is as follows:

- The least-significant byte in register EAX (register AL) indicates the number of times the CPUID instruction must be executed with an input value of 2 to get a complete description of the processor’s caches and TLBs.
- The most significant bit (bit 31) of each register indicates whether the register contains valid information (cleared to 0) or is reserved (set to 1).

Please see the processor specific supplement for further information on how to decode the return values for the processors internal caches and TLBs.

CPUID performs instruction serialization and a memory fence operation.

Operation

CASE (EAX) OF

EAX = 0:
  EAX ← highest input value understood by CPUID; (* 2 for Itanium processor *)
  EBX ← Vendor identification string;
  EDX ← Vendor identification string;
  ECX ← Vendor identification string;
  BREAK;
EAX = 1:
  EAX[3:0] ← Stepping ID;
  EAX[7:4] ← Model;
  EAX[11:8] ← Family;
  EAX[15:12] ← Reserved;
  EAX[19:16] ← Extended Model ID;
  EAX[27:20] ← Extended Family ID;
  EAX[31:28] ← Reserved;
  EBX ← Reserved;
  ECX ← Reserved;
  EDX ← Feature flags;
  BREAK;
EAX = 2:
  EAX[7:0] ← N_Param_Descrip_Blocks = 1;
  EAX[31:8], EBX, ECX, EDX = cache and TLB parameters
  BREAK;
DEFAULT: (* EAX > highest value recognized by CPUID *)
  EAX ← Reserved, Undefined;
  EBX ← Reserved, Undefined;
  ECX ← Reserved, Undefined;
  EDX ← Reserved, Undefined;
  BREAK;
ESAC;

memory_fence();
instruction_serialize();

Flags Affected

None.
CPUID—CPU Identification (Continued)

Additional Itanium® System Environment Exceptions
Itanium Reg Faults   NaT Register Consumption Abort.

Exceptions (All Operating Modes)
None.

Intel® Architecture Compatibility

The CPUID instruction is not supported in early models of the Intel486 processor or in any Intel architecture processor earlier than the Intel486 processor. The ID flag in the EFLAGS register can be used to determine if this instruction is supported. If a procedure is able to set or clear this flag, the CPUID is supported by the processor running the procedure.
CWD/CDQ—Convert Word to Doubleword/Convert Doubleword to Quadword

**Description**

Doubles the size of the operand in register AX or EAX (depending on the operand size) by means of sign extension and stores the result in registers DX:AX or EDX:EAX, respectively. The CWD instruction copies the sign (bit 15) of the value in the AX register into every bit position in the DX register. The CDQ instruction copies the sign (bit 31) of the value in the EAX register into every bit position in the EDX register.

The CWD instruction can be used to produce a doubleword dividend from a word before a word division, and the CDQ instruction can be used to produce a quadword dividend from a doubleword before doubleword division.

The CWD and CDQ mnemonics reference the same opcode. The CWD instruction is intended for use when the operand-size attribute is 16 and the CDQ instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when CWD is used and to 32 when CDQ is used. Others may treat these mnemonics as synonyms (CWD/CDQ) and use the current setting of the operand-size attribute to determine the size of values to be converted, regardless of the mnemonic used.

**Operation**

```plaintext
IF OperandSize = 16 (* CWD instruction *)
    THEN DX ← SignExtend(AX);
ELSE (* OperandSize = 32, CDQ instruction *)
    EDX ← SignExtend(EAX);
FI;
```

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults  NaT Register Consumption Abort.

**Flags Affected**

None.

**Exceptions (All Operating Modes)**

None.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>99</td>
<td>CWD</td>
<td>DX:AX ← sign-extend of AX</td>
</tr>
<tr>
<td>99</td>
<td>CDQ</td>
<td>EDX:EAX ← sign-extend of EAX</td>
</tr>
</tbody>
</table>
CWDE—Convert Word to Doubleword

See entry for CBW/CWDE—Convert Byte to Word/Convert Word to Doubleword.
DAA—Decimal Adjust AL after Addition

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>27</td>
<td>DAA</td>
<td>Decimal adjust AL after addition</td>
</tr>
</tbody>
</table>

**Description**

Adjusts the sum of two packed BCD values to create a packed BCD result. The AL register is the implied source and destination operand. The DAA instruction is only useful when it follows an ADD instruction that adds (binary addition) two 2-digit, packed BCD values and stores a byte result in the AL register. The DAA instruction then adjusts the contents of the AL register to contain the correct 2-digit, packed BCD result. If a decimal carry is detected, the CF and AF flags are set accordingly.

**Operation**

IF (((AL AND 0FH) > 9) or AF = 1)
THEN
  AL ← AL + 6;
  CF ← CF OR CarryFromLastAddition; (* CF OR carry from AL ← AL + 6 *)
  AF ← 1;
ELSE
  AF ← 0;
FI;
IF ((AL AND F0H) > 90H) or CF = 1)
THEN
  AL ← AL + 60H;
  CF ← 1;
ELSE
  CF ← 0;
FI;

**Example**

ADD AL, BL Before: AL=79H BL=35H EFLAGS(OSZAPC)=XXXXXX
After: AL=AEH BL=35H EFLAGS(OSZAPC)=110000
DAA Before: AL=AEH BL=35H EFLAGS(OSZAPC)=110000
After: AL=AEH BL=35H EFLAGS(OSZAPC)=X00111

**Flags Affected**

The CF and AF flags are set if the adjustment of the value results in a decimal carry in either digit of the result (see “Operation” above). The SF, ZF, and PF flags are set according to the result. The OF flag is undefined.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults NaT Register Consumption Abort.

**Exceptions (All Operating Modes)**

None.
DAS—Decimal Adjust AL after Subtraction

**Description**

Adjusts the result of the subtraction of two packed BCD values to create a packed BCD result. The AL register is the implied source and destination operand. The DAS instruction is only useful when it follows a SUB instruction that subtracts (binary subtraction) one 2-digit, packed BCD value from another and stores a byte result in the AL register. The DAS instruction then adjusts the contents of the AL register to contain the correct 2-digit, packed BCD result. If a decimal borrow is detected, the CF and AF flags are set accordingly.

**Operation**

\[
\text{IF } (\text{AL AND 0FH}) > 9 \text{ OR AF} = 1 \\
\quad \text{THEN} \\
\quad \quad \text{AL} \leftarrow \text{AL} - 6; \\
\quad \quad \text{CF} \leftarrow \text{CF OR BorrowFromLastSubtraction}; \quad (* \text{CF OR borrow from AL} \leftarrow \text{AL} - 6 *) \\
\quad \quad \text{AF} \leftarrow 1; \\
\quad \text{ELSE AF} \leftarrow 0; \\
\text{FI;}
\]

\[
\text{IF } ((\text{AL} > 9FH) \text{ or CF} = 1) \\
\quad \text{THEN} \\
\quad \quad \text{AL} \leftarrow \text{AL} - 60H; \\
\quad \quad \text{CF} \leftarrow 1; \\
\quad \text{ELSE CF} \leftarrow 0; \\
\text{FI;}
\]

**Example**

SUB AL, BL  
Before: AL=35H BL=47H EFLAGS(OSZAPC)=XXXXXX  
After: AL=EEH BL=47H EFLAGS(OSZAPC)=010111

DAA  
Before: AL=EEH BL=47H EFLAGS(OSZAPC)=010111  
After: AL=88H BL=47H EFLAGS(OSZAPC)=X10111

**Flags Affected**

The CF and AF flags are set if the adjustment of the value results in a decimal borrow in either digit of the result (see “Operation” above). The SF, ZF, and PF flags are set according to the result. The OF flag is undefined.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults   NaT Register Consumption Abort.

**Exceptions (All Operating Modes)**

None.
DEC—Decrement by 1

### Description

Subtracts 1 from the operand, while preserving the state of the CF flag. The source operand can be a register or a memory location. This instruction allows a loop counter to be updated without disturbing the CF flag. (Use a SUB instruction with an immediate operand of 1 to perform a decrement operation that does updates the CF flag.)

### Operation

\[ \text{DEST} \leftarrow \text{DEST} - 1; \]

### Flags Affected

The CF flag is not affected. The OF, SF, ZF, AF, and PF flags are set according to the result.

### Additional Itanium® System Environment Exceptions

- **Itanium Reg Faults**: NaT Register Consumption Abort.
- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

### Protected Mode Exceptions

- **#GP(0)**
  - If the destination is located in a nonwritable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.
- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)**
  - If a page fault occurs.
- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

### Real Address Mode Exceptions

- **#GP**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS**
  - If a memory operand effective address is outside the SS segment limit.

### Opcode Instruction Description

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE /1</td>
<td>DEC r/m8</td>
<td>Decrement r/m8 by 1</td>
</tr>
<tr>
<td>FF /1</td>
<td>DEC r/m16</td>
<td>Decrement r/m16 by 1</td>
</tr>
<tr>
<td>FF /1</td>
<td>DEC r/m32</td>
<td>Decrement r/m32 by 1</td>
</tr>
<tr>
<td>48+rw</td>
<td>DEC r/m32</td>
<td>Decrement r/m32 by 1</td>
</tr>
<tr>
<td>48+rd</td>
<td>DEC r16</td>
<td>Decrement r16 by 1</td>
</tr>
</tbody>
</table>

---

*Volume 3: Base IA-32 Instruction Reference*
DEC—Decrement by 1 (Continued)

**Virtual 8086 Mode Exceptions**

<table>
<thead>
<tr>
<th>Exception</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP(0)</td>
<td>If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.</td>
</tr>
<tr>
<td>#SS(0)</td>
<td>If a memory operand effective address is outside the SS segment limit.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#AC(0)</td>
<td>If alignment checking is enabled and an unaligned memory reference is made.</td>
</tr>
</tbody>
</table>
DIV—Unsigned Divide

### Description

Divides (unsigned) the value in the AL, AX, or EAX register (dividend) by the source operand (divisor) and stores the result in the AX, DX:AX, or EDX:EAX registers. The source operand can be a general-purpose register or a memory location. The action of this instruction depends on the operand size, as shown in the following table:

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Dividend</th>
<th>Divisor</th>
<th>Quotient</th>
<th>Remainder</th>
<th>Maximum Quotient</th>
</tr>
</thead>
<tbody>
<tr>
<td>Word/byte</td>
<td>AX</td>
<td>r/m8</td>
<td>AL</td>
<td>AH</td>
<td>255</td>
</tr>
<tr>
<td>Doubleword/word</td>
<td>DX:AX</td>
<td>r/m16</td>
<td>AX</td>
<td>DX</td>
<td>65,535</td>
</tr>
<tr>
<td>Quadword/doubleword</td>
<td>EDX:EAX</td>
<td>r/m32</td>
<td>EAX</td>
<td>EDX</td>
<td>$2^{32} - 1$</td>
</tr>
</tbody>
</table>

Non-integral results are truncated (chopped) towards 0. The remainder is always less than the divisor in magnitude. Overflow is indicated with the #DE (divide error) exception rather than with the CF flag.

### Operation

IF SRC = 0
    THEN #DE; (* divide error *)
FI;

IF OperandSize = 8 (* word/byte operation *)
    THEN
        temp ← AX / SRC;
        IF temp > FFH
            THEN #DE; (* divide error *)
            ELSE
                AL ← temp;
                AH ← AX MOD SRC;
            FI;
        ELSE
            IF OperandSize = 16 (* doubleword/word operation *)
                THEN
                    temp ← DX:AX / SRC;
                    IF temp > FFFFH
                        THEN #DE; (* divide error *)
                        ELSE
                            AX ← temp;
                            DX ← DX:AX MOD SRC;
                        FI;
DIV—Unsigned Divide (Continued)

```c
ELSE (* quadword/doubleword operation *)
    temp ← EDX:EAX / SRC;
    IF temp > FFFFFFFFFH
        THEN #DE; (* divide error *);
        ELSE
            EAX ← temp;
            EDX ← EDX:EAX MOD SRC;
        FI;
    FI;
FI;
```

Flags Affected

The CF, OF, SF, ZF, AF, and PF flags are undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults
- NaT Register Consumption Abort.

Itanium Mem Faults
- VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#DE If the source operand (divisor) is 0
If the quotient is too large for the designated register.

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#DE If the source operand (divisor) is 0.
If the quotient is too large for the designated register.

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.
DIV—Unsigned Divide (Continued)

Virtual 8086 Mode Exceptions

#DE If the source operand (divisor) is 0.
   If the quotient is too large for the designated register.

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
ENTER—Make Stack Frame for Procedure Parameters

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C8 iw 00</td>
<td>ENTER imm16,0</td>
<td>Create a stack frame for a procedure</td>
</tr>
<tr>
<td>C8 iw 01</td>
<td>ENTER imm16,1</td>
<td>Create a nested stack frame for a procedure</td>
</tr>
<tr>
<td>C8 iw ib</td>
<td>ENTER imm16,imm8</td>
<td>Create a nested stack frame for a procedure</td>
</tr>
</tbody>
</table>

**Description**

Creates a stack frame for a procedure. The first operand (size operand) specifies the size of the stack frame (that is, the number of bytes of dynamic storage allocated on the stack for the procedure). The second operand (nesting level operand) gives the lexical nesting level (0 to 31) of the procedure. The nesting level determines the number of stack frame pointers that are copied into the “display area” of the new stack frame from the preceding frame. Both of these operands are immediate values.

The stack-size attribute determines whether the BP (16 bits) or EBP (32 bits) register specifies the current frame pointer and whether SP (16 bits) or ESP (32 bits) specifies the stack pointer.

The ENTER and companion LEAVE instructions are provided to support block structured languages. They do not provide a jump or call to another procedure; they merely set up a new stack frame for an already called procedure. An ENTER instruction is commonly followed by a CALL, JMP, or Jcc instruction to transfer program control to the procedure being called.

If the nesting level is 0, the processor pushes the frame pointer from the EBP register onto the stack, copies the current stack pointer from the ESP register into the EBP register, and loads the ESP register with the current stack-pointer value minus the value in the size operand. For nesting levels of 1 or greater, the processor pushes additional frame pointers on the stack before adjusting the stack pointer. These additional frame pointers provide the called procedure with access points to other nested frames on the stack.

**Operation**

\[
\text{NestingLevel} \leftarrow \text{NestingLevel} \mod 32 \\
\text{IF StackSize} = 32 \\
\quad \text{THEN} \\
\quad \begin{aligned}
\text{Push(EBP)} ; \\
\text{FrameTemp} \leftarrow \text{ESP} ; \\
\text{ELSE ( StackSize = 16) } \\
\text{PUSH(BP)} ; \\
\text{FrameTemp} \leftarrow \text{SP} ;
\end{aligned}
\]

\FI\
\text{IF NestingLevel = 0 } \\
\quad \text{THEN GOTO CONTINUE;} \\
\FI\
\text{IF (NestingLevel > 0) } \\
\quad \text{FOR } i \leftarrow 1 \text{ TO (NestingLevel } - 1) \\
\quad \quad \text{DO } \\
\quad \quad \quad \text{IF OperandSize} = 32 \\
\quad \quad \quad \quad \text{THEN} \\
\quad \quad \quad \quad \quad \text{IF StackSize} = 32 \\
\quad \quad \quad \quad \quad \quad \text{EBP} \leftarrow \text{EBP} - 4;
ENTER—Make Stack Frame for Procedure Parameters (Continued)

Push([EBP]); (* doubleword push *)

ELSE (* StackSize = 16*)
	BP ← BP − 4;
	Push([BP]); (* doubleword push *)
FI;
ELSE (* OperandSize = 16 *)
IF StackSize = 32
	THEN
		EBP ← EBP − 2;
		Push([EBP]); (* word push *)
ELSE (* StackSize = 16*)
	BP ← BP − 2;
	Push([BP]); (* word push *)
FI;
FI;
OD;
IF OperandSize = 32
THEN
	Push(FrameTemp); (* doubleword push *)
ELSE (* OperandSize = 16 *)
	Push(FrameTemp); (* word push *)
FI;
GOTO CONTINUE;
FI;
CONTINUE:
IF StackSize = 32
THEN
	EBP ← FrameTemp
	ESP ← EBP − Size;
ELSE (* StackSize = 16*)
	BP ← FrameTemp
	SP ← BP − Size;
FI;
END;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults   NaT Register Consumption Abort.

Itanium Mem Faults
VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
ENTER—Make Stack Frame for Procedure Parameters (Continued)

Protected Mode Exceptions

#SS(0) If the new value of the SP or ESP register is outside the stack segment limit.

#PF(fault-code) If a page fault occurs.

Real Address Mode Exceptions

None.

Virtual 8086 Mode Exceptions

None.
F2XM1—Compute $2^x - 1$

### Opcode

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F0</td>
<td>F2XM1</td>
<td>Replace ST(0) with $(2^{ST(0)} - 1)$</td>
</tr>
</tbody>
</table>

### Description

Calculates the exponential value of 2 to the power of the source operand minus 1. The source operand is located in register ST(0) and the result is also stored in ST(0). The value of the source operand must lie in the range –1.0 to +1.0. If the source value is outside this range, the result is undefined.

The following table shows the results obtained when computing the exponential value of various classes of numbers, assuming that neither overflow nor underflow occurs:

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1.0 to 0</td>
<td>-0.5 to 0</td>
</tr>
<tr>
<td>-0</td>
<td>0</td>
</tr>
<tr>
<td>+0</td>
<td>0</td>
</tr>
<tr>
<td>+0 to +1.0</td>
<td>0.0 to 1.0</td>
</tr>
</tbody>
</table>

Values other than 2 can be exponentiated using the following formula:

$$\exists^y = 2^{y \times \log_2 x}$$

### Operation

$$ST(0) \leftarrow (2^{ST(0)} - 1);$$

### FPU Flags Affected

- **C1**: Set to 0 if stack underflow occurred. Indicates rounding direction if the inexact-result exception (#P) is generated:
  - 0 = not roundup; 1 = roundup.
- **C0, C2, C3**: Undefined.

### Additional Itanium® System Environment Exceptions

- **Itanium Reg Faults**: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

### Floating-point Exceptions

- **#IS**: Stack underflow occurred.
- **#IA**: Source operand is an SNaN value or unsupported format.
- **#D**: Result is a denormal value.
- **#U**: Result is too small for destination format.
- **#P**: Value cannot be represented exactly in destination format.
F2XM1—Compute $2^x - 1$ (Continued)

**Protected Mode Exceptions**

#NM EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM EM or TS in CR0 is set.
FABS—Absolute Value

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 E1</td>
<td>FABS</td>
<td>Replace ST with its absolute value.</td>
</tr>
</tbody>
</table>

**Description**

Clears the sign bit of ST(0) to create the absolute value of the operand. The following table shows the results obtained when creating the absolute value of various classes of numbers.

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>→</td>
<td>+∞</td>
</tr>
<tr>
<td>-F</td>
<td>+F</td>
</tr>
<tr>
<td>-0</td>
<td>+0</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
</tr>
<tr>
<td>+F</td>
<td>+F</td>
</tr>
<tr>
<td>+∞</td>
<td>+∞</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Note:  
F means finite-real number.

**Operation**

ST(0) ← |ST(0)|

**FPU Flags Affected**

C1 Set to 0 if stack underflow occurred; otherwise, cleared to 0.  
C0, C2, C3 Undefined.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

**Floating-point Exceptions**

#IS Stack underflow occurred.

**Protected Mode Exceptions**

#NM EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM EM or TS in CR0 is set.
FADD/FADDP/FIADD—Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /0</td>
<td>FADD m32 real</td>
<td>Add m32real to ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>DC /0</td>
<td>FADD m64real</td>
<td>Add m64real to ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>D8 C0+i</td>
<td>FADD ST(0), ST(i)</td>
<td>Add ST(0) to ST(i) and store result in ST(i)</td>
</tr>
<tr>
<td>DC C0+i</td>
<td>FADD ST(i), ST(0)</td>
<td>Add ST(i) to ST(0) and store result in ST(i)</td>
</tr>
<tr>
<td>DE C0+i</td>
<td>FADDP ST(i), ST(0)</td>
<td>Add ST(0) to ST(i), store result in ST(i), and pop the register stack</td>
</tr>
<tr>
<td>DE C1</td>
<td>FADDP</td>
<td>Add ST(0) to ST(1), store result in ST(1), and pop the register stack</td>
</tr>
<tr>
<td>DA /0</td>
<td>FIADD m32int</td>
<td>Add m32int to ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>DE /0</td>
<td>FIADD m16int</td>
<td>Add m16int to ST(0) and store result in ST(0)</td>
</tr>
</tbody>
</table>

Description

Adds the destination and source operands and stores the sum in the destination location. The destination operand is always an FPU register; the source operand can be a register or a memory location. Source operands in memory can be in single-real, double-real, word-integer, or short-integer formats.

The no-operand version of the instruction adds the contents of the ST(0) register to the ST(1) register. The one-operand version adds the contents of a memory location (either a real or an integer value) to the contents of the ST(0) register. The two-operand version, adds the contents of the ST(0) register to the ST(i) register or vice versa. The value in ST(0) can be doubled by coding:

```assembly
FADD ST(0), ST(0);
```

The FADDP instructions perform the additional operation of popping the FPU register stack after storing the result. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. (The no-operand version of the floating-point add instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FADD rather than FADDP.)

The FIADD instructions convert an integer source operand to extended-real format before performing the addition.

The table on the following page shows the results obtained when adding various classes of numbers, assuming that neither overflow nor underflow occurs.

When the sum of two operands with opposite signs is 0, the result is +0, except for the round toward −∞ mode, in which case the result is −0. When the source operand is an integer 0, it is treated as a +0.

When both operand are infinities of the same sign, the result is ∞ of the expected sign. If both operands are infinities of opposite signs, an invalid-operation exception is generated.
FADD/FADDP/FIADD—Add (Continued)

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>-∞</td>
<td>-∞</td>
</tr>
<tr>
<td>-F or -I</td>
<td>-∞</td>
</tr>
<tr>
<td>-0</td>
<td>-∞</td>
</tr>
<tr>
<td>±0</td>
<td>-∞</td>
</tr>
<tr>
<td>±For +I</td>
<td>-∞</td>
</tr>
<tr>
<td>±∞</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:
F means finite-real number.
L means integer.
* indicates floating-point invalid-arithmetic-operand (#IA) exception.

Operation
IF instruction is FIADD
THEN
    DEST ← DEST + ConvertExtendedReal(SRC);
ELSE (* source operand is real number *)
    DEST ← DEST + SRC;
FI;
IF instruction = FADDP
THEN
    PopRegisterStack;
FI;

FPU Flags Affected
C1
Set to 0 if stack underflow occurred.
Indicates rounding direction if the inexact-result exception (#P) is generated:
0 = not roundup; 1 = roundup.
C0, C2, C3
Undefined.

Additional Itanium® System Environment Exceptions
Itanium Reg Faults
Disabled FP Register Fault if PSR.dfl is 1, NaN Register Consumption Abort.
Itanium Mem Faults
VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaN Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
FADD/FADDP/FIADD—Add (Continued)

Floating-point Exceptions

#IS             Stack underflow occurred.
#IA             Operand is an SNaN value or unsupported format.
                Operands are infinities of unlike sign.
#D              Result is a denormal value.
#U              Result is too small for destination format.
#O              Result is too large for destination format.
#P              Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#GP(0)          If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
                If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0)          If a memory operand effective address is outside the SS segment limit.
#NM             EM or TS in CR0 is set.
#PF(fault-code) If a page fault occurs.
#AC(0)          If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP             If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS             If a memory operand effective address is outside the SS segment limit.
#NM             EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)          If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)          If a memory operand effective address is outside the SS segment limit.
#NM             EM or TS in CR0 is set.
#PF(fault-code) If a page fault occurs.
#AC(0)          If alignment checking is enabled and an unaligned memory reference is made.
FBLD—Load Binary Coded Decimal

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /4</td>
<td>FBLD m80 dec</td>
<td>Convert BCD value to real and push onto the FPU stack.</td>
</tr>
</tbody>
</table>

**Description**

Converts the BCD source operand into extended-real format and pushes the value onto the FPU stack. The source operand is loaded without rounding errors. The sign of the source operand is preserved, including that of −0.

The packed BCD digits are assumed to be in the range 0 through 9; the instruction does not check for invalid digits (AH through FH). Attempting to load an invalid encoding produces an undefined result.

**Operation**

\[
\text{TOP} \leftarrow \text{TOP} - 1; \\
\text{ST}(0) \leftarrow \text{ExtendedReal}(\text{SRC});
\]

**FPU Flags Affected**

- C1 Set to 1 if stack overflow occurred; otherwise, cleared to 0.
- C0, C2, C3 Undefined.

**Floating-point Exceptions**

- #IS Stack overflow occurred.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Protected Mode Exceptions**

- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #NM EM or TS in CR0 is set.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
FBLD—Load Binary Coded Decimal (Continued)

**Real Address Mode Exceptions**

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#NM  EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM   EM or TS in CR0 is set.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
FBSTP—Store BCD Integer and Pop

Description

Converts the value in the ST(0) register to an 18-digit packed BCD integer, stores the result in the destination operand, and pops the register stack. If the source value is a non-integral value, it is rounded to an integer value, according to rounding mode specified by the RC field of the FPU control word. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

The destination operand specifies the address where the first byte destination value is to be stored. The BCD value (including its sign bit) requires 10 bytes of space in memory.

The following table shows the results obtained when storing various classes of numbers in packed BCD format.

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>DEST</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(-\infty)</td>
<td>(*)</td>
<td>*</td>
</tr>
<tr>
<td>(-\infty &lt; -1)</td>
<td>(-D)</td>
<td>**</td>
</tr>
<tr>
<td>(-1 &lt; -F &lt; -0)</td>
<td>(*)</td>
<td>**</td>
</tr>
<tr>
<td>(-0)</td>
<td>(-0)</td>
<td>*</td>
</tr>
<tr>
<td>(+0)</td>
<td>(+0)</td>
<td>*</td>
</tr>
<tr>
<td>(+0 &lt; +F &lt; +1)</td>
<td>(*)</td>
<td>**</td>
</tr>
<tr>
<td>(+F &gt; +1)</td>
<td>(+D)</td>
<td>*</td>
</tr>
<tr>
<td>(+\infty)</td>
<td>(*)</td>
<td>*</td>
</tr>
<tr>
<td>(NaN)</td>
<td>(*)</td>
<td>*</td>
</tr>
</tbody>
</table>

Notes:
- \(F\) means finite-real number.
- \(D\) means packed-BCD number.
- \(*\) indicates floating-point invalid-operation (#IA) exception.
- \(**\) \(\pm0\) or \(\pm1\), depending on the rounding mode.

If the source value is too large for the destination format and the invalid-operation exception is not masked, an invalid-operation exception is generated and no value is stored in the destination operand. If the invalid-operation exception is masked, the packed BCD indefinite value is stored in memory.

If the source value is a quiet NaN, an invalid-operation exception is generated. Quiet NaNs do not normally cause this exception to be generated.

Operation

\[
\text{DEST} \leftarrow \text{BCD(ST(0))}; \\
\text{PopRegisterStack};
\]
FBSTP—Store BCD Integer and Pop (Continued)

FPU Flags Affected

C1  Set to 0 if stack underflow occurred.
    Indicates rounding direction if the inexact exception (#P) is generated: 0 = not
    roundup; 1 = roundup.

C0, C2, C3  Undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB
    Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data
    Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data
    Access Bit Fault, Data Dirty Bit Fault

Floating-point Exceptions

#IS  Stack underflow occurred.

#IA  Source operand is empty; contains a NaN, ±∞, or unsupported format; or
    contains value that exceeds 18 BCD digits in length.

#P  Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#GP(0)  If a segment register is being loaded with a segment selector that points to a
    nonwritable segment.
    If a memory operand effective address is outside the CS, DS, ES, FS, or GS
    segment limit.
    If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  EM or TS in CR0 is set.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made
    while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
    segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#NM  EM or TS in CR0 is set.
FBSTP—Store BCD Integer and Pop (Continued)

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM EM or TS in CR0 is set.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
FCHS—Change Sign

**Description**

Complements the sign bit of ST(0). This operation changes a positive value into a negative value of equal magnitude or vice-versa. The following table shows the results obtained when creating the absolute value of various classes of numbers.

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>±∞</td>
<td>±∞</td>
</tr>
<tr>
<td>−F</td>
<td>+F</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>+0</td>
<td>−0</td>
</tr>
<tr>
<td>+F</td>
<td>−F</td>
</tr>
<tr>
<td>±∞</td>
<td>±∞</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Note:

F means finite-real number.

**Operation**

\[ \text{SignBit(ST(0))} \leftarrow \text{NOT (SignBit(ST(0)))} \]

**FPU Flags Affected**

- **C1**: Set to 0 if stack underflow occurred; otherwise, cleared to 0.
- **C0, C2, C3**: Undefined.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

**Floating-point Exceptions**

- **#IS**: Stack underflow occurred.

**Protected Mode Exceptions**

- **#NM**: EM or TS in CR0 is set.

**Real Address Mode Exceptions**

- **#NM**: EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

- **#NM**: EM or TS in CR0 is set.
FCLEX/FNCLEX—Clear Exceptions

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DB E2</td>
<td>FCLEX</td>
<td>Clear floating-point exception flags after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>DB E2</td>
<td>FNCLEX</td>
<td>Clear floating-point exception flags without checking for pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

Description

Clears the floating-point exception flags (PE, UE, OE, ZE, DE, and IE), the exception summary status flag (ES), the stack fault flag (SF), and the busy flag (B) in the FPU status word. The FCLEX instruction checks for and handles any pending unmasked floating-point exceptions before clearing the exception flags; the FNCLEX instruction does not.

Operation

\[
\begin{align*}
\text{FPUStatusWord}[0..7] & \leftarrow 0; \\
\text{FPUStatusWord}[15] & \leftarrow 0;
\end{align*}
\]

FPU Flags Affected

The PE, UE, OE, ZE, DE, IE, ES, SF, and B flags in the FPU status word are cleared. The C0, C1, C2, and C3 flags are undefined.

Floating-point Exceptions

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Protected Mode Exceptions

#NM EM or TS in CR0 is set.

Real Address Mode Exceptions

#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#NM EM or TS in CR0 is set.
FCMOVcc—Floating-point Conditional Move

Description

Tests the status flags in the EFLAGS register and moves the source operand (second operand) to the destination operand (first operand) if the given test condition is true. The source operand is always in the ST(i) register and the destination operand is always ST(0).

The FCMOVcc instructions are useful for optimizing small IF constructions. They also help eliminate branching overhead for IF operations and the possibility of branch mispredictions by the processor.

A processor in the Pentium Pro processor family may not support the FCMOVcc instructions. Software can check if the FCMOVcc instructions are supported by checking the processor’s feature information with the CPUID instruction (see “CPUID—CPU Identification” on page 3:428). If both the CMOV and FPU feature bits are set, the FCMOVcc instructions are supported.

Operation

IF condition TRUE
   ST(0) ← ST(i)
FI;

FPU Flags Affected

C1  Set to 0 if stack underflow occurred.
C0, C2, C3  Undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Floating-point Exceptions

#IS  Stack underflow occurred.

Integer Flags Affected

None.
FCMOVcc—Floating-point Conditional Move (Continued)

**Protected Mode Exceptions**

#NM EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM EM or TS in CR0 is set.
FCOM/FCOMP/FCOMPP—Compare Real

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /2</td>
<td>FCOM m32real</td>
<td>Compare ST(0) with m32real.</td>
</tr>
<tr>
<td>DC /2</td>
<td>FCOM m64real</td>
<td>Compare ST(0) with m64real.</td>
</tr>
<tr>
<td>D8 D0+i</td>
<td>FCOM ST(i)</td>
<td>Compare ST(0) with ST(i).</td>
</tr>
<tr>
<td>D8 D1</td>
<td>FCOM</td>
<td>Compare ST(0) with ST(1).</td>
</tr>
<tr>
<td>D8 /3</td>
<td>FCOMP m32real</td>
<td>Compare ST(0) with m32real and pop register stack.</td>
</tr>
<tr>
<td>DC /3</td>
<td>FCOMP m64real</td>
<td>Compare ST(0) with m64real and pop register stack.</td>
</tr>
<tr>
<td>D8 D8+i</td>
<td>FCOMP ST(i)</td>
<td>Compare ST(0) with ST(i) and pop register stack.</td>
</tr>
<tr>
<td>D8 D9</td>
<td>FCOMP</td>
<td>Compare ST(0) with ST(1) and pop register stack.</td>
</tr>
<tr>
<td>DE D9</td>
<td>FCOMPP</td>
<td>Compare ST(0) with ST(1) and pop register stack twice.</td>
</tr>
</tbody>
</table>

Description

Compares the contents of register ST(0) and source value and sets condition code flags C0, C2, and C3 in the FPU status word according to the results (see the table below). The source operand can be a data register or a memory location. If no source operand is given, the value in ST(0) is compared with the value in ST(1). The sign of zero is ignored, so that –0.0 = +0.0.

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; SRC</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; SRC</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = SRC</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordereda</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

a. Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.

This instruction checks the class of the numbers being compared. If either operand is a NaN or is in an unsupported format, an invalid-arithmetic-operand exception (#IA) is raised and, if the exception is masked, the condition flags are set to “unordered.” If the invalid-arithmetic-operand exception is unmasked, the condition code flags are not set.

The FCOMP instruction pops the register stack following the comparison operation and the FCOMPP instruction pops the register stack twice following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

The FCOM instructions perform the same operation as the FUCOM instructions. The only difference is how they handle QNaN operands. The FCOM instructions raise an invalid-arithmetic-operand exception (#IA) when either or both of the operands is a NaN value or is in an unsupported format. The FUCOM instructions perform the same operation as the FCOM instructions, except that they do not generate an invalid-arithmetic-operand exception for QNaNs.
FCOM/FCOMP/FCOMPP—Compare Real (Continued)

Operation

CASE (relation of operands) OF

ST > SRC: C3, C2, C0 ← 000;
ST < SRC: C3, C2, C0 ← 001;
ST = SRC: C3, C2, C0 ← 100;

ESAC;

IF ST(0) or SRC = NaN or unsupported format
THEN
    #IA
    IF FPUControlWord.IM = 1
        THEN
            C3, C2, C0 ← 111;
    FI;
FI;

IF instruction = FCOMP
THEN
    PopRegisterStack;
FI;

IF instruction = FCOMPP
THEN
    PopRegisterStack;
    PopRegisterStack;
FI;

FPU Flags Affected

C1 Set to 0 if stack underflow occurred; otherwise, cleared to 0.
C0, C2, C3 See table on previous page.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Floating-point Exceptions

#IS Stack underflow occurred.
#IA One or both operands are NaN values or have unsupported formats.
    Register is marked empty.
#D One or both operands are denormal values.
FCOM/FCOMP/FCOMPP—Compare Real (Continued)

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
FCOMI/FCOMIP/FUCOMI/FUCOMIP—Compare Real and Set EFLAGS

**Description**

Compares the contents of register ST(0) and ST(i) and sets the status flags ZF, PF, and CF in the EFLAGS register according to the results (see the table below). The sign of zero is ignored for comparisons, so that –0.0 = +0.0.

<table>
<thead>
<tr>
<th>Comparison Results</th>
<th>ZF</th>
<th>PF</th>
<th>CF</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST0 &gt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST0 &lt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST0 = ST(i)</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered&lt;sup&gt;a&lt;/sup&gt;</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

<sup>a</sup> Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.

The FCOMI/FCOMIP instructions perform the same operation as the FUCOMI/FUCOMIP instructions. The only difference is how they handle QNaN operands. The FCOMI/FCOMIP instructions set the status flags to “unordered” and generate an invalid-arithmetic-operand exception (#IA) when either or both of the operands is a NaN value (SNaN or QNaN) or is in an unsupported format.

The FUCOMI/FUCOMIP instructions perform the same operation as the FCOMI/FCOMIP instructions, except that they do not generate an invalid-arithmetic-operand exception for QNaNs.

If invalid-operation exception is unmasked, the status flags are not set if the invalid-arithmetic-operand exception is generated.

The FCOMIP and FUCOMIP instructions also pop the register stack following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.
FCOMI/FCOMIP/FUCOMI/FUCOMIP—Compare Real and Set EFLAGS
(Continued)

**Operation**

\[
\text{CASE (relation of operands) OF} \\
\begin{align*}
\text{ST}(0) &> \text{ST}(i) & \text{ZF, PF, CF} &\leftarrow 000; \\
\text{ST}(0) &< \text{ST}(i) & \text{ZF, PF, CF} &\leftarrow 001; \\
\text{ST}(0) &= \text{ST}(i) & \text{ZF, PF, CF} &\leftarrow 100;
\end{align*}
\]

ESAC;

IF instruction is FCOMI or FCOMIP

THEN

\[
\begin{align*}
\text{IF } \text{ST}(0) \text{ or } \text{ST}(i) &= \text{NaN or unsupported format} & \text{THEN} \\
\text{#IA} & \text{IF FPUControlWord.IM} = 1 & \text{THEN} \\
\text{ZF, PF, CF} &\leftarrow 111; \\
\text{FI}; \\
\text{FI}; \\
\text{FI}; \\
\end{align*}
\]

IF instruction is FUCOMI or FUCOMIP

THEN

\[
\begin{align*}
\text{IF } \text{ST}(0) \text{ or } \text{ST}(i) &= \text{QNaN, but not SNaN or unsupported format} & \text{THEN} \\
\text{ZF, PF, CF} &\leftarrow 111; \\
\text{ELSE } (*) \text{ ST}(0) \text{ or ST}(i) \text{ is SNaN or unsupported format } & \text{#IA}; \\
\text{IF FPUControlWord.IM} = 1 & \text{THEN} \\
\text{ZF, PF, CF} &\leftarrow 111; \\
\text{FI}; \\
\text{FI}; \\
\text{FI};
\end{align*}
\]

IF instruction is FCOMIP or FUCOMIP

THEN

\[
\text{PopRegisterStack;}
\]

FI;

**FPU Flags Affected**

- **C1** Set to 0 if stack underflow occurred; otherwise, cleared to 0.
- **C0, C2, C3** Not affected.

**Additional Itanium® System Environment Exceptions**

- **Itanium Reg Faults** Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Floating-point Exceptions

#IS Stack underflow occurred.

#IA (FCOMI or FCOMIP instruction) One or both operands are NaN values or have unsupported formats.

(FUCOMI or FUCOMIP instruction) One or both operands are SNaN values (but not QNaNs) or have undefined formats. Detection of a QNaN value does not raise an invalid-operand exception.

Protected Mode Exceptions

#NM EM or TS in CR0 is set.

Real Address Mode Exceptions

#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#NM EM or TS in CR0 is set.
FCOS—Cosine

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 FF</td>
<td>FCOS</td>
<td>Replace ST(0) with its cosine</td>
</tr>
</tbody>
</table>

Description

Calculates the cosine of the source operand in register ST(0) and stores the result in ST(0). The source operand must be given in radians and must be within the range $-2^{63}$ to $+2^{63}$. The following table shows the results obtained when taking the cosine of various classes of numbers, assuming that neither overflow nor underflow occurs.

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$</td>
<td>*</td>
</tr>
<tr>
<td>$-F$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$-0$</td>
<td>$+1$</td>
</tr>
<tr>
<td>$+0$</td>
<td>$+1$</td>
</tr>
<tr>
<td>$+F$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$+\infty$</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:
- $F$ means finite-real number.
- * indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range $-2^{63}$ to $+2^{63}$ can be reduced to the range of the instruction by subtracting an appropriate integer multiple of $2\pi$ or by using the FPREM instruction with a divisor of $2\pi$.

Operation

```
IF |ST(0)| < $2^{63}$
THEN
    C2 ← 0;
    ST(0) ← cosine(ST(0));
ELSE (*source operand is out-of-range *)
    C2 ← 1;
FI;
```
FCOS—Cosine (Continued)

FPU Flags Affected

C1 \( \text{Set to 0 if stack underflow occurred.} \)
\( \text{Indicates rounding direction if the inexact-result exception (#P) is generated:} \)
\( 0 = \text{not roundup; } 1 = \text{roundup.} \)
\( \text{Undefined if C2 is 1.} \)

C2 \( \text{Set to 1 if source operand is outside the range } -2^{63} \text{ to } +2^{63}; \text{ otherwise, cleared to 0.} \)

C0, C3 \( \text{Undefined.} \)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults \( \text{Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.} \)

Floating-point Exceptions

#IS \( \text{Stack underflow occurred.} \)
#IA \( \text{Source operand is an SNaN value, } \infty, \text{ or unsupported format.} \)
#D \( \text{Result is a denormal value.} \)
#U \( \text{Result is too small for destination format.} \)
#P \( \text{Value cannot be represented exactly in destination format.} \)

Protected Mode Exceptions

#NM \( \text{EM or TS in CR0 is set.} \)

Real Address Mode Exceptions

#NM \( \text{EM or TS in CR0 is set.} \)

Virtual 8086 Mode Exceptions

#NM \( \text{EM or TS in CR0 is set.} \)
FDECSTP—Decrement Stack-Top Pointer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F6</td>
<td>FDECSTP</td>
<td>Decrement TOP field in FPU status word.</td>
</tr>
</tbody>
</table>

**Description**
Subtracts one from the TOP field of the FPU status word (decrements the top-of-stack pointer). The contents of the FPU data registers and tag register are not affected.

**Operation**

IF TOP = 0
    THEN TOP ← 7;
ELSE TOP ← TOP – 1;
FI;

**FPU Flags Affected**
The C1 flag is set to 0; otherwise, cleared to 0. The C0, C2, and C3 flags are undefined.

**Floating-point Exceptions**
None.

**Additional Itanium® System Environment Exceptions**
Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

**Protected Mode Exceptions**

#NM EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM EM or TS in CR0 is set.
FDIV/FDIVP/FIDIV—Divide

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DB /6</td>
<td>FDIV m32real</td>
<td>Divide ST(0) by m32real and store result in ST(0)</td>
</tr>
<tr>
<td>DC /6</td>
<td>FDIV m64real</td>
<td>Divide ST(0) by m64real and store result in ST(0)</td>
</tr>
<tr>
<td>DB F0+i</td>
<td>FDIV ST(0), ST(i)</td>
<td>Divide ST(0) by ST(i) and store result in ST(i)</td>
</tr>
<tr>
<td>DC F8+i</td>
<td>FDIV ST(i), ST(0)</td>
<td>Divide ST(i) by ST(0) and store result in ST(i)</td>
</tr>
<tr>
<td>DE F8+i</td>
<td>FDIVP ST(i), ST(0)</td>
<td>Divide ST(i) by ST(0), store result in ST(i), and pop the register stack</td>
</tr>
<tr>
<td>DE F9</td>
<td>FDIVP</td>
<td>Divide ST(1) by ST(0), store result in ST(1), and pop the register stack</td>
</tr>
<tr>
<td>DA /6</td>
<td>FIDIV m32int</td>
<td>Divide ST(0) by m32int and store result in ST(0)</td>
</tr>
<tr>
<td>DE /6</td>
<td>FIDIV m16int</td>
<td>Divide ST(0) by m16int and store result in ST(0)</td>
</tr>
</tbody>
</table>

Description

Divides the destination operand by the source operand and stores the result in the destination location. The destination operand (dividend) is always in an FPU register; the source operand (divisor) can be a register or a memory location. Source operands in memory can be in single-real, double-real, word-integer, or short-integer formats.

The no-operand version of the instruction divides the contents of the ST(1) register by the contents of the ST(0) register. The one-operand version divides the contents of the ST(0) register by the contents of a memory location (either a real or an integer value). The two-operand version, divides the contents of the ST(0) register by the contents of the ST(i) register or vice versa.

The FDIVP instructions perform the additional operation of popping the FPU register stack after storing the result. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point divide instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FDIV rather than FDIVP.

The FIDIV instructions convert an integer source operand to extended-real format before performing the division. When the source operand is an integer 0, it is treated as a +0.

If an unmasked divide by zero exception (#Z) is generated, no result is stored; if the exception is masked, an \( \infty \) of the appropriate sign is stored in the destination operand.

The following table shows the results obtained when dividing various classes of numbers, assuming that neither overflow nor underflow occurs.
FDIV/FDIVP/FIDIV—Divide (Continued)

### Notes:
- F means finite-real number.
- I means integer.
- * indicates floating-point invalid-arithmetic-operand (#IA) exception.
- ** indicates floating-point zero-divide (#Z) exception.

### Operation

**IF SRC = 0**

**THEN**

#Z

**ELSE**

**IF instruction is FIDIV**

**THEN**

DEST ← DEST / ConvertExtendedReal(SRC);

**ELSE** (* source operand is real number *)

DEST ← DEST / SRC;

FI;

FI;

**IF instruction = FDIVP**

**THEN**

PopRegisterStack

FI;

### FPU Flags Affected

**C1**

Set to 0 if stack underflow occurred.

Indicates rounding direction if the inexact-result exception (#P) is generated:

0 = not roundup; 1 = roundup.

**C0, C2, C3**

Undefined.
FDIV/FDIVP/FIDIV—Divide (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults
Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Itanium Mem Faults
VTQ Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Floating-point Exceptions

#IS Stack underflow occurred.
#IA Operand is an SNaN value or unsupported format.
±∞ / ±∞; ±0 / ±0
#D Result is a denormal value.
#Z DEST / ±0, where DEST is not equal to ±0.
#U Result is too small for destination format.
#O Result is too large for destination format.
#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
FDIVR/FDIVRP/FIDIVR—Reverse Divide

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /7</td>
<td>FDIVR m32real</td>
<td>Divide m32real by ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>DC /7</td>
<td>FDIVR m64real</td>
<td>Divide m64real by ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>D8 F8+i</td>
<td>FDIVR ST(0), ST(i)</td>
<td>Divide ST(i) by ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>DC F0+i</td>
<td>FDIVR ST(i), ST(0)</td>
<td>Divide ST(0) by ST(i) and store result in ST(i)</td>
</tr>
<tr>
<td>DE F0+i</td>
<td>FDIVRP ST(i), ST(0)</td>
<td>Divide ST(0) by ST(i), store result in ST(i), and pop the register stack</td>
</tr>
<tr>
<td>DE F1</td>
<td>FDIVRP</td>
<td>Divide ST(0) by ST(1), store result in ST(1), and pop the register stack</td>
</tr>
<tr>
<td>DA /7</td>
<td>FIDIVR m32int</td>
<td>Divide m32int by ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>DE /7</td>
<td>FIDIVR m16int</td>
<td>Divide m64int by ST(0) and store result in ST(0)</td>
</tr>
</tbody>
</table>

Description

Divides the source operand by the destination operand and stores the result in the destination location. The destination operand (divisor) is always in an FPU register; the source operand (dividend) can be a register or a memory location. Source operands in memory can be in single-real, double-real, word-integer, or short-integer formats.

These instructions perform the reverse operations of the FDIV, FDIVP, and FIDIV instructions. They are provided to support more efficient coding.

The no-operand version of the instruction divides the contents of the ST(0) register by the contents of the ST(1) register. The one-operand version divides the contents of a memory location (either a real or an integer value) by the contents of the ST(0) register. The two-operand version, divides the contents of the ST(i) register by the contents of the ST(0) register or vice versa.

The FDIVRP instructions perform the additional operation of popping the FPU register stack after storing the result. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point divide instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FDIVR rather than FDIVRP.

The FIDIVR instructions convert an integer source operand to extended-real format before performing the division.

If an unmasked divide by zero exception (#Z) is generated, no result is stored; if the exception is masked, an \( \infty \) of the appropriate sign is stored in the destination operand.

The following table shows the results obtained when dividing various classes of numbers, assuming that neither overflow nor underflow occurs.
FDIVR/FDIVRP/FIDIVR—Reverse Divide (Continued)

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
<th>−∞</th>
<th>−F</th>
<th>−0</th>
<th>+0</th>
<th>+F</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>*</td>
<td>+∞</td>
<td>0</td>
<td>−F</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>+0</td>
<td>+F</td>
<td>0</td>
<td>−0</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−I</td>
<td>+0</td>
<td>+F</td>
<td>0</td>
<td>−F</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>+0</td>
<td>+F</td>
<td>0</td>
<td>−F</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>−0</td>
<td>−F</td>
<td>0</td>
<td>+F</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+I</td>
<td>−0</td>
<td>−F</td>
<td>0</td>
<td>+F</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>−0</td>
<td>−F</td>
<td>0</td>
<td>+F</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>*</td>
<td>−∞</td>
<td>0</td>
<td>−F</td>
<td>+0</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:
F means finite-real number.
I means integer.
* indicates floating-point invalid-arithmetic-operand (#IA) exception.
** indicates floating-point zero-divide (#Z) exception.

When the source operand is an integer 0, it is treated as a +0.

Operation

IF DEST = 0
THEN
  #Z
ELSE
  IF instruction is FIDIVR
  THEN
    DEST ← ConvertExtendedReal(SRC) / DEST;
  ELSE (* source operand is real number *)
    DEST ← SRC / DEST;
  FI;
FI;
IF instruction = FDIVRP
THEN
  PopRegisterStack
FI;

FPU Flags Affected

C1
  Set to 0 if stack underflow occurred.
  Indicates rounding direction if the inexact-result exception (#P) is generated:
  0 = not roundup; 1 = roundup.

C0, C2, C3
  Undefined.
FDIVR/FDIVRP/FIDIVR—Reverse Divide (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Floating-point Exceptions

#IS  Stack underflow occurred.
#IA  Operand is an SNaN value or unsupported format.
     ±∞ / ±∞; ±0 / ±0
#D  Result is a denormal value.
#Z  SRC / ±0, where SRC is not equal to ±0.
#U  Result is too small for destination format.
#O  Result is too large for destination format.
#P  Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
FFREE—Free Floating-point Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DD C0+i</td>
<td>FFREE ST(i)</td>
<td>Sets tag for ST(i) to empty</td>
</tr>
</tbody>
</table>

**Description**

Sets the tag in the FPU tag register associated with register ST(i) to empty (11B). The contents of ST(i) and the FPU stack-top pointer (TOP) are not affected.

**Operation**

TAG(i) ← 11B;

**FPU Flags Affected**

C0, C1, C2, C3 undefined.

**Floating-point Exceptions**

None.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1.

**Protected Mode Exceptions**

#NM EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM EM or TS in CR0 is set.
FICOM/FICOMP—Compare Integer

Description

Compares the value in ST(0) with an integer source operand and sets the condition code flags C0, C2, and C3 in the FPU status word according to the results (see table below). The integer value is converted to extended-real format before the comparison is made.

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; SRC</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; SRC</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = SRC</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

These instructions perform an “unordered comparison.” An unordered comparison also checks the class of the numbers being compared. If either operand is a NaN or is in an undefined format, the condition flags are set to “unordered.”

The sign of zero is ignored, so that –0.0 = +0.0.

The FICOMP instructions pop the register stack following the comparison. To pop the register stack, the processor marks the ST(0) register empty and increments the stack pointer (TOP) by 1.

Operation

\[
\text{CASE (relation of operands) OF} \\
\text{ST(0) > SRC: C3, C2, C0 ← 000;} \\
\text{ST(0) < SRC: C3, C2, C0 ← 001;} \\
\text{ST(0) = SRC: C3, C2, C0 ← 100;} \\
\text{Unordered: C3, C2, C0 ← 111;}
\]

\text{ESAC;}

\text{IF instruction = FICOMP}
\text{THEN}
\text{PopRegisterStack;}
\text{FI;}

FPU Flags Affected

C1 Set to 0 if stack underflow occurred; otherwise, set to 0.

C0, C2, C3 See table on previous page.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DE /2</td>
<td>FICOM m16int</td>
<td>Compare ST(0) with m16int</td>
</tr>
<tr>
<td>DA /2</td>
<td>FICOM m32int</td>
<td>Compare ST(0) with m32int</td>
</tr>
<tr>
<td>DE /3</td>
<td>FICOMP m16int</td>
<td>Compare ST(0) with m16int and pop stack register</td>
</tr>
<tr>
<td>DA /3</td>
<td>FICOMP m32int</td>
<td>Compare ST(0) with m32int and pop stack register</td>
</tr>
</tbody>
</table>
**FICOM/FICOMP—Compare Integer (Continued)**

**Additional Itanium® System Environment Exceptions**

- **Itanium Reg Faults**
  - Disabled FP Register Fault if PSR.df1 is 1, NaT Register Consumption Abort.

- **Itanium Mem Faults**
  - VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Floating-point Exceptions**

- **#IS**
  - Stack underflow occurred.
- **#IA**
  - One or both operands are NaN values or have unsupported formats.
- **#D**
  - One or both operands are denormal values.

**Protected Mode Exceptions**

- **#GP(0)**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.

- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.

- **#NM**
  - EM or TS in CR0 is set.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real Address Mode Exceptions**

- **#GP**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS**
  - If a memory operand effective address is outside the SS segment limit.

- **#NM**
  - EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

- **#GP(0)**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.

- **#NM**
  - EM or TS in CR0 is set.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made.
FILD—Load Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /0</td>
<td>FILD m16int</td>
<td>Push m16int onto the FPU register stack.</td>
</tr>
<tr>
<td>DB /0</td>
<td>FILD m32int</td>
<td>Push m32int onto the FPU register stack.</td>
</tr>
<tr>
<td>DF /5</td>
<td>FILD m64int</td>
<td>Push m64int onto the FPU register stack.</td>
</tr>
</tbody>
</table>

Description

Converts the signed-integer source operand into extended-real format and pushes the value onto the FPU register stack. The source operand can be a word, short, or long integer value. It is loaded without rounding errors. The sign of the source operand is preserved.

Operation

\[
\text{TOP} \leftarrow \text{TOP} - 1; \\
\text{ST}(0) \leftarrow \text{ExtendedReal}(\text{SRC});
\]

FPU Flags Affected

- C1 Set to 1 if stack overflow occurred; cleared to 0 otherwise.
- C0, C2, C3 Undefined.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Floating-point Exceptions

- #IS Stack overflow occurred.

Protected Mode Exceptions

- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  
  If the DS, ES, FS, or GS register contains a null segment selector.

- #SS(0) If a memory operand effective address is outside the SS segment limit.

- #NM EM or TS in CR0 is set.

- #PF(fault-code) If a page fault occurs.

- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
FILD—Load Integer (Continued)

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
FINCSTP—Increment Stack-Top Pointer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F7</td>
<td>FINCSTP</td>
<td>Increment the TOP field in the FPU status register</td>
</tr>
</tbody>
</table>

**Description**

Adds one to the TOP field of the FPU status word (increments the top-of-stack pointer). The contents of the FPU data registers and tag register are not affected. This operation is not equivalent to popping the stack, because the tag for the previous top-of-stack register is not marked empty.

**Operation**

\[
\text{IF } \text{TOP} = 7 \\
\quad \text{THEN } \text{TOP} \leftarrow 0; \\
\quad \text{ELSE } \text{TOP} \leftarrow \text{TOP} + 1; \\
\text{FI}; \\
\]

**FPU Flags Affected**

The C1 flag is set to 0; otherwise, generates an #IS fault. The C0, C2, and C3 flags are undefined.

**Floating-point Exceptions**

#IS

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1.

**Protected Mode Exceptions**

#NM EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM EM or TS in CR0 is set.
FINIT/FNINIT—Initialize Floating-point Unit

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DB E3</td>
<td>FINIT</td>
<td>Initialize FPU after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>DB E3</td>
<td>FNINIT</td>
<td>Initialize FPU without checking for pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

**Description**

Sets the FPU control, status, tag, instruction pointer, and data pointer registers to their default states. The FPU control word is set to 037FH (round to nearest, all exceptions masked, 64-bit precision). The status word is cleared (no exception flags set, TOP is set to 0). The data registers in the register stack are left unchanged, but they are all tagged as empty (11B). Both the instruction and data pointers are cleared.

The FINIT instruction checks for and handles any pending unmasked floating-point exceptions before performing the initialization; the FNINIT instruction does not.

**Operation**

\[
\begin{align*}
\text{FPUCW} & \leftarrow 037FH; \\
\text{FPUStatus} & \leftarrow 0; \\
\text{FPUTag} & \leftarrow FFFFH; \\
\text{FPUData} & \leftarrow 0; \\
\text{FPUInst} & \leftarrow 0; \\
\text{FPULastInstOpcode} & \leftarrow 0;
\end{align*}
\]

**FPU Flags Affected**

C0, C1, C2, C3 cleared to 0.

**Floating-point Exceptions**

None.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1.

**Protected Mode Exceptions**

#NM EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM EM or TS in CR0 is set.
FIST/FISTP—Store Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DF /2</td>
<td>FIST m16int</td>
<td>Store ST(0) in m16int</td>
</tr>
<tr>
<td>DB /2</td>
<td>FIST m32int</td>
<td>Store ST(0) in m32int</td>
</tr>
<tr>
<td>DF /3</td>
<td>FISTP m16int</td>
<td>Store ST(0) in m16int and pop register stack</td>
</tr>
<tr>
<td>DB /3</td>
<td>FISTP m32int</td>
<td>Store ST(0) in m32int and pop register stack</td>
</tr>
<tr>
<td>DF /7</td>
<td>FISTP m64int</td>
<td>Store ST(0) in m64int and pop register stack</td>
</tr>
</tbody>
</table>

Description

The FIST instruction converts the value in the ST(0) register to a signed integer and stores the result in the destination operand. Values can be stored in word- or short-integer format. The destination operand specifies the address where the first byte of the destination value is to be stored.

The FISTP instruction performs the same operation as the FIST instruction and then pops the register stack. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The FISTP instruction can also stores values in long-integer format.

The following table shows the results obtained when storing various classes of numbers in integer format.

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>*</td>
</tr>
<tr>
<td>−F &lt; −1</td>
<td>−l</td>
</tr>
<tr>
<td>−1 &lt; −F &lt; −0</td>
<td>**</td>
</tr>
<tr>
<td>−0</td>
<td>0</td>
</tr>
<tr>
<td>+0</td>
<td>0</td>
</tr>
<tr>
<td>+0 &lt; +F &lt; +1</td>
<td>**</td>
</tr>
<tr>
<td>+F &gt; +1</td>
<td>+1</td>
</tr>
<tr>
<td>+∞</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>*</td>
</tr>
</tbody>
</table>

Notes:

F means finite-real number.
I means integer.
* indicates floating-point invalid-operation (#IA) exception.
** ±0 or ±1, depending on the rounding mode.

If the source value is a non-integral value, it is rounded to an integer value, according to the rounding mode specified by the RC field of the FPU control word.

If the value being stored is too large for the destination format, is an ∞, is a NaN, or is in an unsupported format and if the invalid-arithmetic-operand exception (#IA) is unmasked, an invalid-operation exception is generated and no value is stored in the destination operand. If the invalid-operation exception is masked, the integer indefinite value is stored in the destination operand.
FIST/FISTP—Store Integer (Continued)

Operation

\[
\text{DEST} \leftarrow \text{Integer(ST(0))};
\]
\[
\text{IF instruction = FISTP}
\]
\[
\text{THEN}
\]
\[
\text{PopRegisterStack;}
\]
\[
\text{FI;}
\]

FPU Flags Affected

- **C1**
  - Set to 0 if stack underflow occurred.
  - Indicates rounding direction of if the inexact exception (#P) is generated:
    - 0 = not roundup; 1 = roundup.
  - Cleared to 0 otherwise.

- **C0, C2, C3**
  - Undefined.

Additional Itanium® System Environment Exceptions

- **Itanium Reg Faults**
  - Disabled FP Register Fault if PSR.dfl is 1, NaT register Consumption Abort.

- **Itanium Mem Faults**
  - VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Floating-point Exceptions

- **#IS**
  - Stack underflow occurred.

- **#IA**
  - Source operand is too large for the destination format
  - Source operand is a NaN value or unsupported format.

- **#P**
  - Value cannot be represented exactly in destination format.

Protected Mode Exceptions

- **#GP(0)**
  - If the destination is located in a nonwritable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.

- **#NM**
  - EM or TS in CR0 is set.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
FIST/FISTP—Store Integer (Continued)

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  EM or TS in CR0 is set.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
FLD—Load Real

**Description**

Pushes the source operand onto the FPU register stack. If the source operand is in single- or double-real format, it is automatically converted to the extended-real format before being pushed on the stack.

The FLD instruction can also push the value in a selected FPU register \([ST(i)]\) onto the stack. Here, pushing register ST(0) duplicates the stack top.

**Operation**

\[
\text{IF SRC is ST}(i) \\
\quad \text{THEN} \\
\quad \quad \text{temp} \leftarrow \text{ST}(i) \\
\quad \text{TOP} \leftarrow \text{TOP} - 1; \\
\text{IF SRC is memory-operand} \\
\quad \text{THEN} \\
\quad \quad \text{ST}(0) \leftarrow \text{ExtendedReal(SRC)}; \\
\quad \text{ELSE (* SRC is ST}(i) *) \\
\quad \quad \text{ST}(0) \leftarrow \text{temp};
\]

**FPU Flags Affected**

- C1 Set to 1 if stack overflow occurred; otherwise, cleared to 0.
- C0, C2, C3 Undefined.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Floating-point Exceptions**

- #IS Stack overflow occurred.
- #IA Source operand is an SNaN value or unsupported format.
- #D Source operand is a denormal value. Does not occur if the source operand is in extended-real format.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 /0</td>
<td>FLD m32real</td>
<td>Push m32real onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 /i</td>
<td>FLD ST(i)</td>
<td>Push ST(i) onto the FPU register stack.</td>
</tr>
<tr>
<td>DD /0</td>
<td>FLD m64real</td>
<td>Push m64real onto the FPU register stack.</td>
</tr>
<tr>
<td>DB /5</td>
<td>FLD m80real</td>
<td>Push m80real onto the FPU register stack.</td>
</tr>
</tbody>
</table>
Protected Mode Exceptions

#GP(0)  If destination is located in a nonwritable segment.
        If a memory operand effective address is outside the CS, DS, ES, FS, or GS
        segment limit.
        If the DS, ES, FS, or GS register is used to access memory and it contains a
        null segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM     EM or TS in CR0 is set.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made
        while the current privilege level is 3.

Real Address Mode Exceptions

#GP     If a memory operand effective address is outside the CS, DS, ES, FS, or GS
        segment limit.

#SS     If a memory operand effective address is outside the SS segment limit.

#NM     EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
        segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM     EM or TS in CR0 is set.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
FLD1/FLDL2T/FLDL2E/FLDPI/FLDLG2/FLDLN2/FLDZ—Load Constant

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 E8</td>
<td>FLD1</td>
<td>Push +1.0 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 E9</td>
<td>FLDL2T</td>
<td>Push log₂10 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EA</td>
<td>FLDL2E</td>
<td>Push log₂e onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EB</td>
<td>FLDPI</td>
<td>Push π onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EC</td>
<td>FLDLQ2</td>
<td>Push log₁₀2 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 ED</td>
<td>FLDLN2</td>
<td>Push logₑ2 onto the FPU register stack.</td>
</tr>
<tr>
<td>D9 EE</td>
<td>FLDZ</td>
<td>Push +0.0 onto the FPU register stack.</td>
</tr>
</tbody>
</table>

**Description**

Push one of seven commonly-used constants (in extended-real format) onto the FPU register stack. The constants that can be loaded with these instructions include +1.0, +0.0, log₂10, logₑ2, π, log₁₀₂, and logₑ₂. For each constant, an internal 66-bit constant is rounded (as specified by the RC field in the FPU control word) to external-real format. The inexact-result exception (#P) is not generated as a result of the rounding.

**Operation**

\[
\text{TOP} \leftarrow \text{TOP} - 1; \\
\text{ST}(0) \leftarrow \text{CONSTANT};
\]

**FPU Flags Affected**

- C1: Set to 1 if stack overflow occurred; otherwise, cleared to 0.
- C0, C2, C3: Undefined.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1.

**Floating-point Exceptions**

- #IS: Stack overflow occurred.

**Protected Mode Exceptions**

- #NM: EM or TS in CR0 is set.

**Real Address Mode Exceptions**

- #NM: EM or TS in CR0 is set.
FLD1/FLDL2T/FLDL2E/FLDPI/FLDLG2/FLDLN2/FLDZ—Load Constant (Continued)

Virtual 8086 Mode Exceptions

#NM EM or TS in CR0 is set.

Intel® Architecture Compatibility Information

When the RC field is set to round-to-nearest, the FPU produces the same constants that is produced by the Intel 8087 and Intel287 math coprocessors.
FLDCW—Load Control Word

Description
Loads the 16-bit source operand into the FPU control word. The source operand is a memory location. This instruction is typically used to establish or change the FPU’s mode of operation.

If one or more exception flags are set in the FPU status word prior to loading a new FPU control word and the new control word unmasks one or more of those exceptions, a floating-point exception will be generated upon execution of the next floating-point instruction (except for the no-wait floating-point instructions). To avoid raising exceptions when changing FPU operating modes, clear any pending exceptions (using the FCLEX or FNCLEX instruction) before loading the new control word.

Operation
FPUCtrlWord ← SRC;

FPU Flags Affected
C0, C1, C2, C3 undefined.

Floating-point Exceptions
None; however, this operation might unmask a pending exception in the FPU status word. That exception is then generated upon execution of the next waiting floating-point instruction.

Additional Itanium® System Environment Exceptions
Itanium Reg Faults      Disabled FP Register Fault if PSR.dfl is 1.
Itanium Mem Faults     VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions
#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
FLDCW—Load Control Word (Continued)

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM EM or TS in CR0 is set.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
FLDENV—Load FPU Environment

**Description**

Loads the complete FPU operating environment from memory into the FPU registers. The source operand specifies the first byte of the operating-environment data in memory. This data is typically written to the specified memory location by a FSTENV or FNSTENV instruction.

The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. See the *IA-32 Intel® Architecture Software Developer’s Manual* for the layout in memory of the loaded environment, depending on the operating mode of the processor (protected or real) and the size of the current address attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used.

The FLDENV instruction should be executed in the same operating mode as the corresponding FSTENV/FNSTENV instruction.

If one or more unmasked exception flags are set in the new FPU status word, a floating-point exception will be generated upon execution of the next floating-point instruction (except for the no-wait floating-point instructions). To avoid generating exceptions when loading a new environment, clear all the exception flags in the FPU status word that is being loaded.

**Operation**

\[
\begin{align*}
\text{FPUC} & \text{ontrollWord} \leftarrow \text{SRC(}\text{FPUC} \text{ontrollWord}) \\
\text{FPU} & \text{StatusWord} \leftarrow \text{SRC(}\text{FPU} \text{StatusWord}) \\
\text{FPUTagWord} & \leftarrow \text{SRC(}\text{FPUTagWord}) \\
\text{FPU} & \text{DataPointer} \leftarrow \text{SRC(}\text{FPU} \text{DataPointer}) \\
\text{FPUI} & \text{InstructionPointer} \leftarrow \text{SRC(}\text{FPUI} \text{InstructionPointer}) \\
\text{FPUL} & \text{astInstructionOpcode} \leftarrow \text{SRC(}\text{FPUL} \text{astInstructionOpcode})
\end{align*}
\]

**FPU Flags Affected**

The C0, C1, C2, C3 flags are loaded.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Floating-point Exceptions**

None; however, if an unmasked exception is loaded in the status word, it is generated upon execution of the next waiting floating-point instruction.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 /4</td>
<td>FLDENV m14/28byte</td>
<td>Load FPU environment from m14byte or m28byte.</td>
</tr>
</tbody>
</table>
FLDENV—Load FPU Environment (Continued)

Protected Mode Exceptions

#GP(0)    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
          If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)    If a memory operand effective address is outside the SS segment limit.
#NM       EM or TS in CR0 is set.
#PF(fault-code)    If a page fault occurs.
#AC(0)    If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS    If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)    If a memory operand effective address is outside the SS segment limit.
#NM       EM or TS in CR0 is set.
#PF(fault-code)    If a page fault occurs.
#AC(0)    If alignment checking is enabled and an unaligned memory reference is made.
**FMUL/FMULP/FIMUL—Multiply**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /1</td>
<td>FMUL m32real</td>
<td>Multiply ST(0) by m32real and store result in ST(0)</td>
</tr>
<tr>
<td>DC /1</td>
<td>FMUL m64real</td>
<td>Multiply ST(0) by m64real and store result in ST(0)</td>
</tr>
<tr>
<td>D8 C8+i</td>
<td>FMUL ST(0), ST(i)</td>
<td>Multiply ST(0) by ST(i) and store result in ST(0)</td>
</tr>
<tr>
<td>DC C8+i</td>
<td>FMUL ST(i), ST(0)</td>
<td>Multiply ST(i) by ST(0) and store result in ST(i)</td>
</tr>
<tr>
<td>DE C8+i</td>
<td>FMULP ST(i), ST(0)</td>
<td>Multiply ST(i) by ST(0), store result in ST(i), and pop the register stack</td>
</tr>
<tr>
<td>DE C9</td>
<td>FMULP</td>
<td>Multiply ST(0) by ST(1), store result in ST(0), and pop the register stack</td>
</tr>
<tr>
<td>DA /1</td>
<td>FIMUL m32int</td>
<td>Multiply m32int by ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>DE /1</td>
<td>FIMUL m16int</td>
<td>Multiply m16int by ST(0) and store result in ST(0)</td>
</tr>
</tbody>
</table>

**Description**

Multiplies the destination and source operands and stores the product in the destination location. The destination operand is always an FPU data register; the source operand can be a register or a memory location. Source operands in memory can be in single-real, double-real, word-integer, or short-integer formats.

The no-operand version of the instruction multiplies the contents of the ST(0) register by the contents of the ST(1) register. The one-operand version multiplies the contents of a memory location (either a real or an integer value) by the contents of the ST(0) register. The two-operand version multiplies the contents of the ST(0) register by the contents of the ST(i) register or vice versa.

The FMULP instructions perform the additional operation of popping the FPU register stack after storing the product. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point multiply instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FMUL rather than FMULP.

The FIMUL instructions convert an integer source operand to extended-real format before performing the multiplication.

The sign of the result is always the exclusive-OR of the source signs, even if one or more of the values being multiplied is 0 or ∞. When the source operand is an integer 0, it is treated as +0.

The following table shows the results obtained when multiplying various classes of numbers, assuming that neither overflow nor underflow occurs.
### FMUL/FMULP/FIMUL—Multiply (Continued)

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
<th>$-\infty$</th>
<th>$-F$</th>
<th>$-0$</th>
<th>$+0$</th>
<th>$+F$</th>
<th>$+\infty$</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$</td>
<td>$+\infty$</td>
<td>$+\infty$</td>
<td>*</td>
<td>*</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>$-F$</td>
<td>$+\infty$</td>
<td>$+F$</td>
<td>$+0$</td>
<td>$-0$</td>
<td>$-F$</td>
<td>$-\infty$</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>$-I$</td>
<td>$+\infty$</td>
<td>$+F$</td>
<td>$+0$</td>
<td>$-0$</td>
<td>$-F$</td>
<td>$-\infty$</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>$-0$</td>
<td>*</td>
<td>$+0$</td>
<td>$+0$</td>
<td>$-0$</td>
<td>$-0$</td>
<td>*</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>$+0$</td>
<td>*</td>
<td>$-0$</td>
<td>$-0$</td>
<td>$+0$</td>
<td>$+0$</td>
<td>*</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>$+I$</td>
<td>$-\infty$</td>
<td>$-F$</td>
<td>$-0$</td>
<td>$+0$</td>
<td>$+F$</td>
<td>$+\infty$</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>$+F$</td>
<td>$-\infty$</td>
<td>$-F$</td>
<td>$-0$</td>
<td>$+0$</td>
<td>$+F$</td>
<td>$+\infty$</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>$+\infty$</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>*</td>
<td>*</td>
<td>$+\infty$</td>
<td>$+\infty$</td>
<td>NaN</td>
<td></td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td></td>
</tr>
</tbody>
</table>

#### Notes:
- F means finite-real number.
- I means Integer.
- * indicates invalid-arithmetic-operand (#IA) exception.

#### Operation

IF instruction is FIMUL

THEN

DEST ← DEST * ConvertExtendedReal(SRC);

ELSE (* source operand is real number *)

DEST ← DEST * SRC;

FI;

IF instruction = FMULP

THEN

PopRegisterStack

FI;

#### FPU Flags Affected

- **C1**: Set to 0 if stack underflow occurred.
  - Indicates rounding direction if the inexact-result exception (#P) fault is generated: 0 = not roundup; 1 = roundup.

- **C0, C2, C3**: Undefined.

#### Floating-point Exceptions

- **#IS**: Stack underflow occurred.
- **#IA**: Operand is an SNaN value or unsupported format.
  - One operand is ±0 and the other is ±∞.
- **#D**: Source operand is a denormal value.
- **#U**: Result is too small for destination format.
- **#O**: Result is too large for destination format.
- **#P**: Value cannot be represented exactly in destination format.
FMUL/FMULP/FIMUL—Multiply (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  EM or TS in CR0 is set.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  EM or TS in CR0 is set.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
FNOP—No Operation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 D0</td>
<td>FNOP</td>
<td>No operation is performed.</td>
</tr>
</tbody>
</table>

**Description**

Performs no FPU operation. This instruction takes up space in the instruction stream but does not affect the FPU or machine context, except the EIP register.

**FPU Flags Affected**

C0, C1, C2, C3 undefined.

**Floating-point Exceptions**

None.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1.

**Protected Mode Exceptions**

#NM  EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM  EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM  EM or TS in CR0 is set.
FPATAN—Partial Arctangent

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F3</td>
<td>FPATAN</td>
<td>Replace ST(1) with ( \arctan(ST(1)/ST(0)) ) and pop the register stack</td>
</tr>
</tbody>
</table>

**Description**

Computes the arctangent of the source operand in register ST(1) divided by the source operand in register ST(0), stores the result in ST(1), and pops the FPU register stack. The result in register ST(0) has the same sign as the source operand ST(1) and a magnitude less than \( +\pi \).

The following table shows the results obtained when computing the arctangent of various classes of numbers, assuming that underflow does not occur.

**Table 1-6. FPATAN Zeros and NaNs**

<table>
<thead>
<tr>
<th>ST(1)</th>
<th>ST(0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>•</td>
<td>•</td>
</tr>
<tr>
<td>–F</td>
<td>–3\pi/4</td>
</tr>
<tr>
<td>–0</td>
<td>–\pi/2</td>
</tr>
<tr>
<td>+0</td>
<td>+\pi</td>
</tr>
<tr>
<td>+F</td>
<td>+3\pi/4</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

There is no restriction on the range of source operands that FPATAN can accept.

**Operation**

\[
ST(1) \leftarrow \arctan(ST(1)/ST(0));
\]

PopRegisterStack;

**FPU Flags Affected**

- **C1**
  - Set to 0 if stack underflow occurred.
  - Indicates rounding direction if the inexact-result exception (#P) is generated: 0 = not roundup; 1 = roundup.

- **C0, C2, C3**
  - Undefined.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults
  - Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
FPATAN—Partial Arctangent (Continued)

Floating-point Exceptions

#IS Stack underflow occurred.
#IA Source operand is an SNaN value or unsupported format.
#D Source operand is a denormal value.
#U Result is too small for destination format.
#P Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#NM EM or TS in CR0 is set.

Real Address Mode Exceptions

#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#NM EM or TS in CR0 is set.

Intel® Architecture Compatibility Information

The source operands for this instruction are restricted for the 80287 math coprocessor to the following range:

\[ 0 \leq |ST(1)| < |ST(0)| < +\infty \]
FPREM—Partial Remainder

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F8</td>
<td>FPREM</td>
<td>Replace ST(0) with the remainder obtained on dividing ST(0) by ST(1)</td>
</tr>
</tbody>
</table>

**Description**

Computes the remainder obtained on dividing the value in the ST(0) register (the dividend) by the value in the ST(1) register (the divisor or modulus), and stores the result in ST(0). The remainder represents the following value:

\[
\text{Remainder} = ST(0) - (N \times ST(1))
\]

Here, N is an integer value that is obtained by truncating the real-number quotient of \([ST(0) / ST(1)]\) toward zero. The sign of the remainder is the same as the sign of the dividend. The magnitude of the remainder is less than that of the modulus, unless a partial remainder was computed (as described below).

This instruction produces an exact result; the precision (inexact) exception does not occur and the rounding control has no effect. The following table shows the results obtained when computing the remainder of various classes of numbers, assuming that underflow does not occur.

**Table 1-7. FPREM Zeros and NaNs**

<table>
<thead>
<tr>
<th>ST(1)</th>
<th>(-\infty)</th>
<th>(-F)</th>
<th>(-0)</th>
<th>(+0)</th>
<th>(+F)</th>
<th>(+\infty)</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>(-\infty)</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>(-F)</td>
<td>ST(0)</td>
<td>(-F) or (-0)</td>
<td>**</td>
<td>**</td>
<td>(-F) or (-0)</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>(-0)</td>
<td>(-0)</td>
<td>(-0)</td>
<td>*</td>
<td>*</td>
<td>(-0)</td>
<td>(-0)</td>
<td>NaN</td>
</tr>
<tr>
<td>(+0)</td>
<td>(+0)</td>
<td>(+0)</td>
<td>*</td>
<td>*</td>
<td>(+0)</td>
<td>(+0)</td>
<td>NaN</td>
</tr>
<tr>
<td>(+F)</td>
<td>ST(0)</td>
<td>(+F) or (+0)</td>
<td>**</td>
<td>**</td>
<td>(+F) or (+0)</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>(+\infty)</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:

F means finite-real number.

* indicates floating-point invalid-arithmetic-operand (#IA) exception.

** indicates floating-point zero-divide (#Z) exception.

When the result is 0, its sign is the same as that of the dividend. When the modulus is \(\infty\), the result is equal to the value in ST(0).

The FPREM instruction does not compute the remainder specified in IEEE Std. 754. The IEEE specified remainder can be computed with the FPREM1 instruction. The FPREM instruction is provided for compatibility with the Intel 8087 and Intel287 math coprocessors.
The FPREM instruction gets its name “partial remainder” because of the way it computes the remainder. This instruction arrives at a remainder through iterative subtraction. It can, however, reduce the exponent of ST(0) by no more than 63 in one execution of the instruction. If the instruction succeeds in producing a remainder that is less than the modulus, the operation is complete and the C2 flag in the FPU status word is cleared. Otherwise, C2 is set, and the result in ST(0) is called the partial remainder. The exponent of the partial remainder will be less than the exponent of the original dividend by at least 32. Software can re-execute the instruction (using the partial remainder in ST(0) as the dividend) until C2 is cleared.

**Note:** While executing such a remainder-computation loop, a higher-priority interrupting routine that needs the FPU can force a context switch in-between the instructions in the loop.

An important use of the FPREM instruction is to reduce the arguments of periodic functions. When reduction is complete, the instruction stores the three least-significant bits of the quotient in the C3, C1, and C0 flags of the FPU status word. This information is important in argument reduction for the tangent function (using a modulus of $\pi/4$), because it locates the original angle in the correct one of eight sectors of the unit circle.

**Operation**

\[
D \leftarrow \text{exponent(ST(0))} - \text{exponent(ST(1))}; \\
\text{IF } D < 64 \\
\quad \text{THEN} \\
\quad Q \leftarrow \text{Integer(TruncateTowardZero(ST(0) / ST(1))}; \\
\quad \text{ST}(0) \leftarrow \text{ST}(0) - (\text{ST}(1) \times Q); \\
\quad C2 \leftarrow 0; \\
\quad C0, C3, C1 \leftarrow \text{LeastSignificantBits}(Q); (* Q2, Q1, Q0 *) \\
\text{ELSE} \\
\quad C2 \leftarrow 1; \\
\quad N \leftarrow \text{an implementation-dependent number between 32 and 63}; \\
\quad QQ \leftarrow \text{Integer(TruncateTowardZero((ST(0) / ST(1)) / } 2^{D-N}); \\
\quad \text{ST}(0) \leftarrow \text{ST}(0) - (\text{ST}(1) \times QQ \times 2^{D-N}); \\
\text{FI;}
\]

**FPU Flags Affected**

- **C0** Set to bit 2 (Q2) of the quotient.
- **C1** Set to 0 if stack underflow occurred; otherwise, set to least significant bit of quotient (Q0).
- **C2** Set to 0 if reduction complete; set to 1 if incomplete.
- **C3** Set to bit 1 (Q1) of the quotient.

**Additional Itanium® System Environment Exceptions**

- **Itanium Reg Faults** Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
FPREM—Partial Remainder (Continued)

Floating-point Exceptions

#IS Stack underflow occurred.

#IA Source operand is an SNaN value, modulus is 0, dividend is $\infty$, or unsupported format.

#D Source operand is a denormal value.

#U Result is too small for destination format.

Protected Mode Exceptions

#NM EM or TS in CR0 is set.

Real Address Mode Exceptions

#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#NM EM or TS in CR0 is set.
FPREM1—Partial Remainder

Description

Computes the IEEE remainder obtained on dividing the value in the ST(0) register (the dividend) by the value in the ST(1) register (the divisor or modulus), and stores the result in ST(0). The remainder represents the following value:

\[
\text{Remainder} = \text{ST}(0) - (N \times \text{ST}(1))
\]

Here, N is an integer value that is obtained by rounding the real-number quotient of \([\text{ST}(0) / \text{ST}(1)]\) toward the nearest integer value. The sign of the remainder is the same as the sign of the dividend. The magnitude of the remainder is less than half the magnitude of the modulus, unless a partial remainder was computed (as described below).

This instruction produces an exact result; the precision (inexact) exception does not occur and the rounding control has no effect. The following table shows the results obtained when computing the remainder of various classes of numbers, assuming that underflow does not occur.

**Table 1-8. FPREM1 Zeros and NaNs**

<table>
<thead>
<tr>
<th>ST(1)</th>
<th>−∞</th>
<th>−F</th>
<th>−0</th>
<th>+0</th>
<th>+F</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0)</td>
<td>−∞</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>ST(0)</td>
<td>−F or −0</td>
<td>**</td>
<td>**</td>
<td>−F or −0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>−0</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>−0</td>
<td>−0</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>ST(0)</td>
<td>+F or +0</td>
<td>**</td>
<td>**</td>
<td>+F or +0</td>
<td>ST(0)</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:
- F means finite-real number.
- * indicates floating-point invalid-arithmetic-operand (#IA) exception.
- ** indicates floating-point zero-divide (#Z) exception.

When the result is 0, its sign is the same as that of the dividend. When the modulus is \(\infty\), the result is equal to the value in ST(0).

The FPREM1 instruction computes the remainder specified in IEEE Std 754. This instruction operates differently from the FPREM instruction in the way that it rounds the quotient of ST(0) divided by ST(1) to an integer (see the “Operation” below).
FPREM1—Partial Remainder (Continued)

Like the FPREM instruction, the FPREM1 computes the remainder through iterative subtraction, but can reduce the exponent of ST(0) by no more than 63 in one execution of the instruction. If the instruction succeeds in producing a remainder that is less than one half the modulus, the operation is complete and the C2 flag in the FPU status word is cleared. Otherwise, C2 is set, and the result in ST(0) is called the partial remainder. The exponent of the partial remainder will be less than the exponent of the original dividend by at least 32. Software can re-execute the instruction (using the partial remainder in ST(0) as the dividend) until C2 is cleared.

Note: While executing such a remainder-computation loop, a higher-priority interrupting routine that needs the FPU can force a context switch in-between the instructions in the loop.

An important use of the FPREM1 instruction is to reduce the arguments of periodic functions. When reduction is complete, the instruction stores the three least-significant bits of the quotient in the C3, C1, and C0 flags of the FPU status word. This information is important in argument reduction for the tangent function (using a modulus of π/4), because it locates the original angle in the correct one of eight sectors of the unit circle.

Operation

\[ D \leftarrow \text{exponent(ST(0))} - \text{exponent(ST(1))}; \]
\[ \text{IF } D < 64 \]
\[ \text{THEN} \]
\[ Q \leftarrow \text{Integer(RoundTowardNearestInteger(ST(0) / ST(1))}; \]
\[ \text{ST(0)} \leftarrow \text{ST(0)} - (\text{ST(1)} \times Q); \]
\[ C2 \leftarrow 0; \]
\[ C0, C3, C1 \leftarrow \text{LeastSignificantBits}(Q); (* Q2, Q1, Q0 *) \]
\[ \text{ELSE} \]
\[ C2 \leftarrow 1; \]
\[ N \leftarrow \text{an implementation-dependent number between 32 and 63}; \]
\[ QQ \leftarrow \text{Integer(TruncateTowardZero((ST(0) / ST(1)) / 2^{(D-N)}));} \]
\[ \text{ST(0)} \leftarrow \text{ST(0)} - (\text{ST(1)} \times QQ \times 2^{(D-N)}); \]
\[ \text{FI}; \]

FPU Flags Affected

C0 Set to bit 2 (Q2) of the quotient.

C1 Set to 0 if stack underflow occurred; otherwise, set to least significant bit of quotient (Q0).

C2 Set to 0 if reduction complete; set to 1 if incomplete.

C3 Set to bit 1 (Q1) of the quotient.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
FPREM1—Partial Remainder (Continued)

Floating-point Exceptions

#IS          Stack underflow occurred.
#IA          Source operand is an SNaN value, modulus (divisor) is 0, dividend is ∞, or unsupported format.
#D           Source operand is a denormal value.
#U           Result is too small for destination format.

Protected Mode Exceptions

#NM          EM or TS in CR0 is set.

Real Address Mode Exceptions

#NM          EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#NM          EM or TS in CR0 is set.
FPTAN—Partial Tangent

Computes the tangent of the source operand in register ST(0), stores the result in ST(0), and pushes a 1.0 onto the FPU register stack. The source operand must be given in radians and must be less than ±2^{63}. The following table shows the unmasked results obtained when computing the partial tangent of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>ST(0) SRC</th>
<th>ST(0) DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>*</td>
</tr>
<tr>
<td>−F</td>
<td>−F to +F</td>
</tr>
<tr>
<td>−0</td>
<td>−0</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
</tr>
<tr>
<td>+F</td>
<td>−F to +F</td>
</tr>
<tr>
<td>+∞</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:
F means finite-real number.
* indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range −2^{63} to +2^{63} can be reduced to the range of the instruction by subtracting an appropriate integer multiple of 2π or by using the FPREM instruction with a divisor of 2π.

The value 1.0 is pushed onto the register stack after the tangent has been computed to maintain compatibility with the Intel 8087 and Intel287 math coprocessors. This operation also simplifies the calculation of other trigonometric functions. For instance, the cotangent (which is the reciprocal of the tangent) can be computed by executing a FDIVR instruction after the FPTAN instruction.

Operation

IF

IF ST(0) < 2^{63}
THEN
    C2 ← 0;
    ST(0) ← tan(ST(0));
    TOP ← TOP − 1;
    ST(0) ← 1.0;
ELSE (*source operand is out-of-range *)
    C2 ← 1;
FI;
FPTAN—Partial Tangent (Continued)

FPU Flags Affected

C1  Set to 0 if stack underflow occurred; set to 1 if stack overflow occurred.  
Indicates rounding direction if the inexact-result exception (#P) is generated:  
0 = not roundup; 1 = roundup.

C2  Set to 1 if source operand is outside the range $-2^{63}$ to $+2^{63}$; otherwise, cleared to 0.

C0, C3  Undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Floating-point Exceptions

#IS  Stack underflow occurred.

#IA  Source operand is an SNaN value, $\infty$, or unsupported format.

#D  Source operand is a denormal value.

#U  Result is too small for destination format.

#P  Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#NM  EM or TS in CR0 is set.

Real Address Mode Exceptions

#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#NM  EM or TS in CR0 is set.
FRNDINT—Round to Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 FC</td>
<td>FRNDINT</td>
<td>Round ST(0) to an integer.</td>
</tr>
</tbody>
</table>

**Description**

Rounds the source value in the ST(0) register to the nearest integral value, depending on the current rounding mode (setting of the RC field of the FPU control word), and stores the result in ST(0).

If the source value is $\infty$, the value is not changed. If the source value is not an integral value, the floating-point inexact-result exception (#P) is generated.

**Operation**

$$\text{ST}(0) \leftarrow \text{RoundToIntegralValue}(\text{ST}(0))$$

**FPU Flags Affected**

- C1 Set to 0 if stack underflow occurred.
- Indicates rounding direction if the inexact-result exception (#P) is generated: 0 = not roundup; 1 = roundup.
- C0, C2, C3 Undefined.

**Floating-point Exceptions**

- #IS Stack underflow occurred.
- #IA Source operand is an SNaN value or unsupported format.
- #D Source operand is a denormal value.
- #P Source operand is not an integral value.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

**Protected Mode Exceptions**

- #NM EM or TS in CR0 is set.

**Real Address Mode Exceptions**

- #NM EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

- #NM EM or TS in CR0 is set.
FRSTOR—Restore FPU State

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DD /4</td>
<td>FRSTOR m94/108byte</td>
<td>Load FPU state from m94byte or m108byte.</td>
</tr>
</tbody>
</table>

**Description**

Loads the FPU state (operating environment and register stack) from the memory area specified with the source operand. This state data is typically written to the specified memory location by a previous FSAVE/FNSAVE instruction.

The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. See the *IA-32 Intel® Architecture Software Developer’s Manual* for the layout in memory of the stored environment, depending on the operating mode of the processor (protected or real) and the size of the current address attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used. The contents of the FPU register stack are stored in the 80 bytes immediately follow the operating environment image.

The FRSTOR instruction should be executed in the same operating mode as the corresponding FSAVE/FNSAVE instruction.

If one or more unmasked exception bits are set in the new FPU status word, a floating-point exception will be generated. To avoid raising exceptions when loading a new operating environment, clear all the exception flags in the FPU status word that is being loaded.

**Operation**

FPUControlWord ← SRC(FPUControlWord);
FPUStatusWord ← SRC(FPUStatusWord);
FPUTagWord ← SRC(FPUTagWord);
FPUDataPointer ← SRC(FPUDataPointer);
FPUInstructionPointer ← SRC(FPUInstructionPointer);
FPULastInstructionOpcode ← SRC(FPULastInstructionOpcode);
ST(0) ← SRC(ST(0));
ST(1) ← SRC(ST(1));
ST(2) ← SRC(ST(2));
ST(3) ← SRC(ST(3));
ST(4) ← SRC(ST(4));
ST(5) ← SRC(ST(5));
ST(6) ← SRC(ST(6));
ST(7) ← SRC(ST(7));

**FPU Flags Affected**

The C0, C1, C2, C3 flags are loaded.

**Floating-point Exceptions**

None; however, this operation might unmask an existing exception that has been detected but not generated, because it was masked. Here, the exception is generated at the completion of the instruction.
FRSTOR—Restore FPU State (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS    If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
**FSAVE/FNSAVE—Store FPU State**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B DD /6</td>
<td>FSAVE m94/108byte</td>
<td>Store FPU state to m94byte or m108byte after checking for pending unmasked floating-point exceptions. Then re-initialize the FPU.</td>
</tr>
<tr>
<td>DD /6</td>
<td>FNSAVE m94/108byte</td>
<td>Store FPU environment to m94byte or m108byte without checking for pending unmasked floating-point exceptions. Then re-initialize the FPU.</td>
</tr>
</tbody>
</table>

**Description**

Stores the current FPU state (operating environment and register stack) at the specified destination in memory, and then re-initializes the FPU. The FSAVE instruction checks for and handles pending unmasked floating-point exceptions before storing the FPU state; the FNSAVE instruction does not.

The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. See the *IA-32 Intel® Architecture Software Developer’s Manual* for the layout in memory of the stored environment, depending on the operating mode of the processor (protected or real) and the size of the current address attribute (16-bit or 32-bit). In virtual-8086 mode, the real mode layouts are used. The contents of the FPU register stack are stored in the 80 bytes immediately follow the operating environment image.

The saved image reflects the state of the FPU after all floating-point instructions preceding the FSAVE/FNSAVE instruction in the instruction stream have been executed.

After the FPU state has been saved, the FPU is reset to the same default values it is set to with the FINIT/FNINIT instructions (see “FINIT/FNINIT—Initialize Floating-point Unit” on page 3:481).

The FSAVE/FNSAVE instructions are typically used when the operating system needs to perform a context switch, an exception handler needs to use the FPU, or an application program needs to pass a “clean” FPU to a procedure.

**Operation**

(* Save FPU State and Registers *)

DEST(FPUControlWord) ← FPUControlWord;
DEST(FPUStatusWord) ← FPUStatusWord;
DEST(FPUTagWord) ← FPUTagWord;
DEST(FPUDataPointer) ← FPUDataPointer;
DEST(FPUInstructionPointer) ← FPUInstructionPointer;
DEST(FPULastInstructionOpcode) ← FPULastInstructionOpcode;
DEST(ST(0)) ← ST(0);
DEST(ST(1)) ← ST(1);
DEST(ST(2)) ← ST(2);
DEST(ST(3)) ← ST(3);
DEST(ST(4)) ← ST(4);
DEST(ST(5)) ← ST(5);
DEST(ST(6)) ← ST(6);
DEST(ST(7)) ← ST(7);
(* Initialize FPU *)
FPUControlWord ← 037FH;
FSAVE/FNSAVE—Store FPU State (Continued)

FPStatusWord ← 0;
FPUTagWord ← FFFFH;
FPUDataPointer ← 0;
FPUIInstructionPointer ← 0;
FPULastInstructionOpcode ← 0;

FPU Flags Affected

The C0, C1, C2, and C3 flags are saved and then cleared.

Floating-point Exceptions

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If destination is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.
FSAVE/FNSAVE—Store FPU State (Continued)

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Intel® Architecture Compatibility Information

For Intel math coprocessors and FPUs prior to the Pentium processor, an FWAIT instruction should be executed before attempting to read from the memory image stored with a prior FSAVE/FNSAVE instruction. This FWAIT instruction helps ensure that the storage operation has been completed.
FScale—Scale

Description

Multiplies the destination operand by 2 to the power of the source operand and stores the result in the destination operand. This instruction provides rapid multiplication or division by integral powers of 2. The destination operand is a real value that is located in register ST(0). The source operand is the nearest integer value that is smaller than the value in the ST(1) register (that is, the value in register ST(1) is truncated toward 0 to its nearest integer value to form the source operand). The actual scaling operation is performed by adding the source operand (integer value) to the exponent of the value in register ST(0). The following table shows the results obtained when scaling various classes of numbers, assuming that neither overflow nor underflow occurs.

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>ST(1)</th>
<th>−N</th>
<th>0</th>
<th>+N</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
</tr>
<tr>
<td>−F</td>
<td>−F</td>
<td>−F</td>
<td>−F</td>
<td>−F</td>
</tr>
<tr>
<td>−0</td>
<td>−0</td>
<td>−0</td>
<td>−0</td>
<td>−0</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>+0</td>
<td>+0</td>
</tr>
<tr>
<td>+F</td>
<td>+F</td>
<td>+F</td>
<td>+F</td>
<td>+F</td>
</tr>
<tr>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:
F means finite-real number.
N means integer.

In most cases, only the exponent is changed and the mantissa (significand) remains unchanged. However, when the value being scaled in ST(0) is a denormal value, the mantissa is also changed and the result may turn out to be a normalized number. Similarly, if overflow or underflow results from a scale operation, the resulting mantissa will differ from the source’s mantissa.

The FSCALE instruction can also be used to reverse the action of the FXTRACT instruction, as shown in the following example:

```
FXTRACT;
FSCALE;
FSTP ST(1);
```

In this example, the FXTRACT instruction extracts the significand and exponent from the value in ST(0) and stores them in ST(0) and ST(1) respectively. The FSCALE then scales the significand in ST(0) by the exponent in ST(1), recreating the original value before the FXTRACT operation was performed. The FSTP ST(1) instruction returns the recreated value to the FPU register where it originally resided.
FScale—Scale (Continued)

Operation
\[ ST(0) \leftarrow ST(0) \times 2^{ST(1)}; \]

FPU Flags Affected

- C1: Set to 0 if stack underflow occurred.
- Indicates rounding direction if the inexact-result exception (#P) is generated:
  - 0 = not roundup; 1 = roundup.
- C0, C2, C3: Undefined.

Floating-point Exceptions

- #IS: Stack underflow occurred.
- #IA: Source operand is an SNaN value or unsupported format.
- #D: Source operand is a denormal value.
- #U: Result is too small for destination format.
- #O: Result is too large for destination format.
- #P: Value cannot be represented exactly in destination format.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Protected Mode Exceptions

- #NM: EM or TS in CR0 is set.

Real Address Mode Exceptions

- #NM: EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

- #NM: EM or TS in CR0 is set.
FSIN—Sine

**Description**

Calculates the sine of the source operand in register ST(0) and stores the result in ST(0). The source operand must be given in radians and must be within the range $-2^{63}$ to $+2^{63}$. The following table shows the results obtained when taking the sine of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>SRC (ST(0))</th>
<th>DEST (ST(0))</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$</td>
<td>*</td>
</tr>
<tr>
<td>$-F$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$-0$</td>
<td>$0$</td>
</tr>
<tr>
<td>$+0$</td>
<td>$0$</td>
</tr>
<tr>
<td>$+F$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$+\infty$</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:

F means finite-real number.

* indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range $-2^{63}$ to $+2^{63}$ can be reduced to the range of the instruction by subtracting an appropriate integer multiple of $2\pi$ or by using the FPREM instruction with a divisor of $2\pi$.

**Operation**

IF I

IF ST(0) < $2^{63}$

THEN

  C2 ← 0;
  ST(0) ← sin(ST(0));
ELSE (* source operand out of range *)

  C2 ← 1;
FI:
FSIN—Sine (Continued)

FPU Flags Affected

C1  Set to 0 if stack underflow occurred.
    Indicates rounding direction if the inexact-result exception (#P) is generated:
    0 = not roundup; 1 = roundup.

C2  Set to 1 if source operand is outside the range $-2^{63}$ to $+2^{63}$; otherwise, cleared to 0.

C0, C3 Undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Floating-point Exceptions

#IS  Stack underflow occurred.

#IA  Source operand is an SNaN value, $\infty$, or unsupported format.

#D   Source operand is a denormal value.

#P   Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#NM  EM or TS in CR0 is set.

Real Address Mode Exceptions

#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#NM  EM or TS in CR0 is set.
**FSINCOS—Sine and Cosine**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 FB</td>
<td>FSINCOS</td>
<td>Compute the sine and cosine of ST(0); replace ST(0) with the sine, and push the cosine onto the register stack.</td>
</tr>
</tbody>
</table>

**Description**

Computes both the sine and the cosine of the source operand in register ST(0), stores the sine in ST(0), and pushes the cosine onto the top of the FPU register stack. (This instruction is faster than executing the FSIN and FCOS instructions in succession.)

The source operand must be given in radians and must be within the range $-2^{63}$ to $+2^{63}$. The following table shows the results obtained when taking the sine and cosine of various classes of numbers, assuming that underflow does not occur.

<table>
<thead>
<tr>
<th>SRC</th>
<th>DEST</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0)</td>
<td>ST(0) Cosine</td>
</tr>
<tr>
<td>$-\infty$</td>
<td>*</td>
</tr>
<tr>
<td>$-F$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$-0$</td>
<td>$+1$</td>
</tr>
<tr>
<td>$+0$</td>
<td>$+1$</td>
</tr>
<tr>
<td>$+F$</td>
<td>$-1$ to $+1$</td>
</tr>
<tr>
<td>$+\infty$</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

**Notes:**
- F means finite-real number.
- * indicates floating-point invalid-arithmetic-operand (#IA) exception.

If the source operand is outside the acceptable range, the C2 flag in the FPU status word is set, and the value in register ST(0) remains unchanged. The instruction does not raise an exception when the source operand is out of range. It is up to the program to check the C2 flag for out-of-range conditions. Source values outside the range $-2^{63}$ to $+2^{63}$ can be reduced to the range of the instruction by subtracting an appropriate integer multiple of $2\pi$ or by using the FPREM instruction with a divisor of $2\pi$.

**Operation**

```plaintext
IF ST(0) < $2^{63}$ THEN
  C2 ← 0;
  TEMP ← cosine(ST(0));
  ST(0) ← sine(ST(0));
  TOP ← TOP − 1;
  ST(0) ← TEMP;
ELSE (* source operand out of range *)
  C2 ← 1;
FI;
```
FSINCOS—Sine and Cosine (Continued)

FPU Flags Affected

C1  Set to 0 if stack underflow occurred; set to 1 of stack overflow occurs.
    Indicates rounding direction if the inexact-result exception (#P) is generated:
    0 = not roundup; 1 = roundup.
C2  Set to 1 if source operand is outside the range \(-2^{63}\) to \(+2^{63}\); otherwise, cleared
    to 0.
C0, C3 Undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Floating-point Exceptions

#IS  Stack underflow occurred.
#IA  Source operand is an SNaN value, \(\infty\), or unsupported format.
#D   Source operand is a denormal value.
#U   Result is too small for destination format.
#P   Value cannot be represented exactly in destination format.

Protected Mode Exceptions

#NM  EM or TS in CR0 is set.

Real Address Mode Exceptions

#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#NM  EM or TS in CR0 is set.
FSQRT—Square Root

Description

Calculates the square root of the source value in the ST(0) register and stores the result in ST(0).

The following table shows the results obtained when taking the square root of various classes of numbers, assuming that neither overflow nor underflow occurs.

<table>
<thead>
<tr>
<th>SRC (ST(0))</th>
<th>DEST (ST(0))</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>*</td>
</tr>
<tr>
<td>−F</td>
<td>*</td>
</tr>
<tr>
<td>−0</td>
<td>−0</td>
</tr>
<tr>
<td>+0</td>
<td>+0</td>
</tr>
<tr>
<td>+F</td>
<td>+F</td>
</tr>
<tr>
<td>+∞</td>
<td>+∞</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:
F means finite-real number.
* indicates floating-point invalid-arithmetic-operand (#IA) exception.

Operation

ST(0) ← SquareRoot(ST(0));

FPU Flags Affected

C1 Set to 0 if stack underflow occurred.
Indicates rounding direction if inexact-result exception (#P) is generated:
0 = not roundup; 1 = roundup.
C0, C2, C3 Undefined.

Floating-point Exceptions

#IS Stack underflow occurred.
#IA Source operand is an SNaN value or unsupported format.
Source operand is a negative value (except for −0).
#D Source operand is a denormal value.
#P Value cannot be represented exactly in destination format.
FSQRT—Square Root (Continued)

Additional Itanium® System Environment Exceptions
Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Protected Mode Exceptions
#NM  EM or TS in CR0 is set.

Real Address Mode Exceptions
#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions
#NM  EM or TS in CR0 is set.
FST/FSTP—Store Real

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 /2</td>
<td>FST m32real</td>
<td>Copy ST(0) to m32real</td>
</tr>
<tr>
<td>DD /2</td>
<td>FST m64real</td>
<td>Copy ST(0) to m64real</td>
</tr>
<tr>
<td>DD D0+i</td>
<td>FST ST(i)</td>
<td>Copy ST(0) to ST(i)</td>
</tr>
<tr>
<td>D9 /3</td>
<td>FSTP m32real</td>
<td>Copy ST(0) to m32real and pop register stack</td>
</tr>
<tr>
<td>DD /3</td>
<td>FSTP m64real</td>
<td>Copy ST(0) to m64real and pop register stack</td>
</tr>
<tr>
<td>DB /7</td>
<td>FSTP m80real</td>
<td>Copy ST(0) to m80real and pop register stack</td>
</tr>
<tr>
<td>DD D8+i</td>
<td>FSTP ST(i)</td>
<td>Copy ST(0) to ST(i) and pop register stack</td>
</tr>
</tbody>
</table>

Description

The FST instruction copies the value in the ST(0) register to the destination operand, which can be a memory location or another register in the FPU registers stack. When storing the value in memory, the value is converted to single- or double-real format.

The FSTP instruction performs the same operation as the FST instruction and then pops the register stack. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The FSTP instruction can also stores values in memory in extended-real format.

If the destination operand is a memory location, the operand specifies the address where the first byte of the destination value is to be stored. If the destination operand is a register, the operand specifies a register in the register stack relative to the top of the stack.

If the destination size is single- or double-real, the significand of the value being stored is rounded to the width of the destination (according to rounding mode specified by the RC field of the FPU control word), and the exponent is converted to the width and bias of the destination format. If the value being stored is too large for the destination format, a numeric overflow exception (#O) is generated and, if the exception is unmasked, no value is stored in the destination operand. If the value being stored is a denormal value, the denormal exception (#D) is not generated. This condition is simply signaled as a numeric underflow exception (#U) condition.

If the value being stored is ±0, ±∞, or a NaN, the least-significant bits of the significand and the exponent are truncated to fit the destination format. This operation preserves the value’s identity as a 0, ∞, or NaN.

If the destination operand is a non-empty register, the invalid-operation exception is not generated.

Operation

```
DEST ← ST(0);
IF instruction = FSTP
  THEN
    PopRegisterStack;
FI;
```
FST/FSTP—Store Real (Continued)

FPU Flags Affected

C1 Set to 0 if stack underflow occurred.
Indicates rounding direction of if the floating-point inexact exception (#P) is generated: 0 = not roundup; 1 = roundup.
C0, C2, C3 Undefined.

Floating-point Exceptions

#IS Stack underflow occurred.
#IA Source operand is an SNaN value or unsupported format.
#U Result is too small for the destination format.
#O Result is too large for the destination format.
#P Value cannot be represented exactly in destination format.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If the destination is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM EM or TS in CR0 is set.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM EM or TS in CR0 is set.
FST/FSTP—Store Real (Continued)

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
FSTCW/FNSTCW—Store Control Word

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B D9 /7</td>
<td>FSTCW m2byte</td>
<td>Store FPU control word to m2byte after checking for pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>D9 /7</td>
<td>FNSTCW m2byte</td>
<td>Store FPU control word to m2byte without checking for pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

Description

Stores the current value of the FPU control word at the specified destination in memory. The FSTCW instruction checks for and handles pending unmasked floating-point exceptions before storing the control word; the FNSTCW instruction does not.

Operation

DEST ← FPUControlWord;

FPU Flags Affected

The C0, C1, C2, and C3 flags are undefined.

Floating-point Exceptions

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If the destination is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NM  EM or TS in CR0 is set.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
FSTCW/FNSTCW—Store Control Word (Continued)

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
FSTENV/FNSTENV—Store FPU Environment

Description

Saves the current FPU operating environment at the memory location specified with the destination operand, and then masks all floating-point exceptions. The FPU operating environment consists of the FPU control word, status word, tag word, instruction pointer, data pointer, and last opcode. See the IA-32 Intel® Architecture Software Developer’s Manual for the layout in memory of the stored environment, depending on the operating mode of the processor (protected or real) and the size of the current address attribute (16-bit or 32-bit). (In virtual-8086 mode, the real mode layouts are used.)

The FSTENV instruction checks for and handles any pending unmasked floating-point exceptions before storing the FPU environment; the FNSTENV instruction does not. The saved image reflects the state of the FPU after all floating-point instructions preceding the FSTENV/FNSTENV instruction in the instruction stream have been executed.

These instructions are often used by exception handlers because they provide access to the FPU instruction and data pointers. The environment is typically saved in the procedure stack. Masking all exceptions after saving the environment prevents floating-point exceptions from interrupting the exception handler.

Operation

\[
\begin{align*}
\text{DEST}(\text{FPUControlWord}) & \leftarrow \text{FPUControlWord}; \\
\text{DEST}(\text{FPUStatusWord}) & \leftarrow \text{FPUStatusWord}; \\
\text{DEST}(\text{FPUTagWord}) & \leftarrow \text{FPUTagWord}; \\
\text{DEST}(\text{FPUDataPointer}) & \leftarrow \text{FPUDataPointer}; \\
\text{DEST}(\text{FPUInstructionPointer}) & \leftarrow \text{FPUInstructionPointer}; \\
\text{DEST}(\text{FPULastInstructionOpcode}) & \leftarrow \text{FPULastInstructionOpcode};
\end{align*}
\]

FPU Flags Affected

The C0, C1, C2, and C3 are undefined.

Floating-point Exceptions

None.
FSTENV/FNSTENV—Store FPU Environment (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If the destination is located in a nonwritable segment.
        If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS    If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM    EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
FSTSW/FNSTSW—Store Status Word

Stores the current value of the FPU status word in the destination location. The destination operand can be either a two-byte memory location or the AX register. The FSTSW instruction checks for and handles pending unmasked floating-point exceptions before storing the status word; the FNSTSW instruction does not.

The FNSTSW AX form of the instruction is used primarily in conditional branching (for instance, after an FPU comparison instruction or an FPREM, FPREM1, or FXAM instruction), where the direction of the branch depends on the state of the FPU condition code flags. This instruction can also be used to invoke exception handlers (by examining the exception flags) in environments that do not use interrupts. When the FNSTSW AX instruction is executed, the AX register is updated before the processor executes any further instructions. The status stored in the AX register is thus guaranteed to be from the completion of the prior FPU instruction.

Operation

\[ \text{DEST} \leftarrow \text{FPUSstatusWord}; \]

FPU Flags Affected

The C0, C1, C2, and C3 are undefined.

Floating-point Exceptions

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults

Disabled FP Register Fault if PSR.dfl is 1.

Itanium Mem Faults

VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
FSTSW/FNSTSW—Store Status Word (Continued)

Protected Mode Exceptions

#GP(0) If the destination is located in a nonwritable segment.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#NM EM or TS in CR0 is set.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
**FSUB/FSUBP/FISUB—Subtract**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /4</td>
<td>FSUB m32real</td>
<td>Subtract m32real from ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>DC /4</td>
<td>FSUB m64real</td>
<td>Subtract m64real from ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>D8 E0+i</td>
<td>FSUB ST(0), ST(i)</td>
<td>Subtract ST(i) from ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>DC E8+i</td>
<td>FSUB ST(i), ST(0)</td>
<td>Subtract ST(0) from ST(i) and store result in ST(i)</td>
</tr>
<tr>
<td>DE E8+i</td>
<td>FSUBP ST(i), ST(0)</td>
<td>Subtract ST(0) from ST(i), store result in ST(i), and pop register stack</td>
</tr>
<tr>
<td>DE E9</td>
<td>FSUBP</td>
<td>Subtract ST(0) from ST(1), store result in ST(1), and pop register stack</td>
</tr>
<tr>
<td>DA /4</td>
<td>FISUB m32int</td>
<td>Subtract m32int from ST(0) and store result in ST(0)</td>
</tr>
<tr>
<td>DE /4</td>
<td>FISUB m16int</td>
<td>Subtract m16int from ST(0) and store result in ST(0)</td>
</tr>
</tbody>
</table>

**Description**

Subtracts the source operand from the destination operand and stores the difference in the destination location. The destination operand is always an FPU data register; the source operand can be a register or a memory location. Source operands in memory can be in single-real, double-real, word-integer, or short-integer formats.

The no-operand version of the instruction subtracts the contents of the ST(0) register from the ST(1) register and stores the result in ST(1). The one-operand version subtracts the contents of a memory location (either a real or an integer value) from the contents of the ST(0) register and stores the result in ST(0). The two-operand version, subtracts the contents of the ST(0) register from the ST(i) register or vice versa.

The FSUBP instructions perform the additional operation of popping the FPU register stack following the subtraction. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point subtract instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FSUB rather than FSUBP.

The FISUB instructions convert an integer source operand to extended-real format before performing the subtraction.

The following table shows the results obtained when subtracting various classes of numbers from one another, assuming that neither overflow nor underflow occurs. Here, the SRC value is subtracted from the DEST value (DEST − SRC = result).

When the difference between two operands of like sign is 0, the result is +0, except for the round toward −∞ mode, in which case the result is −0. This instruction also guarantees that +0 − (−0) = +0, and that −0 − (+0) = −0. When the source operand is an integer 0, it is treated as a +0.

When one operand is ∞, the result is ∞ of the expected sign. If both operands are ∞ of the same sign, an invalid-operation exception is generated.
FSUB/FSUBP/FISUB—Subtract (Continued)

### Table 1-9. FSUB Zeros and NaNs

<table>
<thead>
<tr>
<th>SRC</th>
<th>−∞</th>
<th>−F or −I</th>
<th>−0</th>
<th>+0</th>
<th>+F or +I</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>*</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−F</td>
<td>+∞</td>
<td>±F or ±0</td>
<td>DEST</td>
<td>DEST</td>
<td>−F</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>+∞</td>
<td>−SRC</td>
<td>±0</td>
<td>−0</td>
<td>−SRC</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>+∞</td>
<td>−SRC</td>
<td>+0</td>
<td>±0</td>
<td>−SRC</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+F</td>
<td>+∞</td>
<td>+F</td>
<td>DEST</td>
<td>DEST</td>
<td>±F or ±0</td>
<td>−∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>*</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:
- F means finite-real number.
- I means integer.
- * indicates floating-point invalid-arithmetic-operand (#IA) exception.

**Operation**

**IF instruction is FISUB**

THEN

DEST ← DEST − ConvertExtendedReal(SRC);

ELSE (* source operand is real number *)

DEST ← DEST − SRC;

FI;

**IF instruction = FSUBP**

THEN

PopRegisterStack

FI;

**FPU Flags Affected**

C1 Set to 0 if stack underflow occurred.

Indicates rounding direction if the inexact-result exception (#P) fault is generated: 0 = not roundup; 1 = roundup.

C0, C2, C3 Undefined.

**Floating-point Exceptions**

#IS Stack underflow occurred.

#IA Operand is an SNaN value or unsupported format.

Operands are infinities of like sign.

#D Source operand is a denormal value.

#U Result is too small for destination format.

#O Result is too large for destination format.

#P Value cannot be represented exactly in destination format.
FSUB/FSUBP/FISUB—Subtract (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
          If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM  EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#NM  EM or TS in CR0 is set.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
FSUBR/FSUBRP/FISUBR—Reverse Subtract

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D8 /5</td>
<td>FSUBR m32real</td>
<td>Subtract ST(0) from m32real and store result in ST(0)</td>
</tr>
<tr>
<td>DC /5</td>
<td>FSUBR m64real</td>
<td>Subtract ST(0) from m64real and store result in ST(0)</td>
</tr>
<tr>
<td>D8 E8+i</td>
<td>FSUBR ST(0), ST(i)</td>
<td>Subtract ST(0) from ST(i) and store result in ST(0)</td>
</tr>
<tr>
<td>DC E0+i</td>
<td>FSUBR ST(i), ST(0)</td>
<td>Subtract ST(i) from ST(0) and store result in ST(i)</td>
</tr>
<tr>
<td>DE E0+i</td>
<td>FSUBRP ST(i), ST(0)</td>
<td>Subtract ST(0) from ST(i), store result in ST(i), and pop register stack</td>
</tr>
<tr>
<td>DE E1</td>
<td>FSUBRP</td>
<td>Subtract ST(1) from ST(0), store result in ST(1), and pop register stack</td>
</tr>
<tr>
<td>DA /5</td>
<td>FISUBR m32int</td>
<td>Subtract ST(0) from m32int and store result in ST(0)</td>
</tr>
<tr>
<td>DE /5</td>
<td>FISUBR m16int</td>
<td>Subtract ST(0) from m16int and store result in ST(0)</td>
</tr>
</tbody>
</table>

Description

Subtracts the destination operand from the source operand and stores the difference in the destination location. The destination operand is always an FPU register; the source operand can be a register or a memory location. Source operands in memory can be in single-real, double-real, word-integer, or short-integer formats.

These instructions perform the reverse operations of the FSUB, FSUBP, and FISUB instructions. They are provided to support more efficient coding.

The no-operand version of the instruction subtracts the contents of the ST(1) register from the ST(0) register and stores the result in ST(0). The one-operand version subtracts the contents of the ST(0) register from the contents of a memory location (either a real or an integer value) and stores the result in ST(0). The two-operand version, subtracts the contents of the ST(i) register from the ST(0) register or vice versa.

The FSUBRP instructions perform the additional operation of popping the FPU register stack following the subtraction. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1. The no-operand version of the floating-point reverse subtract instructions always results in the register stack being popped. In some assemblers, the mnemonic for this instruction is FSUBR rather than FSUBRP.

The FISUBR instructions convert an integer source operand to extended-real format before performing the subtraction.

The following table shows the results obtained when subtracting various classes of numbers from one another, assuming that neither overflow nor underflow occurs. Here, the DEST value is subtracted from the SRC value (SRC – DEST = result).
FSUBR/FSUBRP/FISUBR—Reverse Subtract (Continued)

When the difference between two operands of like sign is 0, the result is +0, except for the round toward −∞ mode, in which case the result is −0. This instruction also guarantees that +0 − (−0) = +0, and that −0 − (+0) = −0. When the source operand is an integer 0, it is treated as a +0.

When one operand is ∞, the result is ∞ of the expected sign. If both operands are ∞ of the same sign, an invalid-operation exception is generated.

Table 1-10. FSUBR Zeros and NaNs

<table>
<thead>
<tr>
<th>SRC</th>
<th>−∞</th>
<th>−F</th>
<th>−0</th>
<th>+0</th>
<th>+F</th>
<th>+∞</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>−∞</td>
<td>*</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−F or −I</td>
<td>−∞</td>
<td>±F or ±0</td>
<td>−DEST</td>
<td>−DEST</td>
<td>+F</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>−0</td>
<td>−∞</td>
<td>SRC</td>
<td>±0</td>
<td>+0</td>
<td>SRC</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+0</td>
<td>−∞</td>
<td>SRC</td>
<td>−0</td>
<td>±0</td>
<td>SRC</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+F or +I</td>
<td>−∞</td>
<td>−F</td>
<td>−DEST</td>
<td>−DEST</td>
<td>±F or ±0</td>
<td>+∞</td>
<td>NaN</td>
</tr>
<tr>
<td>+∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>−∞</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:
F means finite-real number.
I means integer.
* indicates floating-point invalid-arithmetic-operand (#IA) exception.

Operation

IF instruction is FISUBR
THEN
   DEST ← ConvertExtendedReal(SRC) − DEST;
ELSE (* source operand is real number *)
   DEST ← SRC − DEST;
FI;

IF instruction = FSUBRP
THEN
   PopRegisterStack
FI;

FPU Flags Affected

C1 Set to 0 if stack underflow occurred.
Indicates rounding direction if the inexact-result exception (#P) fault is generated: 0 = not roundup; 1 = roundup.

C0, C2, C3 Undefined.
FSUBR/FSUBRP/FISUBR—Reverse Subtract (Continued)

Floating-point Exceptions

#IS Stack underflow occurred.
#IA Operand is an SNaN value or unsupported format.
Operands are infinities of like sign.
#D Source operand is a denormal value.
#U Result is too small for destination format.
#O Result is too large for destination format.
#P Value cannot be represented exactly in destination format.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM EM or TS in CR0 is set.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NM EM or TS in CR0 is set.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
FTST—TEST

**Description**

Compares the value in the ST(0) register with 0.0 and sets the condition code flags C0, C2, and C3 in the FPU status word according to the results (see table below).

<table>
<thead>
<tr>
<th>Condition</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST(0) &gt; 0.0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST(0) &lt; 0.0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST(0) = 0.0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Unordered</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

This instruction performs an “unordered comparison.” An unordered comparison also checks the class of the numbers being compared (see “FXAM—Examine” on page 3:541). If the value in register ST(0) is a NaN or is in an undefined format, the condition flags are set to “unordered.”

The sign of zero is ignored, so that –0.0 = +0.0.

**Operation**

```
CASE (relation of operands) OF
    Not comparable: C3, C2, C0 ← 111;
    ST(0) > 0.0: C3, C2, C0 ← 000;
    ST(0) < 0.0: C3, C2, C0 ← 001;
    ST(0) = 0.0: C3, C2, C0 ← 100;
ESAC;
```

**FPU Flags Affected**

- **C1**: Set to 0 if stack underflow occurred; otherwise, cleared to 0.
- **C0, C2, C3**: See above table.

**Floating-point Exceptions**

- **#IS**: Stack underflow occurred.
- **#IA**: One or both operands are NaN values or have unsupported formats.
- **#D**: One or both operands are denormal values.

**Additional Itanium® System Environment Exceptions**

- **Itanium Reg Faults**: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

**Protected Mode Exceptions**

- **#NM**: EM or TS in CR0 is set.
FTST—TEST (Continued)

**Real Address Mode Exceptions**

#NM  EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM  EM or TS in CR0 is set.
FUCOM/FUCOMP/FUCOMPP—Unordered Compare Real

**Description**

Performs an unordered comparison of the contents of register ST(0) and ST(i) and sets condition code flags C0, C2, and C3 in the FPU status word according to the results (see the table below). If no operand is specified, the contents of registers ST(0) and ST(1) are compared. The sign of zero is ignored, so that \(-0.0 = +0.0\).

An unordered comparison checks the class of the numbers being compared (see “FXAM—Examine” on page 3:541). The FUCOM instructions perform the same operation as the FCOM instructions. The only difference is that the FUCOM instruction raises the invalid-arithmetic-operand exception (#IA) only when either or both operands is an SNaN or is in an unsupported format; QNaNs cause the condition code flags to be set to unordered, but do not cause an exception to be generated. The FCOM instruction raises an invalid-operation exception when either or both of the operands is a NaN value of any kind or is in an unsupported format.

As with the FCOM instructions, if the operation results in an invalid-arithmetic-operand exception being raised, the condition code flags are set only if the exception is masked.

The FUCOMP instructions pop the register stack following the comparison operation and the FUCOMPP instructions pops the register stack twice following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

**Operation**

CASE (relation of operands) OF

<table>
<thead>
<tr>
<th>Relation</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST &gt; SRC</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST &lt; SRC</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST = SRC</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Unordered

A. Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.

An unordered comparison checks the class of the numbers being compared (see “FXAM—Examine” on page 3:541). The FUCOM instructions perform the same operation as the FCOM instructions. The only difference is that the FUCOM instruction raises the invalid-arithmetic-operand exception (#IA) only when either or both operands is an SNaN or is in an unsupported format; QNaNs cause the condition code flags to be set to unordered, but do not cause an exception to be generated. The FCOM instruction raises an invalid-operation exception when either or both of the operands is a NaN value of any kind or is in an unsupported format.

As with the FCOM instructions, if the operation results in an invalid-arithmetic-operand exception being raised, the condition code flags are set only if the exception is masked.

The FUCOMP instructions pop the register stack following the comparison operation and the FUCOMPP instructions pops the register stack twice following the comparison operation. To pop the register stack, the processor marks the ST(0) register as empty and increments the stack pointer (TOP) by 1.

** Opcode Instruction Description**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DD E0+i</td>
<td>FUCOM ST(i)</td>
<td>Compare ST(0) with ST(i)</td>
</tr>
<tr>
<td>DD E1</td>
<td>FUCOM</td>
<td>Compare ST(0) with ST(1)</td>
</tr>
<tr>
<td>DD E8+i</td>
<td>FUCOMP ST(i)</td>
<td>Compare ST(0) with ST(i) and pop register stack</td>
</tr>
<tr>
<td>DD E9</td>
<td>FUCOMP</td>
<td>Compare ST(0) with ST(1) and pop register stack</td>
</tr>
<tr>
<td>DA E9</td>
<td>FUCOMPP</td>
<td>Compare ST(0) with ST(1) and pop register stack twice</td>
</tr>
</tbody>
</table>

Comparison Results

<table>
<thead>
<tr>
<th>Comparison Results</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ST0 &gt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>ST0 &lt; ST(i)</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>ST0 = ST(i)</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Unordered

A. Flags not set if unmasked invalid-arithmetic-operand (#IA) exception is generated.
FUCOM/FUCOMP/FUCOMPP—Unordered Compare Real (Continued)

THEN
    C3, C2, C0 ← 111;
ELSE (* ST(0) or SRC is SNaN or unsupported format *)
    #IA;
    IF FPUControlWord.IM = 1
        THEN
            C3, C2, C0 ← 111;
        FI;
    FI;
IF instruction = FUCOMP
    THEN
        PopRegisterStack;
    FI;
IF instruction = FUCOMPP
    THEN
        PopRegisterStack;
        PopRegisterStack;
    FI;

FPU Flags Affected
C1 Set to 0 if stack underflow occurred.
C0, C2, C3 See table on previous page.

Floating-point Exceptions
#IS Stack underflow occurred.
#IA One or both operands are SNaN values or have unsupported formats.
Detection of a QNaN value in and of itself does not raise an invalid-operand exception.
#D One or both operands are denormal values.

Additional Itanium® System Environment Exceptions
Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Protected Mode Exceptions
#NM EM or TS in CR0 is set.

Real Address Mode Exceptions
#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions
#NM EM or TS in CR0 is set.
FWAIT—Wait

See entry for WAIT.
FXAM—Examine

Description

Examines the contents of the ST(0) register and sets the condition code flags C0, C2, and C3 in the FPU status word to indicate the class of value or number in the register (see the table below).

<table>
<thead>
<tr>
<th>Class</th>
<th>C3</th>
<th>C2</th>
<th>C0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unsupported</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>NaN</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Normal finite number</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Infinity</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Zero</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Empty</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Denormal number</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

The C1 flag is set to the sign of the value in ST(0), regardless of whether the register is empty or full.

Operation

\[
C1 \leftarrow \text{sign bit of ST}; \; \text{(* 0 for positive, 1 for negative *)}
\]

\[
\text{CASE (class of value or number in ST(0)) OF}
\]

\[
\text{Unsupported: } C3, C2, C0 \leftarrow 000;
\]

\[
\text{NaN: } C3, C2, C0 \leftarrow 001;
\]

\[
\text{Normal: } C3, C2, C0 \leftarrow 010;
\]

\[
\text{Infinity: } C3, C2, C0 \leftarrow 011;
\]

\[
\text{Zero: } C3, C2, C0 \leftarrow 100;
\]

\[
\text{Empty: } C3, C2, C0 \leftarrow 101;
\]

\[
\text{Denormal: } C3, C2, C0 \leftarrow 110;
\]

ESAC;

FPU Flags Affected

C1 \quad \text{Sign of value in ST(0)}.

C0, C2, C3 \quad \text{See table above}.

Floating-point Exceptions

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults \quad \text{Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.}
FXAM—Examine (Continued)

Protected Mode Exceptions
#NM EM or TS in CR0 is set.

Real Address Mode Exceptions
#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions
#NM EM or TS in CR0 is set.
FXCH—Exchange Register Contents

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 C8+i</td>
<td>FXCH ST(i)</td>
<td>Exchange the contents of ST(0) and ST(i)</td>
</tr>
<tr>
<td>D9 C9</td>
<td>FXCH</td>
<td>Exchange the contents of ST(0) and ST(1)</td>
</tr>
</tbody>
</table>

**Description**

Exchanges the contents of registers ST(0) and ST(i). If no source operand is specified, the contents of ST(0) and ST(1) are exchanged.

This instruction provides a simple means of moving values in the FPU register stack to the top of the stack [ST(0)], so that they can be operated on by those floating-point instructions that can only operate on values in ST(0). For example, the following instruction sequence takes the square root of the third register from the top of the register stack:

```
FXCH ST(3);
FSQRT;
FXCH ST(3);
```

**Operation**

IF number-of-operands is 1
  THEN
    temp ← ST(0);
    ST(0) ← SRC;
    SRC ← temp;
  ELSE
    temp ← ST(0);
    ST(0) ← ST(1);
    ST(1) ← temp;

**FPU Flags Affected**

C1                 Set to 0 if stack underflow occurred; otherwise, cleared to 0.
C0, C2, C3         Undefined.

**Floating-point Exceptions**

#IS                 Stack underflow occurred.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

**Protected Mode Exceptions**

#NM                 EM or TS in CR0 is set.
FXCH—Exchange Register Contents (Continued)

Real Address Mode Exceptions
#NM  EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions
#NM  EM or TS in CR0 is set.
FXTRACT—Extract Exponent and Significand

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F4</td>
<td>FXTRACT</td>
<td>Separate value in ST(0) into exponent and significand, store exponent in ST(0), and push the significand onto the register stack.</td>
</tr>
</tbody>
</table>

**Description**

Separates the source value in the ST(0) register into its exponent and significand, stores the exponent in ST(0), and pushes the significand onto the register stack. Following this operation, the new top-of-stack register ST(0) contains the value of the original significand expressed as a real number. The sign and significand of this value are the same as those found in the source operand, and the exponent is 3FFFH (biased value for a true exponent of zero). The ST(1) register contains the value of the original operand’s true (unbiased) exponent expressed as a real number. (The operation performed by this instruction is a superset of the IEEE-recommended logb(x) function.)

This instruction and the F2XM1 instruction are useful for performing power and range scaling operations. The FXTRACT instruction is also useful for converting numbers in extended-real format to decimal representations (e.g. for printing or displaying).

If the floating-point zero-divide exception (#Z) is masked and the source operand is zero, an exponent value of $-\infty$ is stored in register ST(1) and 0 with the sign of the source operand is stored in register ST(0).

**Operation**

\[
\text{TEMP} \leftarrow \text{Significand(ST(0))}; \\
\text{ST(0)} \leftarrow \text{Exponent(ST(0))}; \\
\text{TOP} \leftarrow \text{TOP} - 1; \\
\text{ST(0)} \leftarrow \text{TEMP};
\]

**FPU Flags Affected**

- C1: Set to 0 if stack underflow occurred; set to 1 if stack overflow occurred.
- C0, C2, C3: Undefined.

**Floating-point Exceptions**

- #IS: Stack underflow occurred.
- #OA: Stack overflow occurred.
- #IA: Source operand is an SNaN value or unsupported format.
- #Z: ST(0) operand is ±0.
- #D: Source operand is a denormal value.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
FXTRACT—Extract Exponent and Significand (Continued)

Protected Mode Exceptions

#NM EM or TS in CR0 is set.

Real Address Mode Exceptions

#NM EM or TS in CR0 is set.

Virtual 8086 Mode Exceptions

#NM EM or TS in CR0 is set.
FYL2X—Compute $y \times \log_2 x$

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F1</td>
<td>FYL2X</td>
<td>Replace ST(1) with ($ST(1) \times \log_2 ST(0)$) and pop the register stack</td>
</tr>
</tbody>
</table>

**Description**

Calculates ($ST(1) \times \log_2 (ST(0))$), stores the result in register ST(1), and pops the FPU register stack. The source operand in ST(0) must be a non-zero positive number.

The following table shows the results obtained when taking the log of various classes of numbers, assuming that neither overflow nor underflow occurs.

**Table 1-11. FYL2X Zeros and NaNs**

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>$-\infty$</th>
<th>$-F$</th>
<th>$+0$</th>
<th>$+0$</th>
<th>$+F$</th>
<th>$+\infty$</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$</td>
<td>*</td>
<td>*</td>
<td>$+\infty$</td>
<td>$+\infty$</td>
<td>$+\infty$</td>
<td>$-\infty$</td>
<td>NaN</td>
</tr>
<tr>
<td>$-F$</td>
<td>*</td>
<td>*</td>
<td>**</td>
<td>**</td>
<td>**</td>
<td>$\pm F$</td>
<td>$-\infty$</td>
</tr>
<tr>
<td>$-0$</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>$+0$</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>$+0$</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>*</td>
<td>$+0$</td>
<td>*</td>
<td>NaN</td>
</tr>
<tr>
<td>$+F$</td>
<td>*</td>
<td>*</td>
<td>**</td>
<td>**</td>
<td>**</td>
<td>$\pm F$</td>
<td>$+\infty$</td>
</tr>
<tr>
<td>$+\infty$</td>
<td>*</td>
<td>*</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>$-\infty$</td>
<td>$+\infty$</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:

* F means finite-real number.
* * indicates floating-point invalid-operation (#IA) exception.
** * indicates floating-point zero-divide (#Z) exception.

If the divide-by-zero exception is masked and register ST(0) contains ±0, the instruction returns $\infty$ with a sign that is the opposite of the sign of the source operand in register ST(1).

The FYL2X instruction is designed with a built-in multiplication to optimize the calculation of logarithms with an arbitrary positive base (b):

\[
\log_b x = (\log_2 b)^{-1} \times \log_2 x
\]

**Operation**

**IF**

ST(1) ← ST(1) × log₂ST(0);
PopRegisterStack;

**FPU Flags Affected**

<table>
<thead>
<tr>
<th>Flag</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>Set to 0 if stack underflow occurred. Indicates rounding direction if the inexact-result exception (#P) is generated: 0 = not roundup; 1 = roundup.</td>
</tr>
<tr>
<td>C0, C2, C3</td>
<td>Undefined.</td>
</tr>
</tbody>
</table>
FYL2X—Compute $y \times \log_2 x$ (Continued)

**Additional Itanium® System Environment Exceptions**
Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

**Floating-point Exceptions**

#IS  Stack underflow occurred.
#IA  Either operand is an SNaN or unsupported format.
     Source operand in register ST(0) is a negative finite value (not −0).
#Z   Source operand in register ST(0) is ±0.
#D   Source operand is a denormal value.
#U   Result is too small for destination format.
#O   Result is too large for destination format.
#P   Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#NM  EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM  EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM  EM or TS in CR0 is set.
**FYL2XP1—Compute y * log₂(x + 1)**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D9 F9</td>
<td>FYL2XP1</td>
<td>Replace ST(1) with ST(1) * log₂(ST(0) + 1.0) and pop the register stack</td>
</tr>
</tbody>
</table>

**Description**

Calculates the log epsilon (ST(1) * log₂(ST(0) + 1.0)), stores the result in register ST(1), and pops the FPU register stack. The source operand in ST(0) must be in the range:

$-(1 - \sqrt{2}/2) \text{ to } (1 - \sqrt{2}/2)$

The source operand in ST(1) can range from $-\infty$ to $+\infty$. If either of the source operands is outside its acceptable range, the result is undefined and no exception is generated.

The following table shows the results obtained when taking the log epsilon of various classes of numbers, assuming that underflow does not occur:

**Table 1-12. FYL2XP1 Zeros and NaNs**

<table>
<thead>
<tr>
<th>ST(0)</th>
<th>$-\infty$</th>
<th>$-(1 - (\sqrt{2}/2))$ to $-0$</th>
<th>$-0$</th>
<th>$+0$ to $+(1 - (\sqrt{2}/2))$</th>
<th>$+\infty$</th>
<th>NaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>$-\infty$</td>
<td>*</td>
<td>$-\infty$</td>
<td>*</td>
<td>*</td>
<td>$-\infty$</td>
<td>NaN</td>
</tr>
<tr>
<td>$-F$</td>
<td>*</td>
<td>+F</td>
<td>+0</td>
<td>$-0$</td>
<td>$-F$</td>
<td>$-\infty$</td>
</tr>
<tr>
<td>$-0$</td>
<td>*</td>
<td>+0</td>
<td>+0</td>
<td>$-0$</td>
<td>$-0$</td>
<td>*</td>
</tr>
<tr>
<td>$+0$</td>
<td>*</td>
<td>$-0$</td>
<td>$-0$</td>
<td>+0</td>
<td>+0</td>
<td>*</td>
</tr>
<tr>
<td>$+F$</td>
<td>*</td>
<td>$-F$</td>
<td>$-0$</td>
<td>+0</td>
<td>$+F$</td>
<td>$+\infty$</td>
</tr>
<tr>
<td>$+\infty$</td>
<td>*</td>
<td>$-\infty$</td>
<td>*</td>
<td>$+\infty$</td>
<td>$-\infty$</td>
<td>NaN</td>
</tr>
<tr>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
<td>NaN</td>
</tr>
</tbody>
</table>

Notes:

- F means finite-real number.
- * indicates floating-point invalid-operation (#IA) exception.

This instruction provides optimal accuracy for values of epsilon [the value in register ST(0)] that are close to 0. When the epsilon value ($\epsilon$) is small, more significant digits can be retained by using the FYL2XP1 instruction than by using ($\epsilon+1$) as an argument to the FYL2X instruction. The ($\epsilon+1$) expression is commonly found in compound interest and annuity calculations. The result can be simply converted into a value in another logarithm base by including a scale factor in the ST(1) source operand. The following equation is used to calculate the scale factor for a particular logarithm base, where $n$ is the logarithm base desired for the result of the FYL2XP1 instruction:

$$\text{scale factor} = \log_n 2$$

**Operation**

I

ST(1) ← ST(1) * log₂(ST(0) + 1.0);
PopRegisterStack;
FYL2XP1—Compute $y \times \log_2(x + 1)$ (Continued)

**FPU Flags Affected**

C1 Set to 0 if stack underflow occurred.

Indicates rounding direction if the inexact-result exception (#P) is generated:

0 = not roundup; 1 = roundup.

C0, C2, C3 Undefined.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

**Floating-point Exceptions**

#IS  Stack underflow occurred.

#IA  Either operand is an SNaN value or unsupported format.

#D  Source operand is a denormal value.

#U  Result is too small for destination format.

#O  Result is too large for destination format.

#P  Value cannot be represented exactly in destination format.

**Protected Mode Exceptions**

#NM  EM or TS in CR0 is set.

**Real Address Mode Exceptions**

#NM  EM or TS in CR0 is set.

**Virtual 8086 Mode Exceptions**

#NM  EM or TS in CR0 is set.
HLT—Halt

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F4</td>
<td>HLT</td>
<td>Halt</td>
</tr>
</tbody>
</table>

**Description**

Stops instruction execution and places the processor in a HALT state. An enabled interrupt, NMI, or a reset will resume execution. If an interrupt (including NMI) is used to resume execution after a HLT instruction, the saved instruction pointer (CS:EIP) points to the instruction following the HLT instruction.

The HLT instruction is a privileged instruction. When the processor is running in protected or virtual 8086 mode, the privilege level of a program or procedure must to 0 to execute the HLT instruction.

**Operation**

IF Itanium System Environment THEN IA-32_Intercept(INST,HALT);
Enter Halt state;

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

IA-32_Intercept Mandatory Instruction Intercept.

**Protected Mode Exceptions**

#GP(0) If the current privilege level is not 0.

**Real Address Mode Exceptions**

None.

**Virtual 8086 Mode Exceptions**

#GP(0) If the current privilege level is not 0.
IDIV—Signed Divide

**Description**
Divides (signed) the value in the AL, AX, or EAX register by the source operand and stores the result in the AX, DX:AX, or EDX:EAX registers. The source operand can be a general-purpose register or a memory location. The action of this instruction depends on the operand size, as shown in the following table:

**Table 1-13. IDIV Operands**

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Dividend</th>
<th>Divisor</th>
<th>Quotient</th>
<th>Remainder</th>
<th>Quotient Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Word/byte</td>
<td>AX</td>
<td>r/m8</td>
<td>AL</td>
<td>AH</td>
<td>−128 to +127</td>
</tr>
<tr>
<td>Doubleword/word</td>
<td>DX:AX</td>
<td>r/m16</td>
<td>AX</td>
<td>DX</td>
<td>−32,768 to +32,767</td>
</tr>
<tr>
<td>Quadword/doubleword</td>
<td>EDX:EAX</td>
<td>r/m32</td>
<td>EAX</td>
<td>EDX</td>
<td>−2^{31} to 2^{32} − 1</td>
</tr>
</tbody>
</table>

Non-integral results are truncated (chopped) towards 0. The sign of the remainder is always the same as the sign of the dividend. The absolute value of the remainder is always less than the absolute value of the divisor. Overflow is indicated with the #DE (divide error) exception rather than with the OF flag.

**Operation**

```plaintext
IF SRC = 0
THEN #DE; (* divide error *)
FI;
IF OpernadSize = 8 (* word/byte operation *)
THEN
    temp ← AX / SRC; (* signed division *)
    IF (temp > 7FH) OR (temp < 80H)
        (* if a positive result is greater than 7FH or a negative result is less than 80H *)
        THEN #DE; (* divide error *)
        ELSE
            AL ← temp;
            AH ← AX SignedModulus SRC;
        FI;
    ELSE
        IF OpernadSize = 16 (* doubleword/word operation *)
            THEN
```
IDIV—Signed Divide (Continued)

\[
\text{temp} \leftarrow \text{DX:AX} / \text{SRC}; (* \text{signed division} *)
\]
\[
\text{IF (temp} > 7\text{FFFH)} \text{OR (temp} < 8\text{000H)} (* \text{if a positive result is greater than 7FFFH *)}
\]
\[
\text{(* or a negative result is less than 8000H *)}
\]
\[
\text{THEN #DE; (* divide error *) ;}
\]
\[
\text{ELSE}
\]
\[
\text{AX} \leftarrow \text{temp};
\]
\[
\text{DX} \leftarrow \text{DX:AX SignedModulus SRC};
\]
\[
\text{FI};
\]
\[
\text{ELSE (* quadword/doubleword operation *)}
\]
\[
\text{temp} \leftarrow \text{EDX:EAX} / \text{SRC}; (* \text{signed division} *)
\]
\[
\text{IF (temp} > 7\text{FFFFFFFH)} \text{OR (temp} < 8\text{00000000H)} (* \text{if a positive result is greater than 7FFFFFFFH *)}
\]
\[
\text{(* or a negative result is less than 80000000H *)}
\]
\[
\text{THEN #DE; (* divide error *) ;}
\]
\[
\text{ELSE}
\]
\[
\text{EAX} \leftarrow \text{temp};
\]
\[
\text{EDX} \leftarrow \text{EDXE:AX SignedModulus SRC};
\]
\[
\text{FI};
\]
\[
\text{FI};
\]

Flags Affected

The CF, OF, SF, ZF, AF, and PF flags are undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults NaT Register Consumption Abort.

Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#DE If the source operand (divisor) is 0. The signed result (quotient) is too large for the destination.

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit. If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
IDIV—Signed Divide (Continued)

Real Address Mode Exceptions

#DE If the source operand (divisor) is 0.

The signed result (quotient) is too large for the destination.

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#DE If the source operand (divisor) is 0.

The signed result (quotient) is too large for the destination.

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
IMUL—Signed Multiply

**Description**

Performs a signed multiplication of two operands. This instruction has three forms, depending on the number of operands.

- **One-operand form.** This form is identical to that used by the MUL instruction. Here, the source operand (in a general-purpose register or memory location) is multiplied by the value in the AL, AX, or EAX register (depending on the operand size) and the product is stored in the AX, DX:AX, or EDX:EAX registers, respectively.

- **Two-operand form.** With this form the destination operand (the first operand) is multiplied by the source operand (second operand). The destination operand is a general-purpose register and the source operand is an immediate value, a general-purpose register, or a memory location. The product is then stored in the destination operand location.

- **Three-operand form.** This form requires a destination operand (the first operand) and two source operands (the second and the third operands). Here, the first source operand (which can be a general-purpose register or a memory location) is multiplied by the second source operand (an immediate value). The product is then stored in the destination operand (a general-purpose register).

When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The CF and OF flags are set when significant bits are carried into the upper half of the result. The CF and OF flags are cleared when the result fits exactly in the lower half of the result.

---

**opcode instruction description**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /5</td>
<td>IMUL r/m8</td>
<td>AX ← AL * r/m byte</td>
</tr>
<tr>
<td>F7 /5</td>
<td>IMUL r/m16</td>
<td>DX:AX ← AX * r/m word</td>
</tr>
<tr>
<td>F7 /5</td>
<td>IMUL r/m32</td>
<td>EDX:EAX ← EAX * r/m doubleword</td>
</tr>
<tr>
<td>0F AF /r</td>
<td>IMUL r16,r/m16</td>
<td>word register ← word register * r/m word</td>
</tr>
<tr>
<td>0F AF /r</td>
<td>IMUL r32,r/m32</td>
<td>doubleword register ← doubleword register * r/m doubleword</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r16,r16,imm8</td>
<td>word register ← r16 * sign-extended immediate byte</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r32,r32,imm8</td>
<td>doubleword register ← r32 * sign-extended immediate byte</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r16,imm8</td>
<td>word register ← word register * sign-extended immediate byte</td>
</tr>
<tr>
<td>6B /r ib</td>
<td>IMUL r32,imm8</td>
<td>doubleword register ← doubleword register * sign-extended immediate byte</td>
</tr>
<tr>
<td>69 /r iw</td>
<td>IMUL r16,ri16,m16,imm16</td>
<td>word register ← r16 * immediate word</td>
</tr>
<tr>
<td>69 /r id</td>
<td>IMUL r32,ri32,m32,imm32</td>
<td>doubleword register ← r32 * immediate doubleword</td>
</tr>
<tr>
<td>69 /r iw</td>
<td>IMUL r16,imm16</td>
<td>word register ← r16 * immediate word</td>
</tr>
<tr>
<td>69 /r id</td>
<td>IMUL r32,imm32</td>
<td>doubleword register ← r32 * immediate doubleword</td>
</tr>
</tbody>
</table>
IMUL—Signed Multiply (Continued)

The three forms of the IMUL instruction are similar in that the length of the product is calculated to twice the length of the operands. With the one-operand form, the product is stored exactly in the destination. With the two- and three-operand forms, however, result is truncated to the length of the destination before it is stored in the destination register. Because of this truncation, the CF or OF flag should be tested to ensure that no significant bits are lost.

The two- and three-operand forms may also be used with unsigned operands because the lower half of the product is the same regardless if the operands are signed or unsigned. The CF and OF flags, however, cannot be used to determine if the upper half of the result is non-zero.

Operation

IF (NumberOfOperands = 1)
    THEN IF (OperandSize = 8)
        THEN
            AX ← AL * SRC (* signed multiplication *)
            IF ((AH = 00H) OR (AH = FFH))
                THEN CF = 0; OF = 0;
                ELSE CF = 1; OF = 1;
            FI;
        ELSE IF OperandSize = 16
            THEN
                DX:AX ← AX * SRC (* signed multiplication *)
                IF ((DX = 0000H) OR (DX = FFFFH))
                    THEN CF = 0; OF = 0;
                    ELSE CF = 1; OF = 1;
                FI;
            ELSE (* OperandSize = 32 *)
                EDX:EAX ← EAX * SRC (* signed multiplication *)
                IF ((EDX = 00000000H) OR (EDX = FFFFFFFFH))
                    THEN CF = 0; OF = 0;
                    ELSE CF = 1; OF = 1;
                FI;
            FI;
    ELSE IF (NumberOfOperands = 2)
        THEN
            temp ← DEST * SRC (* signed multiplication; temp is double DEST size*)
            DEST ← DEST * SRC (* signed multiplication *)
            IF temp ≠ DEST
                THEN CF = 1; OF = 1;
                ELSE CF = 0; OF = 0;
            FI;
        ELSE (* NumberOfOperands = 3 *)
            DEST ← SRC1 * SRC2 (* signed multiplication *)
            temp ← SRC1 * SRC2 (* signed multiplication; temp is double SRC1 size *)
            IF temp ≠ DEST
                THEN CF = 1; OF = 1;
                ELSE CF = 0; OF = 0;
            FI;
        FI;
    FI;
FI;
IMUL—Signed Multiply (Continued)

Flags Affected

For the one operand form of the instruction, the CF and OF flags are set when significant bits are carried into the upper half of the result and cleared when the result fits exactly in the lower half of the result. For the two- and three-operand forms of the instruction, the CF and OF flags are set when the result must be truncated to fit in the destination operand size and cleared when the result fits exactly in the destination operand size. The SF, ZF, AF, and PF flags are undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
         If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
IN—Input from Port

### Description

Copies the value from the I/O port specified with the second operand (source operand) to the destination operand (first operand). The source operand can be a byte-immediate or the DX register; the destination operand can be register AL, AX, or EAX, depending on the size of the port being accessed (8, 16, or 32 bits, respectively). Using the DX register as a source operand allows I/O port addresses from 0 to 65,535 to be accessed; using a byte immediate allows I/O port addresses 0 to 255 to be accessed.

When accessing an 8-bit I/O port, the opcode determines the port size; when accessing a 16- and 32-bit I/O port, the operand-size attribute determines the port size.

At the machine code level, I/O instructions are shorter when accessing 8-bit I/O ports. Here, the upper eight bits of the port address will be 0.

This instruction is only useful for accessing I/O ports located in the processor’s I/O address space.

I/O transactions are performed after all prior data memory operations. No subsequent data memory operations can pass an I/O transaction.

In the Itanium System Environment, I/O port references are mapped into the 64-bit virtual address pointed to by the IOBase register, with four ports per 4K-byte virtual page. Operating systems can utilize the TLB in the Itanium architecture to grant or deny permission to any four I/O ports. The I/O port space can be mapped into any arbitrary 64-bit physical memory location by operating system code. If CFLG.io is 1 and CPL>IOPL, the TSS is consulted for I/O permission. If CFLG.io is 0 or CPL≤IOPL, permission is granted regardless of the state of the TSS I/O permission bitmap (the bitmap is not referenced).

If the referenced I/O port is mapped to an unimplemented virtual address (via the I/O Base register) or if data translations are disabled (PSR.dt is 0) a GPFault is generated on the referencing IN instruction.

### Operation

\[
\text{IF } ((\text{PE} = 1) \text{ AND } ((\text{VM} = 1) \text{ OR } (\text{CPL} > \text{IOPL})))
\]
\[
\text{THEN } (* \text{ Protected mode or virtual-8086 mode with CPL > IOPL } *)
\]
\[
\text{IF } (\text{CFLG.io AND Any I/O Permission Bit for I/O port being accessed = 1})
\]
\[
\text{THEN } \#GP(0);
\]
\[
\text{FI};
\]
\[
\text{ELSE } (* \text{ Real-address mode or protected mode with CPL ≤ IOPL } *)
\]
\[
(* \text{ or virtual-8086 mode with all I/O permission bits for I/O port cleared } *)
\]

### Opcode Instruction Description

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E4 ib</td>
<td>IN AL,imm8</td>
<td>Input byte from imm8 I/O port address into AL</td>
</tr>
<tr>
<td>E5 ib</td>
<td>IN AX,imm8</td>
<td>Input byte from imm8 I/O port address into AX</td>
</tr>
<tr>
<td>E5 ib</td>
<td>IN EAX,imm8</td>
<td>Input byte from imm8 I/O port address into EAX</td>
</tr>
<tr>
<td>EC</td>
<td>IN AL,DX</td>
<td>Input byte from I/O port in DX into AL</td>
</tr>
<tr>
<td>ED</td>
<td>IN AX,DX</td>
<td>Input word from I/O port in DX into AX</td>
</tr>
<tr>
<td>ED</td>
<td>IN EAX,DX</td>
<td>Input doubleword from I/O port in DX into EAX</td>
</tr>
</tbody>
</table>
IN—Input from Port (Continued)

FI;
IF (Itanium_System_Environment THEN
   SRC_VA = IOBase | (Port{15:2}<<12) | Port{11:0};
   SRC_PA = translate(SRC_VA);
   DEST ← [SRC_PA]; (* Reads from I/O port *)
FI;

memory_fence();
DEST <-SRC;
memory-fence();

Flags Affected
None.

Additional Itanium® System Environment Exceptions
Itanium Reg Faults NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
IA-32_Exception Debug traps for data breakpoints and single step
IA-32_Exception Alignment faults
#GP(0) Referenced Port is to an unimplemented virtual address or PSR.dt is zero.

Protected Mode Exceptions
#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1 when CFLG.io is 1.

Real Address Mode Exceptions
None.

Virtual 8086 Mode Exceptions
#GP(0) If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.
INC—Increment by 1

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FE /0</td>
<td>INC r/m8</td>
<td>Increment r/m byte by 1</td>
</tr>
<tr>
<td>FF /0</td>
<td>INC r/m16</td>
<td>Increment r/m word by 1</td>
</tr>
<tr>
<td>FF /0</td>
<td>INC r/m32</td>
<td>Increment r/m doubleword by 1</td>
</tr>
<tr>
<td>40+ rw</td>
<td>INC r16</td>
<td>Increment word register by 1</td>
</tr>
<tr>
<td>40+ rd</td>
<td>INC r32</td>
<td>Increment doubleword register by 1</td>
</tr>
</tbody>
</table>

Description

Adds 1 to the operand, while preserving the state of the CF flag. The source operand can be a register or a memory location. This instruction allows a loop counter to be updated without disturbing the CF flag. (Use a ADD instruction with an immediate operand of 1 to perform a increment operation that does updates the CF flag.)

Operation

DEST ← DEST – 1;

Flags Affected

The CF flag is not affected. The OF, SF, ZF, AF, and PF flags are set according to the result.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If the operand is located in a nonwritable segment.
        If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
        If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
INC—Increment by 1 (Continued)

Virtual 8086 Mode Exceptions

- #GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0)  If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code)  If a page fault occurs.
- #AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
INS/INSB/INSW/INSD—Input from Port to String

Description

Copies the data from the I/O port specified with the second operand (source operand) to the destination operand (first operand). The source operand must be the DX register, allowing I/O port addresses from 0 to 65,535 to be accessed. When accessing an 8-bit I/O port, the opcode determines the port size; when accessing a 16- and 32-bit I/O port, the operand-size attribute determines the port size.

The destination operand is a memory location at the address ES:EDI. (When the operand-size attribute is 16, the DI register is used as the destination-index register.) The ES segment cannot be overridden with a segment override prefix.

The INSB, INSW, and INSD mnemonics are synonyms of the byte, word, and doubleword versions of the INS instructions. (For the INS instruction, “ES:EDI” must be explicitly specified in the instruction.)

After the byte, word, or doubleword is transfer from the I/O port to the memory location, the EDI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the EDI register is incremented; if the DF flag is 1, the EDI register is decremented.) The EDI register is incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The INS, INSB, INSW, and INSD instructions can be preceded by the REP prefix for block input of ECX bytes, words, or doublewords.

This instruction is only useful for accessing I/O ports located in the processor’s I/O address space.

I/O transactions are performed after all prior data memory operations. No subsequent data memory operations can pass an I/O transaction.

In the Itanium System Environment, I/O port references are mapped into the 64-bit virtual address pointed to by the IOBase register, with four ports per 4K-byte virtual page. Operating systems can utilize the TLBs in the Itanium architecture to grant or deny permission to any four I/O ports. The I/O port space can be mapped into any arbitrary 64-bit physical memory location by operating system code. If CFLG.io is 1 and CPL>IOPL, the TSS is consulted for I/O permission. If CFLG.io is 0 or CPL<=IOPL, permission is granted regardless of the state of the TSS I/O permission bitmap (the bitmap is not referenced).

If the referenced I/O port is mapped to an unimplemented virtual address (via the IOBase register) or if data translations are disabled (PSR.dt is 0) a GPFault is generated on the referencing INS instruction.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6C</td>
<td>INS ES:(E)DI, DX</td>
<td>Input byte from port DX into ES:(E)DI</td>
</tr>
<tr>
<td>6D</td>
<td>INS ES:DI, DX</td>
<td>Input word from port DX into ES:DI</td>
</tr>
<tr>
<td>6D</td>
<td>INS ES:EDI, DX</td>
<td>Input doubleword from port DX into ES:EDI</td>
</tr>
<tr>
<td>6C</td>
<td>INSB</td>
<td>Input byte from port DX into ES:(E)DI</td>
</tr>
<tr>
<td>6D</td>
<td>INSW</td>
<td>Input word from port DX into ES:DI</td>
</tr>
<tr>
<td>6D</td>
<td>INSD</td>
<td>Input doubleword from port DX into ES:EDI</td>
</tr>
</tbody>
</table>

Volume 3: Base IA-32 Instruction Reference
INS/INSB/INSW/INSD—Input from Port to String (Continued)

Operation

\[
\text{IF } ((\text{PE} = 1) \text{ AND } ((\text{VM} = 1) \text{ OR } (\text{CPL} > \text{IOPL}))) \\
\text{THEN } (* \text{ Protected mode or virtual-8086 mode with CPL > IOPL } *) \\
\text{IF } (\text{CFLG.io AND Any I/O Permission Bit for I/O port being accessed } = 1) \\
\text{THEN } \#\text{GP}(0); \\
\text{ELSE } (* \text{ I/O operation is allowed } *) \\
\FI;
\]

\[
\text{IF } (\text{Itanium System Environment}) \text{ THEN} \\
\text{SRC VA } = \text{IOBase } | (\text{Port}(15:2)<<12) | \text{Port}(11:0); \\
\text{SRC PA } = \text{translate}(\text{SRC VA}); \\
\text{DEST } \leftarrow [\text{SRC PA}]; (* \text{ Reads from I/O port } *) \\
\FI;
\]

\[
\text{memory_fence();} \\
\text{DEST } \leftarrow \text{SRC}; \\
\text{memory_fence();} \\
\text{IF } (\text{byte transfer}) \\
\text{THEN IF DF } = 0 \\
\text{THEN } (\text{E})\text{DI } \leftarrow 1; \\
\text{ELSE } (\text{E})\text{DI } \leftarrow -1; \\
\FI; \\
\text{ELSE IF } (\text{word transfer}) \\
\text{THEN IF DF } = 0 \\
\text{THEN DI } \leftarrow 2; \\
\text{ELSE DI } \leftarrow -2; \\
\FI; \\
\text{ELSE } (* \text{ doubleword transfer } *) \\
\text{THEN IF DF } = 0 \\
\text{THEN EDI } \leftarrow 4; \\
\text{ELSE EDI } \leftarrow -4; \\
\FI; \\
\FI;
\]

Flags Affected

None.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
- IA-32_Exception: Debug traps for data breakpoints and single step
- IA-32_Exception: Alignment faults
- #GP(0): Referenced Port is to an unimplemented virtual address or PSR.dt is zero.
INS/INSB/INSW/INSD—Input from Port to String (Continued)

Protected Mode Exceptions

#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1 and when CFLG.io is 1.

If the destination is located in a nonwritable segment.

If an illegal memory operand effective address in the ES segments is given.

#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.

#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
INT\textsubscript{n}/INTO/INT3—Call to Interrupt Procedure

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC</td>
<td>INT3</td>
<td>Interrupt 3—trap to debugger</td>
</tr>
<tr>
<td>CD \textsubscript{ib}</td>
<td>INT \textit{imm8}</td>
<td>Interrupt vector numbered by immediate byte</td>
</tr>
<tr>
<td>CE</td>
<td>INTO</td>
<td>Interrupt 4—if overflow flag is 1</td>
</tr>
</tbody>
</table>

**Description**

The INT\textsubscript{n} instruction generates a call to the interrupt or exception handler specified with the destination operand. The destination operand specifies an interrupt vector from 0 to 255, encoded as an 8-bit unsigned intermediate value. The first 32 interrupt vectors are reserved by Intel for system use. Some of these interrupts are used for internally generated exceptions.

The INT\textsubscript{n} instruction is the general mnemonic for executing a software-generated call to an interrupt handler. The INTO instruction is a special mnemonic for calling overflow exception (#OF), interrupt vector 4. The overflow interrupt checks the OF flag in the EFLAGS register and calls the overflow interrupt handler if the OF flag is set to 1.

The INT3 instruction is a special mnemonic for calling the debug exception handler. The action of the INT3 instruction (opcode CC) is slightly different from the operation of the INT 3 instruction (opcode CC03), as follows:

- Interrupt redirection does not happen when in VME mode; the interrupt is handled by a protected-mode handler.
- The virtual-8086 mode IOPL checks do not occur. The interrupt is taken without faulting at any IOPL level.

The action of the INT\textsubscript{n} instruction (including the INTO and INT3 instructions) is similar to that of a far call made with the CALL instruction. The primary difference is that with the INT\textsubscript{n} instruction, the EFLAGS register is pushed onto the stack before the return address. (The return address is a far address consisting of the current values of the CS and EIP registers.) Returns from interrupt procedures are handled with the IRET instruction, which pops the EFLAGS information and return address from the stack.

The interrupt vector specifies an interrupt descriptor in the interrupt descriptor table (IDT); that is, it provides index into the IDT. The selected interrupt descriptor in turn contains a pointer to an interrupt or exception handler procedure. In protected mode, the IDT contains an array of 8-byte descriptors, each of which points to an interrupt gate, trap gate, or task gate. In real-address mode, the IDT is an array of 4-byte far pointers (2-byte code segment selector and a 2-byte instruction pointer), each of which point directly to procedure in the selected segment.

The following decision table indicates which action in the lower portion of the table is taken given the conditions in the upper portion of the table. Each Y in the lower section of the decision table represents a procedure defined in the “Operation” section for this instruction (except #GP).
INT\textsuperscript{n}/INTO/INT3—Call to Interrupt Procedure (Continued)

### Table 1-14. INT Cases

<table>
<thead>
<tr>
<th>PE</th>
<th>0</th>
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<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
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</thead>
<tbody>
<tr>
<td>VM</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
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<td>IOPL</td>
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<td>−</td>
<td>−</td>
<td>−</td>
<td>−</td>
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<td>=3</td>
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<tr>
<td>DPL/CPL RELATIONSHIP</td>
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<td>DPL&lt; CPL</td>
<td>−</td>
<td>DPL&gt; CPL</td>
<td>DPL= CPL or C</td>
<td>DPL&lt; CPL &amp; NC</td>
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<td>INTERRUPT TYPE</td>
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<td>−</td>
<td>−</td>
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<tr>
<td>GATE TYPE</td>
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<td>−</td>
<td>Task</td>
<td>Trap or Interrupt</td>
<td>Trap or Interrupt</td>
<td>Trap or Interrupt</td>
<td>Trap or Interrupt</td>
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<tr>
<td>REAL-ADDRESS-MODE</td>
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<tr>
<td>PROTECTED-MODE</td>
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<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
<td>Y</td>
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<tr>
<td>TRAP-OR- INTERRUPT-GATE</td>
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<td></td>
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<td>INTER-PRIVILEGE-LEVEL-INTERUPT</td>
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<tr>
<td>INTRA-PRIVILEGE-LEVEL-INTERUPT</td>
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<tr>
<td>INTERRUPT-FROM-VIRTUAL-8086-MODE</td>
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<tr>
<td>TASK-GATE</td>
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<td></td>
<td></td>
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<tr>
<td>#GP</td>
<td>Y</td>
<td>Y</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
− Don't Care
Y Yes, Action Taken
Blank Action Not Taken

When the processor is executing in virtual-8086 mode, the IOPL determines the action of the INT\textsuperscript{n} instruction. If the IOPL is less than 3, the processor generates a general protection exception (#GP); if the IOPL is 3, the processor executes a protected mode interrupt to privilege level 0. The interrupt gate's DPL must be set to three and the target CPL of the interrupt handler procedure must be 0 to execute the protected mode interrupt to privilege level 0.

The interrupt descriptor table register (IDTR) specifies the base linear address and limit of the IDT. The initial base address value of the IDTR after the processor is powered up or reset is 0.

**Operation**

The following operational description applies not only to the INT\textsuperscript{n} and INTO instructions, but also to external interrupts and exceptions.

IF Itanium System Environment THEN

IF INT3 Form THEN IA-32_Exception(3);
IF INTO Form THEN IA-32_Exception(4);
IF INT Form THEN IA-32_Interrupt(N);
FI;
INTn/INTO/INT3—Call to Interrupt Procedure (Continued)

/*IN the Itanium System Environment all of the following operations are intercepted*/
IF PE=0
    THEN
        GOTO REAL-ADDRESS-MODE;
    ELSE (* PE=1 *)
        GOTO PROTECTED-MODE;
FI;

REAL-ADDRESS-MODE:
    IF ((DEST ∗ 4) + 3) is not within IDT limit THEN #GP; FI;
    IF stack not large enough for a 6-byte return information THEN #SS; FI;
    Push (EFLAGS[15:0]);
    IF ← 0; (* Clear interrupt flag *)
    TF ← 0; (* Clear trap flag *)
    AC ← 0; (*Clear AC flag*)
    Push(CS);
    Push(IP);
    (* No error codes are pushed *)
    CS ← IDT(Descriptor (vector ∗ 4), selector));
    EIP ← IDT(Descriptor (vector ∗ 4), offset)); (* 16 bit offset AND 0000FFFFH *)
END;

PROTECTED-MODE:
    IF ((DEST ∗ 8) + 7) is not within IDT limits
      OR selected IDT descriptor is not an interrupt-, trap-, or task-gate type
      THEN #GP((DEST ∗ 8) + 2 + EXT);
      (* EXT is bit 0 in error code *)
    FI;
    IF software interrupt (* generated by INTn, INT3, or INTO *)
      THEN
        IF gate descriptor DPL < CPL
          THEN #GP((vector number ∗ 8) + 2 );
          (* PE=1, DPL<CPL, software interrupt *)
        FI;
      FI;
    IF gate not present THEN #NP((vector number ∗ 8) + 2 + EXT); FI;
    IF task gate (* specified in the selected interrupt table descriptor *)
      THEN GOTO TASK-GATE;
      ELSE GOTO TRAP-OR-INTERRUPT-GATE; (* PE=1, trap/interrupt gate *)
    FI;
END;

TASK-GATE: (* PE=1, task gate *)
    Read segment selector in task gate (IDT descriptor);
    IF local/global bit is set to local
      OR index not within GDT limits
      THEN #GP(TSS selector);
    FI;
    Access TSS descriptor in GDT;
    IF TSS descriptor specifies that the TSS is busy (low-order 5 bits set to 00001)
      THEN #GP(TSS selector);
    FI;
    IF TSS not present
INTn/INTO/INT3—Call to Interrupt Procedure (Continued)

    THEN #NP(TSS selector);
    FI;
    SWITCH-TASKS (with nesting) to TSS;
    IF interrupt caused by fault with error code
        THEN
            IF stack limit does not allow push of two bytes
                THEN #SS(0);
            FI;
            Push(error code);
        FI;
    IF EIP not within code segment limit
        THEN #GP(0);
    FI;
END;

TRAP-OR-INTERRUPT-GATE
    Read segment selector for trap or interrupt gate (IDT descriptor);
    IF segment selector for code segment is null
        THEN #GP(0H + EXT); (* null selector with EXT flag set *)
    FI;
    IF segment selector is not within its descriptor table limits
        THEN #GP(selector + EXT);
    FI;
    Read trap or interrupt handler descriptor;
    IF descriptor does not indicate a code segment
        OR code segment descriptor DPL > CPL
            THEN #GP(selector + EXT);
        FI;
    IF trap or interrupt gate segment is not present,
        THEN #NP(selector + EXT);
    FI;
    IF code segment is non-conforming AND DPL < CPL
        THEN IF VM=0
            THEN
                GOTO INTER-PRIVILEGE-LEVEL-INTERRUPT;
            (* PE=1, interrupt or trap gate, nonconforming *)
            (* code segment, DPL<CPL, VM=0 *)
            ELSE (* VM=1 *)
                IF code segment DPL ≠ 0 THEN #GP(new code segment selector); FI;
                GOTO INTERRUPT-FROM-VIRTUAL-8086-MODE;
            (* PE=1, interrupt or trap gate, DPL<CPL, VM=1 *)
        FI;
    ELSE (* PE=1, interrupt or trap gate, DPL ≥ CPL *)
        IF VM=1 THEN #GP(new code segment selector); FI;
        IF code segment is conforming OR code segment DPL = CPL
            THEN
                GOTO INTRA-PRIVILEGE-LEVEL-INTERRUPT;
            ELSE
                #GP(CodeSegmentSelector + EXT);
                (* PE=1, interrupt or trap gate, nonconforming *)
                (* code segment, DPL>CPL *)
        FI;
    FI;
END;
INTn/INTO/INT3—Call to Interrupt Procedure (Continued)

INTER-PRIVILEGE-LEVEL-INTERRUPT
(* PE=1, interrupt or trap gate, non-conforming code segment, DPL<CPL *)
(* Check segment selector and descriptor for stack of new privilege level in current TSS *)
IF current TSS is 32-bit TSS
    THEN
        TSSstackAddress ← new code segment (DPL * 8 + 4)
        IF (TSSstackAddress + 7) > TSS limit
            THEN #TS(current TSS selector); FI;
        NewSS ← TSSstackAddress + 4;
        NewESP ← stack address;
    ELSE (* TSS is 16-bit *)
        TSSstackAddress ← new code segment (DPL * 4 + 2)
        IF (TSSstackAddress + 4) > TSS limit
            THEN #TS(current TSS selector); FI;
        NewESP ← TSSstackAddress;
        NewSS ← TSSstackAddress + 2;
    FI;
    IF segment selector is null THEN #TS(EXT); FI;
    IF segment selector index is not within its descriptor table limits
        OR segment selector’s RPL ≠ DPL of code segment,
            THEN #TS(SS selector + EXT);
    FI;
Read segment descriptor for stack segment in GDT or LDT;
    IF stack segment DPL ≠ DPL of code segment,
        OR stack segment does not indicate writable data segment,
            THEN #TS(SS selector + EXT);
    FI;
    IF stack segment not present THEN #SS(SS selector+EXT); FI;
    IF 32-bit gate
        THEN
            IF new stack does not have room for 24 bytes (error code pushed)
                OR 20 bytes (no error code pushed)
                    THEN #SS(segment selector + EXT);
                FI;
            ELSE (* 16-bit gate *)
                IF new stack does not have room for 12 bytes (error code pushed)
                    OR 10 bytes (no error code pushed);
                        THEN #SS(segment selector + EXT);
                    FI;
            FI;
    IF instruction pointer is not within code segment limits THEN #GP(0); FI;
SS:ESP ← TSS(SS:ESP) (* segment descriptor information also loaded *)
IF 32-bit gate
    THEN
        CS:EIP ← Gate(CS:EIP); (* segment descriptor information also loaded *)
    ELSE (* 16-bit gate *)
        CS:IP ← Gate(CS:IP); (* segment descriptor information also loaded *)
    FI;
    IF 32-bit gate
        THEN
            Push(far pointer to old stack); (* old SS and ESP, 3 words padded to 4 *)
            Push(EFLAGS);
            Push(far pointer to return instruction); (* old CS and EIP, 3 words padded to 4*);
            Push(ErrorCode); (* if needed, 4 bytes *)
**INTn/INTO/INT3—Call to Interrupt Procedure** (Continued)

ELSE(* 16-bit gate *)
  Push(far pointer to old stack); (* old SS and SP, 2 words *);
  Push(EFLAGS);
  Push(far pointer to return instruction); (* old CS and IP, 2 words *);
  Push(ErrorCode); (* if needed, 2 bytes *)
FI;
CPL ← CodeSegmentDescriptor(DPL);
CS(RPL) ← CPL;
IF interrupt gate
  THEN IF ← 0 (* interrupt flag to 0 (disabled) *); FI;
TF ← 0;
VM ← 0;
RF ← 0;
NT ← 0;
END;
INTERRUPT-FROM-VIRTUAL-8086-MODE:
(* Check segment selector and descriptor for privilege level 0 stack in current TSS *)
IF current TSS is 32-bit TSS
  THEN
    TSSstackAddress ← new code segment (DPL * 8) + 4
    IF (TSSstackAddress + 7) > TSS limit
      THEN #TS(current TSS selector); FI;
    NewSS ← TSSstackAddress + 4;
    NewESP ← stack address;
  ELSE (* TSS is 16-bit *)
    TSSstackAddress ← new code segment (DPL * 4) + 2
    IF (TSSstackAddress + 4) > TSS limit
      THEN #TS(current TSS selector); FI;
    NewESP ← TSSstackAddress;
    NewSS ← TSSstackAddress + 2;
FI;
  IF segment selector is null THEN #TS(EXT); FI;
  IF segment selector index is not within its descriptor table limits
    OR segment selector's RPL ≠ DPL of code segment,
    THEN #TS(SS selector + EXT);
FI;
  Access segment descriptor for stack segment in GDT or LDT;
  IF stack segment DPL ≠ DPL of code segment,
    OR stack segment does not indicate writable data segment,
    THEN #TS(SS selector + EXT);
FI;
  IF stack segment not present THEN #SS(SS selector+EXT); FI;
IF 32-bit gate
  THEN
    IF new stack does not have room for 40 bytes (error code pushed)
      OR 36 bytes (no error code pushed);
      THEN #SS(segment selector + EXT);
    FI;
  ELSE(* 16-bit gate *)
    IF new stack does not have room for 20 bytes (error code pushed)
      OR 18 bytes (no error code pushed);
      THEN #SS(segment selector + EXT);
    FI;
FI;
INTn/INTO/INT3—Call to Interrupt Procedure (Continued)

IF instruction pointer is not within code segment limits THEN #GP(0); FI;

IF CR4.VME = 0
    THEN
        IF IOPL=3
            THEN
                IF Gate DPL = 3
                    THEN (*CPL=3, VM=1, IOPL=3, VME=0, gate DPL=3)
                        IF Target CPL != 0
                            THEN #GP(0);
                            ELSE Goto VM86_INTERRUPT_TO_PRIV0;
                        FI;
                        ELSE (*Gate DPL < 3*)
                            #GP(0);
                        FI;
                    ELSE (*IOPL < 3*)
                        #GP(0);
                    FI;
                ELSE (*VME = 1*)
                    (*Check whether interrupt is directed for INT n instruction only,
                     (*executes virtual 8086 interrupt, protected mode interrupt or faults*)
                    Ptr <- [TSS + 66]; (*Fetch IO permission bitmap pointer*
                    IF BIT[Ptr-32,N] = 0 (*software redirection bitmap is 32 bytes below IO
                    Permission*)
                        THEN (*Interrupt redirected*)
                            Goto VM86_INTERRUPT_TO_VM86;
                        ELSE
                            IF IOPL = 3
                                THEN
                                    IF Gate DPL = 3
                                        THEN
                                            IF Target CPL != 0
                                                THEN #GP(0);
                                                ELSE Goto VM86_INTERRUPT_TO_PRIV0;
                                            FI;
                                            ELSE #GP(0);
                                        FI;
                                    ELSE (*IOPL < 3*)
                                        #GP(0);
                                    FI;
                                FI;
                            END;

VM86_INTERRUPT_TO_PRIV0:

tempEFLAGS <- EFLAGS;
VM <- 0;
TF <- 0;
RF <- 0;
IF service through interrupt gate THEN IF <- 0; FI;
TempSS <- SS;
TempESP <- ESP;
INTn/INTO/INT3—Call to Interrupt Procedure (Continued)

SS:ESP ← TSS(SS0:ESP0); (* Change to level 0 stack segment *)
(* Following pushes are 16 bits for 16-bit gate and 32 bits for 32-bit gates *)
(* Segment selector pushes in 32-bit mode are padded to two words *)
Push(GS);
Push(FS);
Push(DS);
Push(ES);
Push(TempSS);
Push(TempESP);
Push(TempEFlags);
Push(CS);
Push(EIP);
GS ← 0; (*segment registers nullified, invalid in protected mode *)
FS ← 0;
DS ← 0;
ES ← 0;
CS ← Gate(CS);
IF OperandSize=32
    THEN
        EIP ← Gate(instruction pointer);
    ELSE (* OperandSize is 16 *)
        EIP ← Gate(instruction pointer) AND 0000FFFFH;
    FI;
(* Starts execution of new routine in Protected Mode *)
END;
VM86_INTERRUPT_TO_VM86:
IF IOPL = 3
    THEN
        push(FLAGS OR 3000H); (*Push FLAGS w/ IOPL bits as 11B or IOPL 3*)
        push(CS);
        push(IP);
        CS ← [N*4 + 2]; (*N is vector num, read from interrupt table*)
        IP ← [N*4];
        FLGS ← FLGS AND 7CD5H; (*Clear TF and IF in EFLAGS like 8086*)
    ELSE
        TempFLGS ← FLGS OR 3000H; (*Set IOPL to 11B or IOPL 3*)
        TempFLGS.IF ← EFLGS.VIF;
        push(TempFLGS);
        push(CS);
        push(IP);
        CS ← [N*4 + 2]; (*N is vector num, read from interrupt table*)
        IP ← [N*4];
        FLGS ← FLGS AND 77ED5H; (*Clear VIF and TF and IF in EFLAGS like 8086*)
    FI;
END;
INTRA-PRIVILEGE-LEVEL-INTERRUPT:
(* PE=1, DPL = CPL or conforming segment *)
IF 32-bit gate
    THEN
        IF current stack does not have room for 16 bytes (error code pushed)
            OR 12 bytes (no error code pushed); THEN #SS(0);
        FI;
INTn/INTO/INT3—Call to Interrupt Procedure (Continued)

ELSE (* 16-bit gate *)
  IF current stack does not have room for 8 bytes (error code pushed)
  OR 6 bytes (no error code pushed); THEN #SS(0);
  FI;
  IF instruction pointer not within code segment limit THEN #GP(0); FI;
IF 32-bit gate
  THEN
    Push (EFLAGS);
    Push (far pointer to return instruction); (* 3 words padded to 4 *)
    CS:EIP ← Gate(CS:EIP); (* segment descriptor information also loaded *)
    Push (ErrorCode); (* if any *)
ELSE (* 16-bit gate *)
  Push (FLAGS);
  Push (far pointer to return location); (* 2 words *)
  CS:IP ← Gate(CS:IP); (* segment descriptor information also loaded *)
  Push (ErrorCode); (* if any *)
FI;
CS(RPL) ← CPL;
IF interrupt gate
  THEN
    IF ← 0; FI;
    TF ← 0;
    NT ← 0;
    VM ← 0;
    RF ← 0;
  FI;
END;

Flags Affected
The EFLAGS register is pushed onto stack. The IF, TF, NT, AC, RF, and VM flags may be cleared, depending on the mode of operation of the processor when the INT instruction is executed (see “Operation” section.)

Additional Itanium® System Environment Exceptions

IA-32_Exception If INT3 or INTO form, vector numbers are 3 and 4 respectively.
IA-32_Interrupt If INT n form, vector number is N.

Protected Mode Exceptions

#GP(0) If the instruction pointer in the IDT or in the interrupt-, trap-, or task gate is beyond the code segment limits.

#GP(selector) If the segment selector in the interrupt-, trap-, or task gate is null.
  If a interrupt-, trap-, or task gate, code segment, or TSS segment selector index is outside its descriptor table limits.
  If the interrupt vector is outside the IDT limits.
  If an IDT descriptor is not an interrupt-, trap-, or task-descriptor.
  If an interrupt is generated by the INTn instruction and the DPL of an interrupt-, trap-, or task-descriptor is less than the CPL.
INTn/INTO/INT3—Call to Interrupt Procedure (Continued)

If the segment selector in an interrupt- or trap-gate does not point to a segment descriptor for a code segment.

If the segment selector for a TSS has its local/global bit set for local.

If a TSS segment descriptor specifies that the TSS is busy or not available.

#SS(0) If pushing the return address, flags, or error code onto the stack exceeds the bounds of the stack segment and no stack switch occurs.

#SS(selector) If the SS register is being loaded and the segment pointed to is marked not present.

If pushing the return address, flags, error code, or stack segment pointer exceeds the bounds of the stack segment.

#NP(selector) If code segment, interrupt-, trap-, or task gate, or TSS is not present.

#TS(selector) If the RPL of the stack segment selector in the TSS is not equal to the DPL of the code segment being accessed by the interrupt or trap gate.

If DPL of the stack segment descriptor pointed to by the stack segment selector in the TSS is not equal to the DPL of the code segment descriptor for the interrupt or trap gate.

If the stack segment selector in the TSS is null.

If the stack segment for the TSS is not a writable data segment.

If segment-selector index for stack segment is outside descriptor table limits.

#PF(fault-code) If a page fault occurs.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the interrupt vector is outside the IDT limits.

#SS If stack limit violation on push.

If pushing the return address, flags, or error code onto the stack exceeds the bounds of the stack segment when a stack switch occurs.

Virtual 8086 Mode Exceptions

#GP(0) (For INTn instruction) If the IOPL is less than 3 and the DPL of the interrupt-, trap-, or task-gate descriptor is not equal to 3.

If the instruction pointer in the IDT or in the interrupt-, trap-, or task gate is beyond the code segment limits.

#GP(selector) If the segment selector in the interrupt-, trap-, or task gate is null.

If a interrupt-, trap-, or task gate, code segment, or TSS segment selector index is outside its descriptor table limits.

If the interrupt vector is outside the IDT limits.

If an IDT descriptor is not an interrupt-, trap-, or task-descriptor.
INTn/INTO/INT3—Call to Interrupt Procedure (Continued)

- If an interrupt is generated by the INTn instruction and the DPL of an interrupt-, trap-, or task-descriptor is less than the CPL.
- If the segment selector in an interrupt- or trap-gate does not point to a segment descriptor for a code segment.
- If the segment selector for a TSS has its local/global bit set for local.

#SS(selector) If the SS register is being loaded and the segment pointed to is marked not present.
- If pushing the return address, flags, error code, stack segment pointer, or data segments exceeds the bounds of the stack segment.

#NP(selector) If code segment, interrupt-, trap-, or task gate, or TSS is not present.

#TS(selector) If the RPL of the stack segment selector in the TSS is not equal to the DPL of the code segment being accessed by the interrupt or trap gate.
- If DPL of the stack segment descriptor for the TSS’s stack segment is not equal to the DPL of the code segment descriptor for the interrupt or trap gate.
- If the stack segment selector in the TSS is null.
- If the stack segment for the TSS is not a writable data segment.
- If segment-selector index for stack segment is outside descriptor table limits.

#PF(fault-code) If a page fault occurs.

#BP If the INT3 instruction is executed.

#OF If the INTO instruction is executed and the OF flag is set.
INVD—Invalidate Internal Caches

Description

Invalidates (flushes) the processor’s internal caches and issues a special-function bus cycle that directs external caches to also flush themselves. Data held in internal caches is not written back to main memory.

After executing this instruction, the processor does not wait for the external caches to complete their flushing operation before proceeding with instruction execution. It is the responsibility of hardware to respond to the cache flush signal.

The INVD instruction is a privileged instruction. When the processor is running in protected mode, the CPL of a program or procedure must be 0 to execute this instruction. This instruction is also implementation-dependent; its function may be implemented differently on future Intel architecture processors.

Use this instruction with care. Data cached internally and not written back to main memory will be lost. Unless there is a specific requirement or benefit to flushing caches without writing back modified cache lines (for example, testing or fault recovery where cache coherency with main memory is not a concern), software should use the WBINVD instruction.

Operation

IF Itanium System Environment THEN IA-32_Intercept(INST,INVD);
Flush(InternalCaches);
SignalFlush(ExternalCaches);
Continue (* Continue execution);

Flags Affected

None.

Additional Itanium® System Environment Exceptions

IA-32_Intercept     Mandatory Instruction Intercept

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0.

Real Address Mode Exceptions

None.

Virtual 8086 Mode Exceptions

#GP(0) The INVD instruction cannot be executed at the virtual 8086 mode.

Opcode | Instruction | Description
-------|-------------|------------------
0F 08   | INVD        | Flush internal caches; initiate flushing of external caches.
INVD—Invalidate Internal Caches (Continued)

Intel® Architecture Compatibility

This instruction is not supported on Intel architecture processors earlier than the Intel486 processor.
## INVLPG—Invalidate TLB Entry

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01/7</td>
<td>INVLPG m</td>
<td>Invalidate TLB Entry for page that contains m</td>
</tr>
</tbody>
</table>

### Description
Invalidates (flushes) the translation lookaside buffer (TLB) entry specified with the source operand. The source operand is a memory address. The processor determines the page that contains that address and flushes the TLB entry for that page.

The INVLPG instruction is a privileged instruction. When the processor is running in protected mode, the CPL of a program or procedure must be 0 to execute this instruction. This instruction is also implementation-dependent; its function may be implemented differently on future Intel architecture processors.

The INVLPG instruction normally flushes the TLB entry only for the specified page; however, in some cases, it flushes the entire TLB.

### Operation

```
IF Itanium System Environment THEN IA-32_Intercept(INST,INVLPG);
Flush(RelevantTLBEntries);
Continue (* Continue execution);
```

### Flags Affected
None.

### Additional Itanium® System Environment Exceptions

**IA-32_Intercept**  
Mandatory Instruction Intercept

### Protected Mode Exceptions

- **#GP(0)**  
  If the current privilege level is not 0.
- **#UD**  
  Operand is a register.

### Real Address Mode Exceptions
None.

### Virtual 8086 Mode Exceptions

- **#GP(0)**  
  The INVLPG instruction cannot be executed at the virtual 8086 mode.

### Intel® Architecture Compatibility

This instruction is not supported on Intel architecture processors earlier than the Intel486 processor.
IRET/IRETD—Interrupt Return

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CF</td>
<td>IRET</td>
<td>Interrupt return (16-bit operand size)</td>
</tr>
<tr>
<td>CF</td>
<td>IRETD</td>
<td>Interrupt return (32-bit operand size)</td>
</tr>
</tbody>
</table>

**Description**

Returns program control from an exception or interrupt handler to a program or procedure that was interrupted by an exception, an external interrupt or, a software-generated interrupt, or returns from a nested task. IRET and IRETD are mnemonics for the same opcode. The IRETD mnemonic (interrupt return double) is intended for use when returning from an interrupt when using the 32-bit operand size; however, most assemblers use the IRET mnemonic interchangeably for both operand sizes.

In Real Address Mode, the IRET instruction performs a far return to the interrupted program or procedure. During this operation, the processor pops the return instruction pointer, return code segment selector, and EFLAGS image from the stack to the EIP, CS, and EFLAGS registers, respectively, and then resumes execution of the interrupted program or procedure.

In Protected Mode, the action of the IRET instruction depends on the settings of the NT (nested task) and VM flags in the EFLAGS register and the VM flag in the EFLAGS image stored on the current stack. Depending on the setting of these flags, the processor performs the following types of interrupt returns:

- Real Mode.
- Return from virtual-8086 mode.
- Return to virtual-8086 mode.
- Intra-privilege level return.
- Inter-privilege level return.

**Return from nested task (task switch)**

All forms of IRET result in an IA-32_Intercept(Inst,IRET) in the Itanium System Environment.

If the NT flag (EFLAGS register) is cleared, the IRET instruction performs a far return from the interrupt procedure, without a task switch. The code segment being returned to must be equally or less privileged than the interrupt handler routine (as indicated by the RPL field of the code segment selector popped from the stack). As with a real-address mode interrupt return, the IRET instruction pops the return instruction pointer, return code segment selector, and EFLAGS image from the stack to the EIP, CS, and EFLAGS registers, respectively, and then resumes execution of the interrupted program or procedure. If the return is to another privilege level, the IRET instruction also pops the stack pointer and SS from the stack, before resuming program execution. If the return is to virtual-8086 mode, the processor also pops the data segment registers from the stack.

If the NT flag is set, the IRET instruction performs a return from a nested task (switches from the called task back to the calling task) or reverses the operation of an interrupt or exception that caused a task switch. The updated state of the task executing the IRET instruction is saved in its TSS. If the task is reentered later, the code that follows the IRET instruction is executed.

IRET performs an instruction serialization and a memory fence operation.
IRET/IRETD—Interrupt Return (Continued)

Operation

IF(Itanium System Environment)
    THEN IA-32_Intercept(Inst.IRET);

IF PE = 0
    THEN
        GOTO REAL-ADDRESS-MODE;;
    ELSE
        GOTO PROTECTED-MODE;
    FI;

REAL-ADDRESS-MODE:
    IF OperandSize = 32
        THEN
            IF top 12 bytes of stack not within stack limits THEN #SS; FI;
            IF instruction pointer not within code segment limits THEN #GP(0); FI;
            EIP ← Pop();
            CS ← Pop(); (* 32-bit pop, high-order 16-bits discarded *)
            tempEFLAGS ← Pop();
            EFLAGS ← (tempEFLAGS AND 257FD5H) OR (EFLAGS AND 1A0000H);
        ELSE (* OperandSize = 16 *)
            IF top 6 bytes of stack are not within stack limits THEN #SS; FI;
            IF instruction pointer not within code segment limits THEN #GP(0); FI;
            EIP ← Pop();
            EIP ← EIP AND 0000FFFFH;
            CS ← Pop(); (* 16-bit pop *)
            EFLAGS[15:0] ← Pop();
        FI;
    END;

PROTECTED-MODE:
    IF VM = 1 (* Virtual-8086 mode: PE=1, VM=1 *)
        THEN
            GOTO RETURN-FROM-VIRTUAL-8086-MODE; (* PE=1, VM=1 *)
    FI;
    IF NT = 1
        THEN
            GOTO TASK-RETURN;(* PE=1, VM=0, NT=1 *)
    FI;

    IF OperandSize=32
        THEN
            IF top 12 bytes of stack not within stack limits
                THEN #SS(0)
            FI;
            tempEIP ← Pop();
            tempCS ← Pop();
            tempEFLAGS ← Pop();
        ELSE (* OperandSize = 16 *)
            IF top 6 bytes of stack are not within stack limits
                THEN #SS(0);
            FI;
IRET/IRETD—Interrupt Return (Continued)

    FL;
    tempEIP ← Pop();
    tempCS ← Pop();
    tempEFLAGS ← Pop();
    tempEIP ← tempEIP AND FFFFH;
    tempEFLAGS ← tempEFLAGS AND FFFFH;
    FI;
    IF tempEFLAGS(VM) = 1 AND CPL=0
      THEN
        GOTO RETURN-TO-VIRTUAL-8086-MODE;
        (* PE=1, VM=1 in EFLAGS image *)
      ELSE
        GOTO PROTECTED-MODE-RETURN;
        (* PE=1, VM=0 in EFLAGS image *)
      FI;
RETURN-FROM-VIRTUAL-8086-MODE:
(* Processor is in virtual-8086 mode when IRET is executed and stays in virtual-8086 mode *)

    IF CR4.VME = 0
    THEN
      IF IOPL=3 (* Virtual mode: PE=1, VM=1, IOPL=3 *)
        THEN
          IF OperandSize = 32
            THEN
              IF top 12 bytes of stack not within stack limits THEN #SS(0); FI;
              IF instruction pointer not within code segment limits THEN #GP(0); FI;
              EIP ← Pop();
              CS ← Pop(); (* 32-bit pop, high-order 16-bits discarded *)
              EFLAGS ← Pop();
              (*VM,IOPL,VIP,and VIF EFLAGS bits are not modified by pop *)
            ELSE (* OperandSize = 16 *)
              IF top 6 bytes of stack are not within stack limits THEN #SS(0); FI;
              IF instruction pointer not within code segment limits THEN #GP(0); FI;
              EIP ← Pop();
              EIP ← EIP AND 0000FFFFH;
              CS ← Pop(); (* 16-bit pop *)
              EFLAGS[15:0] ← Pop(); (* IOPL in EFLAGS is not modified by pop *)
            FI;
          ELSE #GP(0); (* trap to virtual-8086 monitor: PE=1, VM=1, IOPL<3 *)
        FI;
      ELSE (*VME is 1*)
        IF IOPL = 3
          THEN
            IF OperandSize = 32
              THEN
                EIP ← Pop();
                CS ← Pop(); (* 32-bit pop, high-order 16-bits discarded *)
                TempEFlags ← Pop();
                FLAGS = (EFLAGS AND 1B3000H) OR (TempEFlags AND 244FD7H)
                (*VM,IOPL,RF,VIP,and VIF EFLAGS bits are not modified by pop *)
              ELSE (* OperandSize = 16 *)
                EIP ← Pop();
                EIP ← EIP AND 0000FFFFH;
IRET/IRETD—Interrupt Return (Continued)

CS ← Pop(); (* 16-bit pop *)
TempFlags ← Pop();
FLAGS = (FLAGS AND 3000H) OR (TempFlags AND 4FD5H)
(*IOPL unmodified*)
FI;
ELSE (*IOPL < 3*)
IF OperandSize = 16
THEN
IF ((STACK.TF !-0) OR (EFLAGS.VIP=1 AND STACK.IF=1))
THEN #GP(0);
ELSE
IF OperandSize = 32 *)
#GP(0);
FI;
END;

RETURN-TO-VIRTUAL-8086-MODE:
(* Interrupted procedure was in virtual-8086 mode: PE=1, VM=1 in flags image *)
IF top 24 bytes of stack are not within stack segment limits
THEN #SS(0);
FI;
IF instruction pointer not within code segment limits
THEN #GP(0);
FI;
CS ← tempCS;
EIP ← tempEIP;
EFLAGS ← tempEFLAGS
TempESP ← Pop();
TempSS ← Pop();
ES ← Pop(); (* pop 2 words; throw away high-order word *)
DS ← Pop(); (* pop 2 words; throw away high-order word *)
FS ← Pop(); (* pop 2 words; throw away high-order word *)
GS ← Pop(); (* pop 2 words; throw away high-order word *)
SS:ESP ← TempSS:TempESP;
(* Resume execution in Virtual 8086 mode *)
END;

TASK-RETURN: (* PE=1, VM=1, NT=1 *)
Read segment selector in link field of current TSS;
IF local/global bit is set to local
OR index not within GDT limits
THEN #GP(TSS selector);
FI;
Access TSS for task specified in link field of current TSS;
IRET/IRETD—Interrupt Return (Continued)

IF TSS descriptor type is not TSS or if the TSS is marked not busy
    THEN #GP(TSS selector);
FI;
IF TSS not present
    THEN #NP(TSS selector);
FI;
SWITCH-TASKS (without nesting) to TSS specified in link field of current TSS;
Mark the task just abandoned as NOT BUSY;
IF EIP is not within code segment limit
    THEN #GP(0);
FI;
END;

PROTECTED-MODE-RETURN: (* PE=1, VM=0 in flags image *)
    IF return code segment selector is null THEN GP(0); FI;
    IF return code segment selector addresses descriptor beyond descriptor table limit
        THEN GP(selector); FI;
Read segment descriptor pointed to by the return code segment selector
    IF return code segment descriptor is not a code segment THEN #GP(selector); FI;
    IF return code segment selector RPL < CPL THEN #GP(selector); FI;
    IF return code segment descriptor is conforming
        AND return code segment DPL > return code segment selector RPL
            THEN #GP(selector); FI;
    IF return code segment descriptor is not present THEN #NP(selector); FI;
    IF return code segment selector RPL > CPL
        THEN GOTO RETURN-OUTER-PRIVILEGE-LEVEL;
        ELSE GOTO RETURN-TO-SAME-PRIVILEGE-LEVEL
FI;
END;

RETURN-TO-SAME-PRIVILEGE-LEVEL: (* PE=1, VM=0 in flags image, RPL=CPL *)
    IF EIP is not within code segment limits THEN #GP(0); FI;
    EIP ← tempEIP;
    CS ← tempCS; (* segment descriptor information also loaded *)
    EFLAGS (CF, PF, AF, ZF, SF, TF, DF, OF, NT) ← tempEFLAGS;
    IF OperandSize=32
        THEN
            EFLAGS(RF, AC, ID) ← tempEFLAGS;
        FI;
    IF CPL ≤ IOPL
        THEN
            EFLAGS(IF) ← tempEFLAGS;
        FI;
    IF CPL = 0
        THEN
            EFLAGS(IOPL) ← tempEFLAGS;
            IF OperandSize=32
                THEN EFLAGS(VM, VIF, VIP) ← tempEFLAGS;
            FI;
        FI;
    END;

RETURN-TO-OUTER-PRIVILEGE-LEVEL:
IRET/IRETD—Interrupt Return (Continued)

IF OperandSize=32
THEN
    IF top 8 bytes on stack are not within limits THEN #SS(0); FI;
ELSE (* OperandSize=16 *)
    IF top 4 bytes on stack are not within limits THEN #SS(0); FI;
FI;
Read return segment selector;
IF stack segment selector is null THEN #GP(0); FI;
IF return stack segment selector index is not within its descriptor table limits
THEN #GP(SSselector); FI;
Read segment descriptor pointed to by return segment selector;
IF stack segment selector RPL ≠ RPL of the return code segment selector
    IF stack segment selector RPL ≠ RPL of the return code segment selector
        OR the stack segment descriptor does not indicate a writable data segment;
        OR stack segment DPL ≠ RPL of the return code segment selector
        THEN #GP(SS selector); FI;
    FI;
    IF stack segment is not present THEN #NP(SS selector); FI;
EIP ← tempEIP;
CS ← tempCS;
EFLAGS (CF, PF, AF, ZF, SF, TF, DF, OF, NT) ← tempEFLAGS;
IF OperandSize=32
THEN
    EFLAGS(RF, AC, ID) ← tempEFLAGS;
FI;
IF CPO ≤ IOPL
THEN
    EFLAGS(IF) ← tempEFLAGS;
FI;
IF CPL = 0
THEN
    EFLAGS(IOPL) ← tempEFLAGS;
    IF OperandSize=32
        THEN EFLAGS(VM, VIF, VIP) ← tempEFLAGS;
    FI;
    FI;
CPL ← RPL of the return code segment selector;
FOR each of segment register (ES, FS, GS, and DS)
DO;
    IF segment register points to data or non-conforming code segment
    AND CPL > segment descriptor DPL (* stored in hidden part of segment register *)
    THEN (* segment register invalid *)
        SegmentSelector ← 0; (* null segment selector *)
    FI;
OD;
END:
IRET/IRETD—Interrupt Return (Continued)

Flags Affected

All the flags and fields in the EFLAGS register are potentially modified, depending on the mode of operation of the processor.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
- IA-32_Intercept: Instruction Intercept Trap for ALL forms of IRET.

Protected Mode Exceptions

- #GP(0): If the return code or stack segment selector is null.
- #GP(selector): If the return instruction pointer is not within the return code segment limit.
- #GP(selector): If a segment selector index is outside its descriptor table limits.
- #GP(selector): If the return code segment selector RPL is greater than the CPL.
- #GP(selector): If the DPL of a conforming-code segment is greater than the return code segment selector RPL.
- #GP(selector): If the DPL for a nonconforming-code segment is not equal to the RPL of the code segment selector.
- #GP(selector): If the stack segment descriptor DPL is not equal to the RPL of the return code segment selector.
- #GP(selector): If the stack segment is not a writable data segment.
- #GP(selector): If the stack segment selector RPL is not equal to the RPL of the return code segment selector.
- #GP(selector): If the segment descriptor for a code segment does not indicate it is a code segment.
- #GP(selector): If the segment selector for a TSS has its local/global bit set for local.
- #GP(selector): If a TSS segment descriptor specifies that the TSS is busy or not available.
- #SS(0): If the top bytes of stack are not within stack limits.
- #NP(selector): If the return code or stack segment is not present.
- #PF(fault-code): If a page fault occurs.
- #AC(0): If an unaligned memory reference occurs when the CPL is 3 and alignment checking is enabled.

Real Address Mode Exceptions

- #GP: If the return instruction pointer is not within the return code segment limit.
- #SS: If the top bytes of stack are not within stack limits.
IRET/IRETD—Interrupt Return (Continued)

Virtual 8086 Mode Exceptions

#GP(0) If the return instruction pointer is not within the return code segment limit.
    IF IOPL not equal to 3
#PF(fault-code) If a page fault occurs.
#SS(0) If the top bytes of stack are not within stack limits.
#AC(0) If an unaligned memory reference occurs and alignment checking is enabled.
## Jcc—Jump if Condition Is Met

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>77 cb</td>
<td>JA rel8</td>
<td>Jump short if above (CF=0 and ZF=0)</td>
</tr>
<tr>
<td>73 cb</td>
<td>JAE rel8</td>
<td>Jump short if above or equal (CF=0)</td>
</tr>
<tr>
<td>72 cb</td>
<td>JB rel8</td>
<td>Jump short if below (CF=1)</td>
</tr>
<tr>
<td>76 cb</td>
<td>JBE rel8</td>
<td>Jump short if below or equal (CF=1 or ZF=1)</td>
</tr>
<tr>
<td>72 cb</td>
<td>JC rel8</td>
<td>Jump short if carry (CF=1)</td>
</tr>
<tr>
<td>E3 cb</td>
<td>JCXZ rel8</td>
<td>Jump short if CX register is 0</td>
</tr>
<tr>
<td>E3 cb</td>
<td>JE CXZ rel8</td>
<td>Jump short if ECX register is 0</td>
</tr>
<tr>
<td>74 cb</td>
<td>JE rel8</td>
<td>Jump short if equal (ZF=1)</td>
</tr>
<tr>
<td>7F cb</td>
<td>JG rel8</td>
<td>Jump short if greater (ZF=0 and SF=OF)</td>
</tr>
<tr>
<td>7D cb</td>
<td>JGE rel8</td>
<td>Jump short if greater or equal (SF=OF)</td>
</tr>
<tr>
<td>7C cb</td>
<td>JL rel8</td>
<td>Jump short if less (SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>7E cb</td>
<td>JLE rel8</td>
<td>Jump short if less or equal (ZF=1 or SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>76 cb</td>
<td>JNA rel8</td>
<td>Jump short if not above (CF=1 or ZF=1)</td>
</tr>
<tr>
<td>72 cb</td>
<td>JNBE rel8</td>
<td>Jump short if not below or equal (CF=0 and ZF=0)</td>
</tr>
<tr>
<td>73 cb</td>
<td>JNC rel8</td>
<td>Jump short if not carry (CF=0)</td>
</tr>
<tr>
<td>75 cb</td>
<td>JNE rel8</td>
<td>Jump short if not equal (ZF=0)</td>
</tr>
<tr>
<td>7E cb</td>
<td>JNG rel8</td>
<td>Jump short if not greater (ZF=1 or SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>7C cb</td>
<td>JNGE rel8</td>
<td>Jump short if not greater or equal (SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>7D cb</td>
<td>JNL rel8</td>
<td>Jump short if not less (SF=OF)</td>
</tr>
<tr>
<td>7F cb</td>
<td>JNLE rel8</td>
<td>Jump short if not less or equal (ZF=0 and SF=OF)</td>
</tr>
<tr>
<td>71 cb</td>
<td>JNO rel8</td>
<td>Jump short if not overflow (OF=0)</td>
</tr>
<tr>
<td>7B cb</td>
<td>JNP rel8</td>
<td>Jump short if not parity (PF=0)</td>
</tr>
<tr>
<td>79 cb</td>
<td>JNS rel8</td>
<td>Jump short if not sign (SF=0)</td>
</tr>
<tr>
<td>75 cb</td>
<td>JNZ rel8</td>
<td>Jump short if not zero (ZF=0)</td>
</tr>
<tr>
<td>70 cb</td>
<td>JO rel8</td>
<td>Jump short if overflow (OF=1)</td>
</tr>
<tr>
<td>7A cb</td>
<td>JP rel8</td>
<td>Jump short if parity (PF=1)</td>
</tr>
<tr>
<td>7A cb</td>
<td>JPE rel8</td>
<td>Jump short if parity even (PF=1)</td>
</tr>
<tr>
<td>7B cb</td>
<td>JPO rel8</td>
<td>Jump short if parity odd (PF=0)</td>
</tr>
<tr>
<td>78 cb</td>
<td>JS rel8</td>
<td>Jump short if sign (SF=1)</td>
</tr>
<tr>
<td>74 cb</td>
<td>JZ rel8</td>
<td>Jump short if zero (ZF = 1)</td>
</tr>
<tr>
<td>0F 87 cw/cd</td>
<td>JA rel16/32</td>
<td>Jump near if above (CF=0 and ZF=0)</td>
</tr>
<tr>
<td>0F 83 cw/cd</td>
<td>JAE rel16/32</td>
<td>Jump near if above or equal (CF=0)</td>
</tr>
<tr>
<td>0F 82 cw/cd</td>
<td>JB rel16/32</td>
<td>Jump near if below (CF=1)</td>
</tr>
<tr>
<td>0F 86 cw/cd</td>
<td>JBE rel16/32</td>
<td>Jump near if below or equal (CF=1 or ZF=1)</td>
</tr>
<tr>
<td>0F 82 cw/cd</td>
<td>JC rel16/32</td>
<td>Jump near if carry (CF=1)</td>
</tr>
<tr>
<td>0F 84 cw/cd</td>
<td>JE rel16/32</td>
<td>Jump near if equal (ZF=1)</td>
</tr>
<tr>
<td>0F 84 cw/cd</td>
<td>JZ rel16/32</td>
<td>Jump near if 0 (ZF=1)</td>
</tr>
<tr>
<td>0F 8F cw/cd</td>
<td>JG rel16/32</td>
<td>Jump near if greater (ZF=0 and SF=OF)</td>
</tr>
</tbody>
</table>
### Jcc—Jump if Condition Is Met (Continued)

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 8D cw/cd</td>
<td>JGE rel16/32</td>
<td>Jump near if greater or equal (SF=OF)</td>
</tr>
<tr>
<td>0F 8C cw/cd</td>
<td>JL rel16/32</td>
<td>Jump near if less (SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 8E cw/cd</td>
<td>JLE rel16/32</td>
<td>Jump near if less or equal (ZF=1 or SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 86 cw/cd</td>
<td>JNA rel16/32</td>
<td>Jump near if not above (CF=1 or ZF=1)</td>
</tr>
<tr>
<td>0F 82 cw/cd</td>
<td>JNAE rel16/32</td>
<td>Jump near if not above or equal (CF=1)</td>
</tr>
<tr>
<td>0F 83 cw/cd</td>
<td>JNB rel16/32</td>
<td>Jump near if not below (CF=0)</td>
</tr>
<tr>
<td>0F 87 cw/cd</td>
<td>JNBE rel16/32</td>
<td>Jump near if not below or equal (CF=0 and ZF=0)</td>
</tr>
<tr>
<td>0F 83 cw/cd</td>
<td>JNC rel16/32</td>
<td>Jump near if not carry (CF=0)</td>
</tr>
<tr>
<td>0F 85 cw/cd</td>
<td>JNA rel16/32</td>
<td>Jump near if not equal (ZF=0)</td>
</tr>
<tr>
<td>0F 8E cw/cd</td>
<td>JNG rel16/32</td>
<td>Jump near if not greater (ZF=1 or SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 8C cw/cd</td>
<td>JNGE rel16/32</td>
<td>Jump near if not greater or equal (SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 8D cw/cd</td>
<td>JNL rel16/32</td>
<td>Jump near if not less (SF=OF)</td>
</tr>
<tr>
<td>0F 8F cw/cd</td>
<td>JNLE rel16/32</td>
<td>Jump near if not less or equal (ZF=0 and SF=OF)</td>
</tr>
<tr>
<td>0F 81 cw/cd</td>
<td>JNO rel16/32</td>
<td>Jump near if not overflow (OF=0)</td>
</tr>
<tr>
<td>0F 8B cw/cd</td>
<td>JNP rel16/32</td>
<td>Jump near if not parity (PF=0)</td>
</tr>
<tr>
<td>0F 89 cw/cd</td>
<td>JNS rel16/32</td>
<td>Jump near if not sign (SF=0)</td>
</tr>
<tr>
<td>0F 85 cw/cd</td>
<td>JNZ rel16/32</td>
<td>Jump near if not zero (ZF=0)</td>
</tr>
<tr>
<td>0F 80 cw/cd</td>
<td>JO rel16/32</td>
<td>Jump near if overflow (OF=1)</td>
</tr>
<tr>
<td>0F 8A cw/cd</td>
<td>JP rel16/32</td>
<td>Jump near if parity (PF=1)</td>
</tr>
<tr>
<td>0F 8A cw/cd</td>
<td>JPE rel16/32</td>
<td>Jump near if parity even (PF=1)</td>
</tr>
<tr>
<td>0F 8B cw/cd</td>
<td>JPO rel16/32</td>
<td>Jump near if parity odd (PF=0)</td>
</tr>
<tr>
<td>0F 88 cw/cd</td>
<td>JS rel16/32</td>
<td>Jump near if sign (SF=1)</td>
</tr>
<tr>
<td>0F 84 cw/cd</td>
<td>JZ rel16/32</td>
<td>Jump near if 0 (ZF=1)</td>
</tr>
</tbody>
</table>

**Description**

Checks the state of one or more of the status flags in the EFLAGS register (CF, OF, PF, SF, and ZF) and, if the flags are in the specified state (condition), performs a jump to the target instruction specified by the destination operand. A condition code (cc) is associated with each instruction to indicate the condition being tested for. If the condition is not satisfied, the jump is not performed and execution continues with the instruction following the Jcc instruction.

The target instruction is specified with a relative offset (a signed offset relative to the current value of the instruction pointer in the EIP register). A relative offset (rel8, rel16, or rel32) is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed, 8-bit or 32-bit immediate value, which is added to the instruction pointer. Instruction coding is most efficient for offsets of –128 to +127. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared to 0s, resulting in a maximum instruction pointer size of 16 bits.

The conditions for each Jcc mnemonic are given in the “Description” column of the above table. The terms “less” and “greater” are used for comparisons of signed integers and the terms “above” and “below” are used for unsigned integers.
Jcc—Jump if Condition Is Met (Continued)

Because a particular state of the status flags can sometimes be interpreted in two ways, two mnemonics are defined for some opcodes. For example, the JA (jump if above) instruction and the JNBE (jump if not below or equal) instruction are alternate mnemonics for the opcode 77H.

The Jcc instruction does not support far jumps (jumps to other code segments). When the target for the conditional jump is in a different segment, use the opposite condition from the condition being tested for the Jcc instruction, and then access the target with an unconditional far jump (JMP instruction) to the other segment. For example, the following conditional far jump is illegal:

```
   JZ          FARLABEL;
```

To accomplish this far jump, use the following two instructions:

```
   JNZ         BEYOND;
   JMP          FARLABEL;
   BEYOND:
```

The JEZX and JCXZ instructions differ from the other Jcc instructions because they do not check the status flags. Instead they check the contents of the ECX and CX registers, respectively, for 0. These instructions are useful at the beginning of a conditional loop that terminates with a conditional loop instruction (such as LOOPNE). They prevent entering the loop when the ECX or CX register is equal to 0, which would cause the loop to execute $2^{32}$ or 64K times, respectively, instead of zero times.

All conditional jumps are converted to code fetches of one or two cache lines, regardless of jump address or cacheability.

**Operation**

```
IF condition THEN
  EIP ← EIP + SignExtend(DEST);
IF OperandSize = 16 THEN
  EIP ← EIP AND 0000FFFFH;
FI;
IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
FI;
```

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

IA-32_Exception Taken Branch Debug Exception if PSR.tb is 1

**Protected Mode Exceptions**

#GP(0) If the offset being jumped to is beyond the limits of the CS segment.
Jcc—Jump if Condition Is Met (Continued)

Real Address Mode Exceptions

#GP        If the offset being jumped to is beyond the limits of the CS segment or is outside of the effective address space from 0 to FFFFH. This condition can occur if 32-address size override prefix is used.

Virtual 8086 Mode Exceptions

#GP(0)     If the offset being jumped to is beyond the limits of the CS segment or is outside of the effective address space from 0 to FFFFH. This condition can occur if 32-address size override prefix is used.
JMP—Jump

### Description

Transfers program control to a different point in the instruction stream without recording return information. The destination (target) operand specifies the address of the instruction being jumped to. This operand can be an immediate value, a general-purpose register, or a memory location.

- **Near jump** – A jump to an instruction within the current code segment (the segment currently pointed to by the CS register), sometimes referred to as an intrasegment call.
- **Far jump** – A jump to an instruction located in a different segment than the current code segment, sometimes referred to as an intersegment call.
- **Task switch** – A jump to an instruction located in a different task. (This is a form of a far jump.) Results in an IA-32 Intercept(Gate) in Itanium System Environment.

A task switch can only be executed in protected mode (see Chapter 6 in the IA-32 Intel® Architecture Software Developer’s Manual, Volume 3 for information on task switching with the JMP instruction).

When executing a near jump, the processor jumps to the address (within the current code segment) that is specified with the target operand. The target operand specifies either an absolute address (that is an offset from the base of the code segment) or a relative offset (a signed offset relative to the current value of the instruction pointer in the EIP register). An absolute address is specified directly in a register or indirectly in a memory location (r/m16 or r/m32 operand form). A relative offset (rel8, rel16, or rel32) is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed, 8-bit or 32-bit immediate value, which is added to the value in the EIP register (that is, to the instruction following the JMP instruction). The operand-size attribute determines the size of the target operand (16 or 32 bits) for absolute addresses. Absolute addresses are loaded directly into the EIP register. When a relative offset is specified, it is added to the value of the EIP register. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared to 0s, resulting in a maximum instruction pointer size of 16 bits. The CS register is not changed on near jumps.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EB cb</td>
<td>JMP rel8</td>
<td>Jump near, relative address</td>
</tr>
<tr>
<td>E9 cw</td>
<td>JMP rel16</td>
<td>Jump near, relative address</td>
</tr>
<tr>
<td>E9 cd</td>
<td>JMP rel32</td>
<td>Jump near, relative address</td>
</tr>
<tr>
<td>FF /4</td>
<td>JMP r/m16</td>
<td>Jump near, indirect address</td>
</tr>
<tr>
<td>FF /4</td>
<td>JMP r/m32</td>
<td>Jump near, indirect address</td>
</tr>
<tr>
<td>EA cd</td>
<td>JMP ptr16:16</td>
<td>Jump far, absolute address</td>
</tr>
<tr>
<td>EA cp</td>
<td>JMP ptr16:32</td>
<td>Jump far, absolute address</td>
</tr>
<tr>
<td>FF /5</td>
<td>JMP m16:16</td>
<td>Jump far, indirect address</td>
</tr>
<tr>
<td>FF /5</td>
<td>JMP m16:32</td>
<td>Jump far, indirect address</td>
</tr>
</tbody>
</table>
JMP—Jump (Continued)

When executing a far jump, the processor jumps to the code segment and address specified with the target operand. Here the target operand specifies an absolute far address either directly with a pointer (\texttt{ptr16:16} or \texttt{ptr16:32}) or indirectly with a memory location (\texttt{m16:16} or \texttt{m16:32}). With the pointer method, the segment and address of the called procedure is encoded in the instruction using a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address immediate. With the indirect method, the target operand specifies a memory location that contains a 4-byte (16-bit operand size) or 6-byte (32-bit operand size) far address. The operand-size attribute determines the size of the offset (16 or 32 bits) in the far address. The far address is loaded directly into the CS and EIP registers. If the operand-size attribute is 16, the upper two bytes of the EIP register are cleared to 0s.

When the processor is operating in protected mode, a far jump can also be used to access a code segment through a call gate or to switch tasks. Here, the processor uses the segment selector part of the far address to access the segment descriptor for the segment being jumped to. Depending on the value of the type and access rights information in the segment selector, the JMP instruction can perform:

- A far jump to a conforming or non-conforming code segment (same mechanism as the far jump described in the previous paragraph, except that the processor checks the access rights of the code segment being jumped to).
- An far jump through a call gate.
- A task switch. \textbf{Results in an IA-32 Intercept(Gate) in Itanium System Environment.}

The JMP instruction cannot be used to perform inter-privilege level jumps.

When executing an far jump through a call gate, the segment selector specified by the target operand identifies the call gate. (The offset part of the target operand is ignored.) The processor then jumps to the code segment specified in the call gate descriptor and begins executing the instruction at the offset specified in the gate. No stack switch occurs. Here again, the target operand can specify the far address of the call gate and instruction either directly with a pointer (\texttt{ptr16:16} or \texttt{ptr16:32}) or indirectly with a memory location (\texttt{m16:16} or \texttt{m16:32}).

Executing a task switch with the JMP instruction, is similar to executing a jump through a call gate. Here the target operand specifies the segment selector of the task gate for the task being switched to. (The offset part of the target operand is ignored). The task gate in turn points to the TSS for the task, which contains the segment selectors for the task’s code, data, and stack segments and the instruction pointer to the target instruction. One form of the JMP instruction allows the jump to be made directly to a TSS, without going through a task gate. See Chapter 13 in \textit{IA-32 Intel Architecture Software Developer’s Manual, Volume 3} the for detailed information on the mechanics of a task switch.

All branches are converted to code fetches of one or two cache lines, regardless of jump address or cacheability.
JMP—Jump (Continued)

Operation
IF near jump
    THEN IF near relative jump
        THEN
            tempEIP ← EIP + DEST; (* EIP is instruction following JMP instruction *)
        ELSE (* near absolute jump *)
            tempEIP ← DEST;
        FI;
    IF tempEIP is beyond code segment limit THEN #GP(0); FI;
    IF OperandSize = 32
        THEN
            EIP ← tempEIP;
        ELSE (* OperandSize=16 *)
            EIP ← tempEIP AND 0000FFFFH;
        FI;
    IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
FI;

IF far jump AND (PE = 0 OR (PE = 1 AND VM = 1)) (* real address or virtual 8086 mode *)
    THEN
        tempEIP ← DEST(offset); (* DEST is ptr16:32 or [m16:32] *)
        IF tempEIP is beyond code segment limit THEN #GP(0); FI;
        CS ← DEST(segment selector); (* DEST is ptr16:32 or [m16:32] *)
        IF OperandSize = 32
            THEN
                EIP ← tempEIP; (* DEST is ptr16:32 or [m16:32] *)
            ELSE (* OperandSize = 16 *)
                EIP ← tempEIP AND 0000FFFFH; (* clear upper 16 bits *)
            FI;
        IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
    FI;

IF far call AND (PE = 1 AND VM = 0) (* Protected mode, not virtual 8086 mode *)
    THEN
        IF effective address in the CS, DS, ES, FS, GS, or SS segment is illegal
            OR segment selector in target operand null
            THEN #GP(0);
        FI;
        IF segment selector index not within descriptor table limits
            THEN #GP(new selector);
        FI;
        Read type and access rights of segment descriptor;
        IF segment type is not a conforming or nonconforming code segment, call gate, task gate, or TSS THEN #GP(segment selector); FI;
        Depending on type and access rights
            GO TO CONFORMING-CODE-SEGMENT;
            GO TO NONCONFORMING-CODE-SEGMENT;
            GO TO CALL-GATE;
            GO TO TASK-GATE;
            GO TO TASK-STATE-SEGMENT;
        ELSE
            #GP(segment selector);
        FI;
    FI;
JMP—Jump (Continued)

CONFORMING-CODE-SEGMENT:
IF DPL > CPL THEN #GP(segment selector); FI;
IF segment not present THEN #NP(segment selector); FI;
tempEIP ← DEST(offset);
IF OperandSize=16
    THEN tempEIP ← tempEIP AND 0000FFFFH;
FI;
IF tempEIP not in code segment limit THEN #GP(0); FI;
CS ← DEST(SegmentSelector); (* segment descriptor information also loaded *)
CS(RPL) ← CPL
EIP ← tempEIP;
IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
END;

NONCONFORMING-CODE-SEGMENT:
IF (RPL > CPL) OR (DPL ≠ CPL) THEN #GP(code segment selector); FI;
IF segment not present THEN #NP(segment selector); FI;
IF instruction pointer outside code segment limit THEN #GP(0); FI;
tempEIP ← DEST(offset);
IF OperandSize=16
    THEN tempEIP ← tempEIP AND 0000FFFFH;
FI;
IF tempEIP not in code segment limit THEN #GP(0); FI;
CS ← DEST(SegmentSelector); (* segment descriptor information also loaded *)
CS(RPL) ← CPL
EIP ← tempEIP;
IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
END;

CALL-GATE:
IF call gate DPL < CPL
    OR call gate DPL < call gate segment-selector RPL
    THEN #GP(call gate selector); FI;
IF call gate not present THEN #NP(call gate selector); FI;
IF Itanium System Environment THEN IA-32_Intercept(Gate,JMP);
IF call gate code-segment selector is null THEN #GP(0); FI;
IF call gate code-segment selector index is outside descriptor table limits
    THEN #GP(code segment selector); FI;
Read code segment descriptor;
IF code-segment segment descriptor does not indicate a code segment
    OR code-segment segment descriptor is conforming and DPL > CPL
    OR code-segment segment descriptor is non-conforming and DPL ≠ CPL
    THEN #GP(code segment selector); FI;
IF code segment is not present THEN #NP(code-segment selector); FI;
IF instruction pointer is not within code-segment limit THEN #GP(0); FI;
tempEIP ← DEST(offset);
IF GateSize=16
    THEN tempEIP ← tempEIP AND 0000FFFFH;
FI;
IF tempEIP not in code segment limit THEN #GP(0); FI;
CS ← DEST(SegmentSelector); (* segment descriptor information also loaded *)
CS(RPL) ← CPL
EIP ← tempEIP;
JMP—Jump (Continued)

END;

TASK-GATE:
  IF task gate DPL < CPL
    OR task gate DPL < task gate segment-selector RPL
    THEN #GP(task gate selector); FI;
  IF task gate not present THEN #NP(gate selector); FI;
  IF Itanium System Environment THEN IA-32_Intercept(Gate,JMP);
  Read the TSS segment selector in the task-gate descriptor;
  IF TSS segment selector local/global bit is set to local
    OR index not within GDT limits
    OR TSS descriptor specifies that the TSS is busy
    THEN #GP(TSS selector); FI;
  IF TSS not present THEN #NP(TSS selector); FI;
  IF Itanium System Environment THEN IA-32_Intercept(Gate,JMP);
  SWITCH-TASKS to TSS;
  IF EIP not within code segment limit THEN #GP(0); FI;
END;

TASK-STATE-SEGMENT:
  IF TSS DPL < CPL
    OR TSS DPL < TSS segment-selector RPL
    OR TSS descriptor indicates TSS not available
    THEN #GP(TSS selector); FI;
  IF TSS is not present THEN #NP(TSS selector); FI;
  IF Itanium System Environment THEN IA-32_Intercept(Gate,JMP);
  SWITCH-TASKS to TSS;
  IF EIP not within code segment limit THEN #GP(0); FI;
END;

Flags Affected

All flags are affected if a task switch occurs; no flags are affected if a task switch does not occur.

Additional Itanium® System Environment Exceptions

Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
IA-32_Intercept Gate Intercept for JMP through CALL Gates, Task Gates and Task Segments
IA-32_Exception Taken Branch Debug Exception if PSR.tb is 1

Protected Mode Exceptions

#GP(0)  If offset in target operand, call gate, or TSS is beyond the code segment limits.
        If the segment selector in the destination operand, call gate, task gate, or TSS
        is null.
        If a memory operand effective address is outside the CS, DS, ES, FS, or GS
        segment limit.
JMP—Jump (Continued)

If the DS, ES, FS, or GS register is used to access memory and it contains a
null segment selector.

#GP(selector)  If segment selector index is outside descriptor table limits.

If the segment descriptor pointed to by the segment selector in the destination
operand is not for a conforming-code segment, nonconforming-code
segment, call gate, task gate, or task state segment.

If the DPL for a nonconforming-code segment is not equal to the CPL
(When not using a call gate.) If the RPL for the segment’s segment selector is
greater than the CPL.

If the DPL for a conforming-code segment is greater than the CPL.

If the DPL from a call-gate, task-gate, or TSS segment descriptor is less than
the CPL or than the RPL of the call-gate, task-gate, or TSS’s segment selector.

If the segment descriptor for selector in a call gate does not indicate it is a
code segment.

If the segment descriptor for the segment selector in a task gate does not
indicate available TSS.

If the segment selector for a TSS has its local/global bit set for local.

If a TSS segment descriptor specifies that the TSS is busy or not available.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#NP (selector)  If the code segment being accessed is not present.

If call gate, task gate, or TSS not present.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made
while the current privilege level is 3. (Only occurs when fetching target from
memory.)

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.

#SS  If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If the target operand is beyond the code segment limits.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.

#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
(Only occurs when fetching target from memory.)
JMPE—Jump to Intel® Itanium® Instruction Set

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /6</td>
<td>JMPE r/m16</td>
<td>Jump to Intel® Itanium® instruction set, indirect address specified by r/m16</td>
</tr>
<tr>
<td>0F 00 /6</td>
<td>JMPE r/m32</td>
<td>Jump to Intel® Itanium® instruction set, indirect address specified by r/m32</td>
</tr>
<tr>
<td>0F B8</td>
<td>JMPE disp16</td>
<td>Jump to Intel® Itanium® instruction set, absolute address specified by addr16</td>
</tr>
<tr>
<td>0F B8</td>
<td>JMPE disp32</td>
<td>Jump to Intel® Itanium® instruction set, absolute address specified by addr32</td>
</tr>
</tbody>
</table>

**Description**

This instruction is available only on processors based on the Itanium architecture in the Itanium System Environment. Otherwise, execution of this instruction at privilege levels 1, 2, and 3 results in an Illegal Opcode fault, and at privilege level 0, termination of the IA-32 System Environment on a processor based on the Itanium architecture.

JMPE switches the processor to the Itanium instruction set and starts execution at the specified target address. There are two forms; an indirect form, r/m16/32, and an unsigned absolute form, disp16/32. Both 16 and 32-bit formats are supported.

The absolute form computes the 16-byte aligned 64-bit virtual target address in the Itanium instruction set by adding the unsigned 16 or 32-bit displacement to the current CS base \( (IP{31:0} = \text{disp16/32} + \text{CSD.base}) \). The indirect form specifies the virtual target address by the contents of a register or memory location \( (IP{31:0} = [r/m16/32] + \text{CSD.base}) \). Target addresses are constrained to the lower 4G-bytes of the 64-bit virtual address space within virtual region 0.

GR[1] is loaded with the next sequential instruction address following JMPE.

If PSR.di is 1, the instruction is nullified and a Disabled Instruction Set Transition fault is generated. If Itanium branch debugging is enabled, an IA-32_Exception(Debug) trap is taken after JMPE completes execution.

JMPE can be performed at any privilege level and does not change the privilege level of the processor.

JMPE performs a FWAIT operation, any pending IA-32 unmasked floating-point exceptions are reported as faults on the JMPE instruction.

JMPE does not perform a memory fence or serialization operation.

Successful execution of JMPE clears EFLAG.rf and PSR.id to zero.

If the register stack engine is enabled for eager execution, the register stack engine may immediately start loading registers when the processor enters the Itanium instruction set.
JMPE—Jump to Intel® Itanium® Instruction Set (Continued)

Operation

if (NOT Itanium System Environment) {
    if (PSR.cpl==0) Terminate_IA-32_System_Env();
    else IA_32_Exception(IllegalOpcode);
} else if (PSR.di==1) {
    Disabled_Instruction_Set_Transition_Fault();
} else if (pending_numeric_exceptions()) {
    IA_32_exception(FPError);
} else {
    if (absolute_form) { //compute virtual target
        IP{31:0} = disp16/32 + AR[CSD].base;//disp is 16/32-bit unsigned value
    } else if (indirect_form) {
        IP{31:0} = [r/m16/32] + AR[CSD].base;
    }
    PSR.is = 0; //set Itanium Instruction Set bit
    IP{3:0}= 0; //Force 16-byte alignment
    IP{63:32} = 0; //zero extend from 32-bits to 64-bits
    GR[1]{31:0} = EIP + AR[CSD].base; //next sequential instruction address
    GR[1]{63:32} = 0;
    PSR.id = EFLAG.rf = 0;
    if (PSR.tb) //taken branch trap
        IA_32_Exception(Debug);
}

Flags Affected

None (other than EFLAG.rf)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults NaT Register Consumption Fault.
Disabled ISA Disabled Instruction Set Transition Fault, if PSR.di is 1
IA-32_Exception Floating-point Error, if any floating-point exceptions are pending
IA-32_Exception Taken Branch trap, if PSR.tb is 1.

IA-32 System Environment Exceptions (All Operating Modes)

#UD JMPE raises an invalid opcode exception at privilege levels 1, 2 and 3.
Privilege level 0 results in termination of the IA-32 System Environment on a processor based on the Itanium architecture.
LAHF—Load Status Flags into AH Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9F</td>
<td>LAHF</td>
<td>Load: AH = EFLAGS(SF:ZF:0:AF:0:PF:1:CF)</td>
</tr>
</tbody>
</table>

**Description**

Moves the low byte of the EFLAGS register (which includes status flags SF, ZF, AF, PF, and CF) to the AH register. Reserved bits 1, 3, and 5 of the EFLAGS register are set in the AH register as shown in the “Operation” below.

**Operation**

\[
\text{AH} \leftarrow \text{EFLAGS}(\text{SF}:\text{ZF}:0:\text{AF}:0:\text{PF}:1:\text{CF})
\]

**Flags Affected**

None (that is, the state of the flags in the EFLAGS register are not affected).

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults  NaT Register Consumption Abort.

**Exceptions (All Operating Modes)**

None.
LAR—Load Access Rights Byte

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 02 /r</td>
<td>LAR r16,r/m16</td>
<td>r16 ← r/m16 masked by FF00H</td>
</tr>
<tr>
<td>0F 02 /r</td>
<td>LAR r32,r/m32</td>
<td>r32 ← r/m32 masked by 00FxFF00H</td>
</tr>
</tbody>
</table>

Description

Loads the access rights from the segment descriptor specified by the second operand (source operand) into the first operand (destination operand) and sets the ZF flag in the EFLAGS register. The source operand (which can be a register or a memory location) contains the segment selector for the segment descriptor being accessed. The destination operand is a general-purpose register.

The processor performs access checks as part of the loading process. Once loaded in the destination register, software can perform additional checks on the access rights information.

When the operand size is 32 bits, the access rights for a segment descriptor comprise the type and DPL fields and the S, P, AVL, D/B, and G flags, all of which are located in the second doubleword (bytes 4 through 7) of the segment descriptor. The doubleword is masked by 00FxFF00H before it is loaded into the destination operand. When the operand size is 16 bits, the access rights comprise the type and DPL fields. Here, the two lower-order bytes of the doubleword are masked by FF00H before being loaded into the destination operand.

This instruction performs the following checks before it loads the access rights in the destination register:

- Checks that the segment selector is not null.
- Checks that the segment selector points to a descriptor that is within the limits of the GDT or LDT being accessed.
- Checks that the descriptor type is valid for this instruction. All code and data segment descriptors are valid for (can be accessed with) the LAR instruction. The valid system segment and gate descriptor types are given in the following table.
- If the segment is not a conforming code segment, it checks that the specified segment descriptor is visible at the CPL (that is, if the CPL and the RPL of the segment selector are less than or equal to the DPL of the segment selector).

If the segment descriptor cannot be accessed or is an invalid type for the instruction, the ZF flag is cleared and no access rights are loaded in the destination operand.

The LAR instruction can only be executed in protected mode.
LAR—Load Access Rights Byte (Continued)

Table 1-15. LAR Descriptor Validity

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Valid</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>Available 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>LDT</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>Busy 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>16-bit call gate</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>16-bit/32-bit task gate</td>
<td>Yes</td>
</tr>
<tr>
<td>6</td>
<td>16-bit trap gate</td>
<td>No</td>
</tr>
<tr>
<td>7</td>
<td>16-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>9</td>
<td>Available 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>A</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>B</td>
<td>Busy 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>C</td>
<td>32-bit call gate</td>
<td>Yes</td>
</tr>
<tr>
<td>D</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>E</td>
<td>32-bit trap gate</td>
<td>No</td>
</tr>
<tr>
<td>F</td>
<td>32-bit interrupt gate</td>
<td>No</td>
</tr>
</tbody>
</table>

Operation

IF SRC(Offset) > descriptor table limit THEN ZF ← 0; FI;
Read segment descriptor;
IF SegmentDescriptor(Type) ≠ conforming code segment
AND (CPL > DPL) OR (RPL > DPL)
OR Segment type is not valid for instruction
THEN
    ZF ← 0
ELSE
    IF OperandSize = 32
        THEN
            DEST ← [SRC] AND 00FxFF00H;
        ELSE (*OperandSize = 16*)
            DEST ← [SRC] AND FF00H;
        FI;
    FI;

Flags Affected

The ZF flag is set to 1 if the access rights are loaded successfully; otherwise, it is cleared to 0.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
LAR—Load Access Rights Byte (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3. (Only occurs when fetching target from memory.)

Real Address Mode Exceptions

#UD The LAR instruction is not recognized in real address mode.

Virtual 8086 Mode Exceptions

#UD The LAR instruction cannot be executed in virtual 8086 mode.
LDS/LES/LFS/LGS/LSS—Load Far Pointer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C5 i/r</td>
<td>LDS r16,m16:16</td>
<td>Load DS:r16 with far pointer from memory</td>
</tr>
<tr>
<td>C5 i/r</td>
<td>LDS r32,m16:32</td>
<td>Load DS:r32 with far pointer from memory</td>
</tr>
<tr>
<td>0F B2 i/r</td>
<td>LSS r16,m16:16</td>
<td>Load SS:r16 with far pointer from memory</td>
</tr>
<tr>
<td>0F B2 i/r</td>
<td>LSS r32,m16:32</td>
<td>Load SS:r32 with far pointer from memory</td>
</tr>
<tr>
<td>C4 i/r</td>
<td>LES r16,m16:16</td>
<td>Load ES:r16 with far pointer from memory</td>
</tr>
<tr>
<td>C4 i/r</td>
<td>LES r32,m16:32</td>
<td>Load ES:r32 with far pointer from memory</td>
</tr>
<tr>
<td>0F B4 i/r</td>
<td>LFS r16,m16:16</td>
<td>Load FS:r16 with far pointer from memory</td>
</tr>
<tr>
<td>0F B4 i/r</td>
<td>LFS r32,m16:32</td>
<td>Load FS:r32 with far pointer from memory</td>
</tr>
<tr>
<td>0F B5 i/r</td>
<td>LGS r16,m16:16</td>
<td>Load GS:r16 with far pointer from memory</td>
</tr>
<tr>
<td>0F B5 i/r</td>
<td>LGS r32,m16:32</td>
<td>Load GS:r32 with far pointer from memory</td>
</tr>
</tbody>
</table>

Description

Load a far pointer (segment selector and offset) from the second operand (source operand) into a segment register and the first operand (destination operand). The source operand specifies a 48-bit or a 32-bit pointer in memory depending on the current setting of the operand-size attribute (32 bits or 16 bits, respectively). The instruction opcode and the destination operand specify a segment register/general-purpose register pair. The 16-bit segment selector from the source operand is loaded into the segment register implied with the opcode (DS, SS, ES, FS, or GS). The 32-bit or 16-bit offset is loaded into the register specified with the destination operand.

If one of these instructions is executed in protected mode, additional information from the segment descriptor pointed to by the segment selector in the source operand is loaded in the hidden part of the selected segment register.

Also in protected mode, a null selector (values 0000 through 0003) can be loaded into DS, ES, FS, or GS registers without causing a protection exception. (Any subsequent reference to a segment whose corresponding segment register is loaded with a null selector, causes a general-protection exception (#GP) and no memory reference to the segment occurs.)

Operation

IF ProtectedMode
THEN IF SS is loaded
    THEN IF SegmentSelector = null
        THEN #GP(0);
    FI;
ELSE IF Segment selector index is not within descriptor table limits
OR Segment selector RPL ≠ CPL
OR Access rights indicate nonwritable data segment
OR DPL ≠ CPL
    THEN #GP(selector);
FI;
ELSE IF Segment marked not present
    THEN #SS(selector);
FI;
SS ← SegmentSelector(SRC);
SS ← SegmentDescriptor([SRC]);
LDS/LES/LFS/LGS/LSS—Load Far Pointer (Continued)

ELSE IF DS, ES, FS, or GS is loaded with non-null segment selector
THEN IF Segment selector index is not within descriptor table limits
OR Access rights indicate segment neither data nor readable code segment
OR (Segment is data or nonconforming-code segment
   AND both RPL and CPL > DPL)
   THEN #GP(selector);
FI;
ELSE IF Segment marked not present
THEN #NP(selector);
FI;
SegmentRegister ← SegmentSelector(SRC) AND RPL;
SegmentRegister ← SegmentDescriptor([SRC]);
ELSE IF DS, ES, FS or GS is loaded with a null selector:
   SegmentRegister ← NullSelector;
   SegmentRegister(DescriptorValidBit) ← 0; (*hidden flag; not accessible by software*)
FI;
FI;
IF (Real-Address or Virtual 8086 Mode)
THEN
   SS ← SegmentSelector(SRC);
FI;
DEST ← Offset(SRC);

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault,
                    Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault,
                    Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault,
                    Data Dirty Bit Fault

Protected Mode Exceptions

#UD  If source operand is not a memory location.
#GP(0)  If a null selector is loaded into the SS register.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#GP(selector)  If the SS register is being loaded and any of the following is true: the segment selector index is not within the descriptor table limits, the segment selector RPL is not equal to CPL, the segment is a nonwritable data segment, or DPL is not equal to CPL.
LDS/LES/LFS/LGS/LSS—Load Far Pointer (Continued)

If the DS, ES, FS, or GS register is being loaded with a non-null segment selector and any of the following is true: the segment selector index is not within descriptor table limits, the segment is neither a data nor a readable code segment, or the segment is a data or nonconforming-code segment and both RPL and CPL are greater than DPL.

#SS(0) If a memory operand effective address is outside the SS segment limit.
#SS(selector) If the SS register is being loaded and the segment is marked not present.
#NP(selector) If DS, ES, FS, or GS register is being loaded with a non-null segment selector and the segment is marked not present.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If source operand is not a memory location.

Virtual 8086 Mode Exceptions

#UD If source operand is not a memory location.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
LEA—Load Effective Address

### Description

Computes the effective address of the second operand (the source operand) and stores it in the first operand (destination operand). The source operand is a memory address (offset part) specified with one of the processors addressing modes; the destination operand is a general-purpose register. The address-size and operand-size attributes affect the action performed by this instruction, as shown in the following table. The operand-size attribute of the instruction is determined by the chosen register; the address-size attribute is determined by the attribute of the code segment.

#### Table 1-16. LEA Address and Operand Sizes

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Address Size</th>
<th>Action Performed</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>16</td>
<td>16-bit effective address is calculated and stored in requested 16-bit register destination.</td>
</tr>
<tr>
<td>16</td>
<td>32</td>
<td>32-bit effective address is calculated. The lower 16 bits of the address are stored in the requested 16-bit register destination.</td>
</tr>
<tr>
<td>32</td>
<td>16</td>
<td>16-bit effective address is calculated. The 16-bit address is zero-extended and stored in the requested 32-bit register destination.</td>
</tr>
<tr>
<td>32</td>
<td>32</td>
<td>32-bit effective address is calculated and stored in the requested 32-bit register destination.</td>
</tr>
</tbody>
</table>

Different assemblers may use different algorithms based on the size attribute and symbolic reference of the source operand.

#### Operation

```assembly
IF OperandSize = 16 AND AddressSize = 16
THEN
    DEST ← EffectiveAddress(SRC); (* 16-bit address *)
ELSE IF OperandSize = 16 AND AddressSize = 32
THEN
    temp ← EffectiveAddress(SRC); (* 32-bit address *)
    DEST ← temp[0..15]; (* 16-bit address *)
ELSE IF OperandSize = 32 AND AddressSize = 16
THEN
    temp ← EffectiveAddress(SRC); (* 16-bit address *)
    DEST ← ZeroExtend(temp); (* 32-bit address *)
ELSE IF OperandSize = 32 AND AddressSize = 32
THEN
    DEST ← EffectiveAddress(SRC); (* 32-bit address *)
FI;
FI;
```
LEA—Load Effective Address (Continued)

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.

Protected Mode Exceptions

#UD  If source operand is not a memory location.

Real Address Mode Exceptions

#UD  If source operand is not a memory location.

Virtual 8086 Mode Exceptions

#UD  If source operand is not a memory location.
LEAVE—High Level Procedure Exit

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C9</td>
<td>LEAVE</td>
<td>Set SP to BP, then pop BP</td>
</tr>
<tr>
<td>C9</td>
<td>LEAVE</td>
<td>Set ESP to EBP, then pop EBP</td>
</tr>
</tbody>
</table>

**Description**

Executes a return from a procedure or group of nested procedures established by an earlier ENTER instruction. The instruction copies the frame pointer (in the EBP register) into the stack pointer register (ESP), releasing the stack space used by a procedure for its local variables. The old frame pointer (the frame pointer for the calling procedure that issued the ENTER instruction) is then popped from the stack into the EBP register, restoring the calling procedure’s frame.

A RET instruction is commonly executed following a LEAVE instruction to return program control to the calling procedure and remove any arguments pushed onto the stack by the procedure being returned from.

**Operation**

IF StackAddressSize = 32
   THEN
   ESP ← EBP;
ELSE (* StackAddressSize = 16*)
   SP ← BP;
FI;

IF OperandSize = 32
   THEN
   EBP ← Pop();
ELSE (* OperandSize = 16*)
   BP ← Pop();
FI;

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Protected Mode Exceptions**

#SS(0)  If the EBP register points to a location that is not within the limits of the current stack segment.
LEAVE—High Level Procedure Exit (Continued)

Real Address Mode Exceptions

#GP If the EBP register points to a location outside of the effective address space from 0 to 0FFFFH.

Virtual 8086 Mode Exceptions

#GP(0) If the EBP register points to a location outside of the effective address space from 0 to 0FFFFH.
LES—Load Full Pointer

See entry for LDS/LES/LFS/LGS/LSS.
LFS—Load Full Pointer

See entry for LDS/LES/LFS/LGS/LSS.
LGDT/LIDT—Load Global/Interrupt Descriptor Table Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 /2</td>
<td>LGDT m16&amp;32</td>
<td>Load m into GDTR</td>
</tr>
<tr>
<td>0F 01 /3</td>
<td>LIDT m16&amp;32</td>
<td>Load m into IDTR</td>
</tr>
</tbody>
</table>

**Description**

Loads the values in the source operand into the global descriptor table register (GDTR) or the interrupt descriptor table register (IDTR). The source operand is a pointer to 6 bytes of data in memory that contains the base address (a linear address) and the limit (size of table in bytes) of the global descriptor table (GDT) or the interrupt descriptor table (IDT). If operand-size attribute is 32 bits, a 16-bit limit (lower 2 bytes of the 6-byte data operand) and a 32-bit base address (upper 4 bytes of the data operand) are loaded into the register. If the operand-size attribute is 16 bits, a 16-bit limit (lower 2 bytes) and a 24-bit base address (third, fourth, and fifth byte) are loaded. Here, the high-order byte of the operand is not used and the high-order byte of the base address in the GDTR or IDTR is filled with zeros.

The LGDT and LIDT instructions are used only in operating-system software; they are not used in application programs. They are the only instructions that directly load a linear address (that is, not a segment-relative address) and a limit in protected mode. They are commonly executed in real-address mode to allow processor initialization prior to switching to protected mode.

**Operation**

IF Itanium System Environment THEN IA-32_Intercept(INST,LGDT/LIDT);

IF instruction is LIDT THEN

IF OperandSize = 16 THEN

IDTR(Limit) ← SRC[0:15];
IDTR(Base) ← SRC[16:47] AND 00FFFFFFH;
ELSE (* 32-bit Operand Size *)
IDTR(Limit) ← SRC[0:15];
IDTR(Base) ← SRC[16:47];
FI;
ELSE (* instruction is LGDT *)
IF OperandSize = 16 THEN

GDTR(Limit) ← SRC[0:15];
GDTR(Base) ← SRC[16:47] AND 00FFFFFFH;
ELSE (* 32-bit Operand Size *)
GDTR(Limit) ← SRC[0:15];
GDTR(Base) ← SRC[16:47];
FI;
FI;

**Flags Affected**

None.
Additional Itanium® System Environment Exceptions
IA-32 Intercept Mandatory Instruction Intercept for LIDT and LGDT

Protected Mode Exceptions
#UD If source operand is not a memory location.
#GP(0) If the current privilege level is not 0.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.

Real Address Mode Exceptions
#UD If source operand is not a memory location.
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions
#UD If source operand is not a memory location.
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
LGS—Load Full Pointer

See entry for LDS/LES/LFS/LGS/LSS.
LLDT—Load Local Descriptor Table Register

**Opcode**  
<table>
<thead>
<tr>
<th>0F 00 /2</th>
<th>LLDT r/m16</th>
</tr>
</thead>
</table>

**Description**

Loads the source operand into the segment selector field of the local descriptor table register (LDTR). The source operand (a general-purpose register or a memory location) contains a segment selector that points to a local descriptor table (LDT). After the segment selector is loaded in the LDTR, the processor uses to segment selector to locate the segment descriptor for the LDT in the global descriptor table (GDT). It then loads the segment limit and base address for the LDT from the segment descriptor into the LDTR. The segment registers DS, ES, SS, FS, GS, and CS are not affected by this instruction, nor is the LDTR field in the task state segment (TSS) for the current task.

If the source operand is 0, the LDTR is marked invalid and all references to descriptors in the LDT (except by the LAR, VERR, VERW or LSL instructions) cause a general protection exception (#GP).

The operand-size attribute has no effect on this instruction.

The LLDT instruction is provided for use in operating-system software; it should not be used in application programs. Also, this instruction can only be executed in protected mode.

**Operation**

**If Itanium System Environment Then IA-32_Intercept(INST, LLDT);**

**IF SRC(Offset) > descriptor table limit THEN #GP(segment selector); FI;**

Read segment descriptor;

**IF SegmentDescriptor(Type) ≠ LDT THEN #GP(segment selector); FI;**

**IF segment descriptor is not present THEN #NP(segment selector);**

LDTR(SegmentSelector) ← SRC;

LDTR(SegmentDescriptor) ← GDTSegmentDescriptor;

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

IA-32_Intercept Instruction Intercept

**Protected Mode Exceptions**

#GP(0)  
If the current privilege level is not 0.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register contains a null segment selector.
LLDT—Load Local Descriptor Table Register (Continued)

#GP(selector) If the selector operand does not point into the Global Descriptor Table or if the entry in the GDT is not a Local Descriptor Table.
   Segment selector is beyond GDT limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#NP(selector) If the LDT descriptor is not present.
#PF(fault-code) If a page fault occurs.

Real Address Mode Exceptions

#UD The LLDT instruction is not recognized in real address mode.

Virtual 8086 Mode Exceptions

#UD The LLDT instruction is recognized in virtual 8086 mode.
LIDT—Load Interrupt Descriptor Table Register

See entry for LGDT/LIDT—Load Global Descriptor Table Register/Load Interrupt Descriptor Table Register.
LMSW—Load Machine Status Word

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 /6</td>
<td>LMSW r/m16</td>
<td>Loads r/m16 in machine status word of CR0</td>
</tr>
</tbody>
</table>

**Description**

Loads the source operand into the machine status word, bits 0 through 15 of register CR0. The source operand can be a 16-bit general-purpose register or a memory location. Only the low-order 4 bits of the source operand (which contains the PE, MP, EM, and TS flags) are loaded into CR0. The PG, CD, NW, AM, WP, NE, and ET flags of CR0 are not affected. The operand-size attribute has no effect on this instruction.

If the PE flag of the source operand (bit 0) is set to 1, the instruction causes the processor to switch to protected mode. The PE flag in the CR0 register is a sticky bit. Once set to 1, the LMSW instruction cannot be used clear this flag and force a switch back to real address mode.

The LMSW instruction is provided for use in operating-system software; it should not be used in application programs. In protected or virtual 8086 mode, it can only be executed at CPL 0.

This instruction is provided for compatibility with the Intel 286 processor; programs and procedures intended to run on processors more recent than the Intel 286 should use the MOV (control registers) instruction to load the machine status word.

This instruction is a serializing instruction.

**Operation**

IF Itanium System Environment THEN IA-32_Intercept(INST,LMSW);
CR0[0:3] ← SRC[0:3];

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

IA-32_Intercept  Mandatory Instruction Intercept

**Protected Mode Exceptions**

#GP(0)  If the current privilege level is not 0.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.
LMSW—Load Machine Status Word (Continued)

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If the current privilege level is not 0.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#PF(fault-code)  If a page fault occurs.
LOCK—Assert LOCK# Signal Prefix

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F0</td>
<td>LOCK</td>
<td>Asserts LOCK# signal for duration of the accompanying instruction</td>
</tr>
</tbody>
</table>

**Description**

Causes the processor’s LOCK# signal to be asserted during execution of the accompanying instruction (turns the instruction into an atomic instruction). In a multiprocessor environment, the LOCK# signal insures that the processor has exclusive use of any shared memory while the signal is asserted.

The LOCK prefix can be prepended only to the following instructions and to those forms of the instructions that use a memory operand: ADD, ADC, AND, BTC, BTR, BTS, CMPXCHG, DEC, INC, NEG, NOT, OR, SBB, SUB, XOR, XADD, and XCHG. An undefined opcode exception will be generated if the LOCK prefix is used with any other instruction. The XCHG instruction always asserts the LOCK# signal regardless of the presence or absence of the LOCK prefix.

The LOCK prefix is typically used with the BTS instruction to perform a read-modify-write operation on a memory location in shared memory environment.

The integrity of the LOCK prefix is not affected by the alignment of the memory field. Memory locking is observed for arbitrarily misaligned fields.

**Operation**

\[
\text{IF Itanium System Environment AND External Bus Lock Required AND DCR.lc} \\
\text{THEN IA-32 Intercept(LOCK);} \\
\text{AssertLOCK#(DurationOfAccompanyingInstruction)}
\]

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
- **IA-32_Intercept**: Lock Intercept - If an external atomic bus lock is required to complete this operation and DCR.lc is 1, no atomic transaction occurs, the instruction is faulted and an IA-32_Intercept(Lock) fault is generated. The software lock handler is responsible for the emulation of the instruction.

**Protected Mode Exceptions**

- **#UD**: If the LOCK prefix is used with an instruction not listed in the “Description” section above. Other exceptions can be generated by the instruction that the LOCK prefix is being applied to.
LOCK—Assert LOCK# Signal Prefix (Continued)

**Real Address Mode Exceptions**

#UD If the LOCK prefix is used with an instruction not listed in the “Description” section above. Other exceptions can be generated by the instruction that the LOCK prefix is being applied to.

**Virtual 8086 Mode Exceptions**

#UD If the LOCK prefix is used with an instruction not listed in the “Description” section above. Other exceptions can be generated by the instruction that the LOCK prefix is being applied to.
LODS/LODSB/LODSW/LODSD—Load String Operand

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC</td>
<td>LODS DS:(E)SI</td>
<td>Load byte at address DS:(E)SI into AL</td>
</tr>
<tr>
<td>AD</td>
<td>LODS DS:SI</td>
<td>Load word at address DS:SI into AX</td>
</tr>
<tr>
<td>AD</td>
<td>LODS DS:ESI</td>
<td>Load doubleword at address DS:ESI into EAX</td>
</tr>
<tr>
<td>AC</td>
<td>LODSB</td>
<td>Load byte at address DS:(E)SI into AL</td>
</tr>
<tr>
<td>AD</td>
<td>LODSW</td>
<td>Load word at address DS:SI into AX</td>
</tr>
<tr>
<td>AD</td>
<td>LODSD</td>
<td>Load doubleword at address DS:ESI into EAX</td>
</tr>
</tbody>
</table>

**Description**

Load a byte, word, or doubleword from the source operand into the AL, AX, or EAX register, respectively. The source operand is a memory location at the address DS:ESI. (When the operand-size attribute is 16, the SI register is used as the source-index register.) The DS segment may be overridden with a segment override prefix.

The LODSB, LODSW, and LODSD mnemonics are synonyms of the byte, word, and doubleword versions of the LODS instructions. (For the LODS instruction, “DS:ESI” must be explicitly specified in the instruction.)

After the byte, word, or doubleword is transfer from the memory location into the AL, AX, or EAX register, the ESI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the ESI register is incremented; if the DF flag is 1, the ESI register is decremented.) The ESI register is incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The LODS, LODSB, LODSW, and LODSD instructions can be preceded by the REP prefix for block loads of ECX bytes, words, or doublewords. More often, however, these instructions are used within a LOOP construct, because further processing of the data moved into the register is usually necessary before the next transfer can be made. See “REP/REPE/REPZ/REPNE/REPNZ—Repeat String Operation Prefix” on page 3:685 for a description of the REP prefix.

**Operation**

IF (byte load) 
THEN
   AL ← SRC; (* byte load *) 
   THEN IF DF = 0 
      THEN (E)SI ← 1; 
      ELSE (E)SI ← −1; 
   Fi; 
ELSE IF (word load) 
THEN 
   AX ← SRC; (* word load *) 
   THEN IF DF = 0 
      THEN SI ← 2; 
      ELSE SI ← −2; 
   Fi; 
ELSE (* doubleword transfer *) 
   EAX ← SRC; (* doubleword load *) 
   THEN IF DF = 0
LODS/LODSB/LODSW/LODSD—Load String Operand (Continued)

THEN ESI ← 4;
ELSE ESI ← –4;
FI;
FI;
FI;
FI;

Flags Affected
None.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>Itanium Mem Faults</th>
</tr>
</thead>
<tbody>
<tr>
<td>NaT Register Consumption Abort.</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.  
If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
LOOP/LOOPcc—Loop According to ECX Counter

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E2 cb</td>
<td>LOOP rel8</td>
<td>Decrement count; jump short if count ≠ 0</td>
</tr>
<tr>
<td>E1 cb</td>
<td>LOOPE rel8</td>
<td>Decrement count; jump short if count ≠ 0 and ZF=1</td>
</tr>
<tr>
<td>E1 cb</td>
<td>LOOPZ rel8</td>
<td>Decrement count; jump short if count ≠ 0 and ZF=1</td>
</tr>
<tr>
<td>E0 cb</td>
<td>LOOPNE rel8</td>
<td>Decrement count; jump short if count ≠ 0 and ZF=0</td>
</tr>
<tr>
<td>E0 cb</td>
<td>LOOPNZ rel8</td>
<td>Decrement count; jump short if count ≠ 0 and ZF=0</td>
</tr>
</tbody>
</table>

**Description**

Performs a loop operation using the ECX or CX register as a counter. Each time the LOOP instruction is executed, the count register is decremented, then checked for 0. If the count is 0, the loop is terminated and program execution continues with the instruction following the LOOP instruction. If the count is not zero, a near jump is performed to the destination (target) operand, which is presumably the instruction at the beginning of the loop. If the address-size attribute is 32 bits, the ECX register is used as the count register; otherwise the CX register is used.

The target instruction is specified with a relative offset (a signed offset relative to the current value of the instruction pointer in the EIP register). This offset is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed, 8-bit immediate value, which is added to the instruction pointer. Offsets of −128 to +127 are allowed with this instruction.

Some forms of the loop instruction (LOOPcc) also accept the ZF flag as a condition for terminating the loop before the count reaches zero. With these forms of the instruction, a condition code (cc) is associated with each instruction to indicate the condition being tested for. Here, the LOOPcc instruction itself does not affect the state of the ZF flag; the ZF flag is changed by other instructions in the loop.

All branches are converted to code fetches of one or two cache lines, regardless of jump address or cacheability.

**Operation**

IF AddressSize = 32
THEN
  Count is ECX;
ELSE (* AddressSize = 16 *)
  Count is CX;
FI;
Count ← Count – 1;

IF instruction in not LOOP
THEN
  IF (instruction = LOOPE) OR (instruction = LOOPZ)
  THEN
    IF (ZF =1) AND (Count ≠ 0)
     THEN BranchCond ← 1;
     ELSE BranchCond ← 0;
    FI;
  FI;
  IF (instruction = LOOPNE) OR (instruction = LOOPNZ)
LOOP/LOOPcc—Loop According to ECX Counter (Continued)

THEN
  IF (ZF = 0) AND (Count ≠ 0)
    THEN BranchCond ← 1;
    ELSE BranchCond ← 0;
  FI;
FI;
ELSE (* instruction = LOOP *)
  IF (Count ≠ 0)
    THEN BranchCond ← 1;
    ELSE BranchCond ← 0;
  FI;
FI;
IF BranchCond = 1
  THEN
    EIP ← EIP + SignExtend(DEST);
    IF OperandSize = 16
      THEN
        EIP ← EIP AND 0000FFFFH;
      FI;
    IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);
    ELSE
      Terminate loop and continue program execution at EIP;
    FI;
FI;

Flags Affected
None.

Additional Itanium® System Environment Exceptions
Itanium Reg Faults NaT Register Consumption Abort.
IA-32_Exception Taken Branch Debug Exception if PSR.tb is 1

Protected Mode Exceptions
#GP(0) If the offset jumped to is beyond the limits of the code segment.

Real Address Mode Exceptions
None.

Virtual 8086 Mode Exceptions
None.
LSL—Load Segment Limit

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 03 /r</td>
<td>LSL r16,r/m16</td>
<td>Load: r16 ← segment limit, selector r/m16</td>
</tr>
<tr>
<td>0F 03 /r</td>
<td>LSL r32,r/m32</td>
<td>Load: r32 ← segment limit, selector r/m32</td>
</tr>
</tbody>
</table>

Description

Loads the unscrambled segment limit from the segment descriptor specified with the second operand (source operand) into the first operand (destination operand) and sets the ZF flag in the EFLAGS register. The source operand (which can be a register or a memory location) contains the segment selector for the segment descriptor being accessed. The destination operand is a general-purpose register.

The processor performs access checks as part of the loading process. Once loaded in the destination register, software can compare the segment limit with the offset of a pointer.

The segment limit is a 20-bit value contained in bytes 0 and 1 and in the first 4 bits of byte 6 of the segment descriptor. If the descriptor has a byte granular segment limit (the granularity flag is set to 0), the destination operand is loaded with a byte granular value (byte limit). If the descriptor has a page granular segment limit (the granularity flag is set to 1), the LSL instruction will translate the page granular limit (page limit) into a byte limit before loading it into the destination operand. The translation is performed by shifting the 20-bit “raw” limit left 12 bits and filling the low-order 12 bits with 1s.

When the operand size is 32 bits, the 32-bit byte limit is stored in the destination operand. When the operand size is 16 bits, a valid 32-bit limit is computed; however, the upper 16 bits are truncated and only the low-order 16 bits are loaded into the destination operand.

This instruction performs the following checks before it loads the segment limit into the destination register:

- Checks that the segment selector is not null.
- Checks that the segment selector points to a descriptor that is within the limits of the GDT or LDT being accessed.
- Checks that the descriptor type is valid for this instruction. All code and data segment descriptors are valid for (can be accessed with) the LSL instruction. The valid special segment and gate descriptor types are given in the following table.
- If the segment is not a conforming code segment, the instruction checks that the specified segment descriptor is visible at the CPL (that is, if the CPL and the RPL of the segment selector are less than or equal to the DPL of the segment selector).

If the segment descriptor cannot be accessed or is an invalid type for the instruction, the ZF flag is cleared and no value is loaded in the destination operand.
**LSL—Load Segment Limit (Continued)**

<table>
<thead>
<tr>
<th>Type</th>
<th>Name</th>
<th>Valid</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>1</td>
<td>Available 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>LDT</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>Busy 16-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>16-bit call gate</td>
<td>No</td>
</tr>
<tr>
<td>5</td>
<td>16-bit/32-bit task gate</td>
<td>No</td>
</tr>
<tr>
<td>6</td>
<td>16-bit trap gate</td>
<td>No</td>
</tr>
<tr>
<td>7</td>
<td>16-bit interrupt gate</td>
<td>No</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>9</td>
<td>Available 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>A</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>B</td>
<td>Busy 32-bit TSS</td>
<td>Yes</td>
</tr>
<tr>
<td>C</td>
<td>32-bit call gate</td>
<td>No</td>
</tr>
<tr>
<td>D</td>
<td>Reserved</td>
<td>No</td>
</tr>
<tr>
<td>E</td>
<td>32-bit trap gate</td>
<td>No</td>
</tr>
<tr>
<td>F</td>
<td>32-bit interrupt gate</td>
<td>No</td>
</tr>
</tbody>
</table>

**Operation**

IF SRC(Offset) > descriptor table limit
  THEN ZF ← 0; FI;
Read segment descriptor;
IF SegmentDescriptor(Type) ≠ conforming code segment
  AND (CPL > DPL) OR (RPL > DPL)
  OR Segment type is not valid for instruction
  THEN
    ZF ← 0
ELSE
  temp ← SegmentLimit([SRC]);
  IF (G = 1)
    THEN
      temp ← ShiftLeft(12, temp) OR 00000FFFH;
    FI;
  IF OperandSize = 32
    THEN
      DEST ← temp;
    ELSE (*OperandSize = 16*)
      DEST ← temp AND FFFFH;
  FI;
FI;

**Flags Affected**

The ZF flag is set to 1 if the segment limit is loaded successfully; otherwise, it is cleared to 0.
LSL—Load Segment Limit (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
          If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#UD  The LSL instruction is not recognized in real address mode.

Virtual 8086 Mode Exceptions

#UD  The LSL instruction is not recognized in virtual 8086 mode.
LSS—Load Full Pointer

See entry for LDS/LES/LFS/LGS/LSS.
LTR—Load Task Register

**Description**

Loads the source operand into the segment selector field of the task register. The source operand (a general-purpose register or a memory location) contains a segment selector that points to a task state segment (TSS). After the segment selector is loaded in the task register, the processor uses to segment selector to locate the segment descriptor for the TSS in the global descriptor table (GDT). It then loads the segment limit and base address for the TSS from the segment descriptor into the task register. The task pointed to by the task register is marked busy, but a switch to the task does not occur.

The LTR instruction is provided for use in operating-system software; it should not be used in application programs. It can only be executed in protected mode when the CPL is 0. It is commonly used in initialization code to establish the first task to be executed.

The operand-size attribute has no effect on this instruction.

**Operation**

\[
\text{IF Itanium System Environment THEN IA-32\_Intercept(INST, LTR);} \\
\text{IF SRC(Offset) > descriptor table limit OR IF SRC(type) \neq \text{global}} \\
\text{THEN \#GP(segment selector);} \\
\text{FI;} \\
\text{Reat segment descriptor;} \\
\text{IF segment descriptor is not for an available TSS THEN \#GP(segment selector); FI;} \\
\text{IF segment descriptor is not present THEN \#NP(segment selector);} \\
\text{TSSSegmentDescriptor(busy) \leftarrow 1;} \\
\text{(* Locked read-modify-write operation on the entire descriptor when setting busy flag *)} \\
\text{TaskRegister(SegmentSelector) \leftarrow SRC;} \\
\text{TaskRegister(SegmentDescriptor) \leftarrow TSSSegmentDescriptor;} \\
\]

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

IA-32\_Intercept Mandatory Instruction Intercept.

**Protected Mode Exceptions**

\#GP(0) If the current privilege level is not 0.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
LTR—Load Task Register (Continued)

- **#GP(selector)** If the source selector points to a segment that is not a TSS or to one for a task that is already busy.
  - If the selector points to LDT or is beyond the GDT limit.
- **#NP(selector)** If the TSS is marked not present.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.

**Real Address Mode Exceptions**

- **#UD** The LTR instruction is not recognized in real address mode.

**Virtual 8086 Mode Exceptions**

- **#UD** The LTR instruction is not recognized in virtual 8086 mode.
MOV—Move

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>88 /  r</td>
<td>MOV r/m8,r8</td>
<td>Move r8 to r/m8</td>
</tr>
<tr>
<td>89 /  r</td>
<td>MOV r/m16,r16</td>
<td>Move r16 to r/m16</td>
</tr>
<tr>
<td>89 /  r</td>
<td>MOV r/m32,r32</td>
<td>Move r32 to r/m32</td>
</tr>
<tr>
<td>8A /  r</td>
<td>MOV r8,r/m8</td>
<td>Move r/m8 to r8</td>
</tr>
<tr>
<td>8B /  r</td>
<td>MOV r16,r/m16</td>
<td>Move r/m16 to r16</td>
</tr>
<tr>
<td>8B /  r</td>
<td>MOV r32,r/m32</td>
<td>Move r/m32 to r32</td>
</tr>
<tr>
<td>8C /  r</td>
<td>MOV r/m16,Sreg**</td>
<td>Move segment register to r/m16</td>
</tr>
<tr>
<td>8E /  r</td>
<td>MOV Sreg,r/m16</td>
<td>Move r/m16 to segment register</td>
</tr>
<tr>
<td>A0</td>
<td>MOV AL,moffs8*</td>
<td>Move byte at (seg:offset) to AL</td>
</tr>
<tr>
<td>A1</td>
<td>MOV AX,moffs16*</td>
<td>Move word at (seg:offset) to AX</td>
</tr>
<tr>
<td>A1</td>
<td>MOV EAX,moffs32*</td>
<td>Move doubleword at (seg:offset) to EAX</td>
</tr>
<tr>
<td>A2</td>
<td>MOV moffs8*,AL</td>
<td>Move AL to (seg:offset)</td>
</tr>
<tr>
<td>A3</td>
<td>MOV moffs16*,AX</td>
<td>Move AX to (seg:offset)</td>
</tr>
<tr>
<td>A3</td>
<td>MOV moffs32*,EAX</td>
<td>Move EAX to (seg:offset)</td>
</tr>
<tr>
<td>B0+ rb</td>
<td>MOV r8,imm8</td>
<td>Move imm8 to r8</td>
</tr>
<tr>
<td>B8+ rw</td>
<td>MOV r16,imm16</td>
<td>Move imm16 to r16</td>
</tr>
<tr>
<td>B8+ rd</td>
<td>MOV r32,imm32</td>
<td>Move imm32 to r32</td>
</tr>
<tr>
<td>C6 /  0</td>
<td>MOV r/m8,imm8</td>
<td>Move imm8 to r/m8</td>
</tr>
<tr>
<td>C7 /  0</td>
<td>MOV r/m16,imm16</td>
<td>Move imm16 to r/m16</td>
</tr>
<tr>
<td>C7 /  0</td>
<td>MOV r/m32,imm32</td>
<td>Move imm32 to r/m32</td>
</tr>
</tbody>
</table>

Notes:
* The moffs8, moffs16, and moffs32 operands specify a simple offset relative to the segment base, where 8, 16, and 32 refer to the size of the data. The address-size attribute of the instruction determines the size of the offset, either 16 or 32 bits.
** In 32-bit mode, the assembler may require the use of the 16-bit operand size prefix (a byte with the value 66H preceding the instruction).

Description

Copies the second operand (source operand) to the first operand (destination operand). The source operand can be an immediate value, general-purpose register, segment register, or memory location; the destination register can be a general-purpose register, segment register, or memory location. Both operands must be the same size, which can be a byte, a word, or a doubleword.

The MOV instruction cannot be used to load the CS register. Attempting to do so results in an invalid opcode exception (#UD). To load the CS register, use the RET instruction.
MOV—Move (Continued)

If the destination operand is a segment register (DS, ES, FS, GS, or SS), the source operand must be a valid segment selector. In protected mode, moving a segment selector into a segment register automatically causes the segment descriptor information associated with that segment selector to be loaded into the hidden (shadow) part of the segment register. While loading this information, the segment selector and segment descriptor information is validated (see the “Operation” algorithm below). The segment descriptor data is obtained from the GDT or LDT entry for the specified segment selector.

A null segment selector (values 0000-0003) can be loaded into the DS, ES, FS, and GS registers without causing a protection exception. However, any subsequent attempt to reference a segment whose corresponding segment register is loaded with a null value causes a general protection exception (#GP) and no memory reference occurs.

Loading the SS register with a MOV instruction inhibits all external interrupts and traps until after the execution of the next instruction in the IA-32 System Environment. For the Itanium System Environment, MOV to SS results in a IA-32_Intercept(SystemFlag) trap after the instruction completes. This operation allows a stack pointer to be loaded into the ESP register with the next instruction (MOV ESP, stack-pointer value) before an interrupt occurs. The LSS instruction offers a more efficient method of loading the SS and ESP registers.

When moving data in 32-bit mode between a segment register and a 32-bit general-purpose register, the Pentium Pro processor does not require the use of a 16-bit operand size prefix; however, some assemblers do require this prefix. The processor assumes that the sixteen least-significant bits of the general-purpose register are the destination or source operand. When moving a value from a segment selector to a 32-bit register, the processor fills the two high-order bytes of the register with zeros.

Operation
DEST ← SRC;

Loading a segment register while in protected mode results in special checks and actions, as described in the following listing. These checks are performed on the segment selector and the segment descriptor it points to.

IF SS is loaded;
THEN
  IF segment selector is null
    THEN #GP(0);
  FI;
  IF segment selector index is outside descriptor table limits
    OR segment selector's RPL ≠ CPL
    OR segment is not a writable data segment
    OR DPL ≠ CPL
    THEN #GP(selector);
  FI;
  IF segment not marked present
    THEN #SS(selector);
ELSE
  SS ← segment selector;
  SS ← segment descriptor;
FI;
MOV—Move (Continued)

FI;
IF DS, ES, FS or GS is loaded with non-null selector;

THEN
  IF segment selector index is outside descriptor table limits
    OR segment is not a data or readable code segment
    OR ((segment is a data or nonconforming code segment)
        AND (both RPL and CPL > DPL))
    THEN #GP(selector);
  IF segment not marked present
    THEN #NP(selector);
  ELSE
    SegmentRegister ← segment selector;
    SegmentRegister ← segment descriptor;
  FI;
FI;
IF DS, ES, FS or GS is loaded with a null selector;
THEN
  SegmentRegister ← null segment selector;
  SegmentRegister ← null segment descriptor;
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

IA-32_Interceptor System Flag Intercept trap for Move to SS
Itanium Reg Faults NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB
Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data
Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data
Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If attempt is made to load SS register with null segment selector.
If the destination operand is in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#GP(selector) If segment selector index is outside descriptor table limits.
If the SS register is being loaded and the segment selector’s RPL and the
segment descriptor’s DPL are not equal to the CPL.
If the SS register is being loaded and the segment pointed to is a nonwritable
data segment.
If the DS, ES, FS, or GS register is being loaded and the segment pointed to
is not a data or readable code segment.
MOV—Move (Continued)

If the DS, ES, FS, or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.

#SS(0) If a memory operand effective address is outside the SS segment limit.
#SS(selector) If the SS register is being loaded and the segment pointed to is marked not present.
#NP If the DS, ES, FS, or GS register is being loaded and the segment pointed to is marked not present.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
#UD If attempt is made to load the CS register.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
#UD If attempt is made to load the CS register.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
#UD If attempt is made to load the CS register.
MOV—Move to/from Control Registers

Description

Moves the contents of a control register (CR0, CR2, CR3, or CR4) to a general-purpose register or vice versa. The operand size for these instructions is always 32 bits, regardless of the operand-size attribute. (See the IA-32 Intel® Architecture Software Developer’s Manual, Volume 3 for a detailed description of the flags and fields in the control registers.)

When loading a control register, a program should not attempt to change any of the reserved bits; that is, always set reserved bits to the value previously read.

At the opcode level, the reg field within the ModR/M byte specifies which of the control registers is loaded or read. The 2 bits in the mod field are always 11B. The r/m field specifies the general-purpose register loaded or read.

These instructions have the following side effects:

- When writing to control register CR3, all non-global TLB entries are flushed (see the IA-32 Intel® Architecture Software Developer’s Manual, Volume 3).
- When modifying any of the paging flags in the control registers (PE and PG in register CR0 and PGE, PSE, and PAE in register CR4), all TLB entries are flushed, including global entries. This operation is implementation specific for the Pentium Pro processor. Software should not depend on this functionality in future Intel architecture processors.
- If the PG flag is set to 1 and control register CR4 is written to set the PAE flag to 1 (to enable the physical address extension mode), the pointers (PDPTRs) in the page-directory pointers table will be loaded into the processor (into internal, non-architectural registers).
- If the PAE flag is set to 1 and the PG flag set to 1, writing to control register CR3 will cause the PDPTRs to be reloaded into the processor.
- If the PAE flag is set to 1 and control register CR0 is written to set the PG flag, the PDPTRs are reloaded into the processor.

Operation

IF Itanium System Environment AND Move To CR Form THEN IA-32_Intercept(INST,MOVCR);
DEST ← SRC;

Flags Affected

The OF, SF, ZF, AF, PF, and CF flags are undefined.
MOV—Move to/from Control Registers (Continued)

Additional Itanium® System Environment Exceptions

IA-32_Interceptor Move To CR#, Mandatory Instruction Intercept.

Move From CR#, read the virtualized control register values, CR0{15:6} return zeros.

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0.

If an attempt is made to write a 1 to any reserved bit in CR4.

If an attempt is made to write reserved bits in the page-directory pointers table (used in the extended physical addressing mode) when the PAE flag in control register CR4 and the PG flag in control register CR0 are set to 1.

Real Address Mode Exceptions

#GP If an attempt is made to write a 1 to any reserved bit in CR4.

Virtual 8086 Mode Exceptions

#GP(0) These instructions cannot be executed in virtual 8086 mode.
MOV—Move to/from Debug Registers

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 21/r</td>
<td>MOV r32, DR0-DR3</td>
<td>Move debug registers to r32</td>
</tr>
<tr>
<td>0F 21/r</td>
<td>MOV r32, DR4-DR5</td>
<td>Move debug registers to r32</td>
</tr>
<tr>
<td>0F 21/r</td>
<td>MOV r32, DR6-DR7</td>
<td>Move debug registers to r32</td>
</tr>
<tr>
<td>0F 23/r</td>
<td>MOV DR0-DR3, r32</td>
<td>Move r32 to debug registers</td>
</tr>
<tr>
<td>0F 23/r</td>
<td>MOV DR4-DR5, r32</td>
<td>Move r32 to debug registers</td>
</tr>
<tr>
<td>0F 23/r</td>
<td>MOV DR6-DR7, r32</td>
<td>Move r32 to debug registers</td>
</tr>
</tbody>
</table>

Description

Moves the contents of two or more debug registers (DR0 through DR3, DR4 and DR5, or DR6 and DR7) to a general-purpose register or vice versa. The operand size for these instructions is always 32 bits, regardless of the operand-size attribute. (See the *IA-32 Intel® Architecture Software Developer’s Manual, Volume 3* for a detailed description of the flags and fields in the debug registers.)

The instructions must be executed at privilege level 0 or in real-address mode.

When the debug extension (DE) flag in register CR4 is clear, these instructions operate on debug registers in a manner that is compatible with Intel386™ and Intel486 processors. In this mode, references to DR4 and DR5 refer to DR6 and DR7, respectively. When the DE set in CR4 is set, attempts to reference DR4 and DR5 result in an undefined opcode (#UD) exception.

At the opcode level, the *reg* field within the ModR/M byte specifies which of the debug registers is loaded or read. The two bits in the *mod* field are always 11. The *r/m* field specifies the general-purpose register loaded or read.

Operation

```plaintext
IF Itanium System Environment THEN IA-32_Intercept(INST,MOVDR);
IF ((DE = 1) and (SRC or DEST = DR4 or DR5))
THEN #UD;
ELSE
  DEST ← SRC;
```

Flags Affected

The OF, SF, ZF, AF, PF, and CF flags are undefined.

Additional Itanium® System Environment Exceptions

IA-32_Intercept  Mandatory Instruction Intercept.

Protected Mode Exceptions

- **#GP(0)**  If the current privilege level is not 0.
- **#UD**     If the DE (debug extensions) bit of CR4 is set and a MOV instruction is executed involving DR4 or DR5.
MOV—Move to/from Debug Registers (Continued)

#DB If any debug register is accessed while the GD flag in debug register DR7 is set.

Real Address Mode Exceptions

#UD If the DE (debug extensions) bit of CR4 is set and a MOV instruction is executed involving DR4 or DR5.

#DB If any debug register is accessed while the GD flag in debug register DR7 is set.

Virtual 8086 Mode Exceptions

#GP(0) The debug registers cannot be loaded or read when in virtual 8086 mode.
MOVS/MOVSB/MOVSW/MOVSD—Move Data from String to String

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A4</td>
<td>MOVS ES:(E)DI, DS:(E)SI</td>
<td>Move byte at address DS:(E)SI to address ES:(E)DI</td>
</tr>
<tr>
<td>A5</td>
<td>MOVS ES:DI, DS:SI</td>
<td>Move word at address DS:SI to address ES:DI</td>
</tr>
<tr>
<td>A5</td>
<td>MOVS EDI, DS:ESI</td>
<td>Move doubleword at address DS:ESI to address ES:EDI</td>
</tr>
<tr>
<td>A4</td>
<td>MOVSB</td>
<td>Move byte at address DS:(E)SI to address ES:(E)DI</td>
</tr>
<tr>
<td>A5</td>
<td>MOVSW</td>
<td>Move word at address DS:SI to address ES:DI</td>
</tr>
<tr>
<td>A5</td>
<td>MOVSD</td>
<td>Move doubleword at address DS:ESI to address ES:EDI</td>
</tr>
</tbody>
</table>

Description

Moves the byte, word, or doubleword specified with the second operand (source operand) to the location specified with the first operand (destination operand). The source operand specifies the memory location at the address DS:ESI and the destination operand specifies the memory location at address ES:EDI. (When the operand-size attribute is 16, the SI and DI register are used as the source-index and destination-index registers, respectively.) The DS segment may be overridden with a segment override prefix, but the ES segment cannot be overridden.

The MOVSB, MOVSW, and MOVSD mnemonics are synonyms of the byte, word, and doubleword versions of the MOVS instructions. They are simpler to use, but provide no type or segment checking. (For the MOVS instruction, “DS:ESI” and “ES:EDI” must be explicitly specified in the instruction.)

After the transfer, the ESI and EDI registers are incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the ESI and EDI register are incremented; if the DF flag is 1, the ESI and EDI registers are decremented.) The registers are incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The MOVS, MOVSB, MOVSW, and MOVSD instructions can be preceded by the REP prefix (see “REP/REPE/REPZ/REPNE/REPNZ—Repeat Following String Operation” on “REP/REPE/REPZ/REPNE/REPNZ—Repeat String Operation Prefix” on page 3:685) for block moves of ECX bytes, words, or doublewords.

Operation

DEST ← SRC;
IF (byte move)
  THEN IF DF = 0
    THEN (E)DI ← 1;
    ELSE (E)DI ← −1;
  FI;
ELSE IF (word move)
  THEN IF DF = 0
    THEN DI ← 2;
    ELSE DI ← −2;

MOVS/MOVSB/MOVSW/MOVSD—Move Data from String to String
(Continued)

FI;
ELSE (* doubleword move*)
    THEN IF DF = 0
        THEN EDI ← 4;
        ELSE EDI ← -4;
    FI;
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If the destination is located in a nonwritable segment.
    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
    If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
MOVSX—Move with Sign-Extension

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F BE /r</td>
<td>MOVSX r16,rm8</td>
<td>Move byte to word with sign-extension</td>
</tr>
<tr>
<td>0F BE /r</td>
<td>MOVSX r32,rm8</td>
<td>Move byte to doubleword, sign-extension</td>
</tr>
<tr>
<td>0F BF /r</td>
<td>MOVSX r32,rm16</td>
<td>Move word to doubleword, sign-extension</td>
</tr>
</tbody>
</table>

**Description**
Copies the contents of the source operand (register or memory location) to the destination operand (register) and sign extends the value to 16 or 32 bits. The size of the converted value depends on the operand-size attribute.

**Operation**
\[
\text{DEST} \leftarrow \text{SignExtend(SRC)};
\]

**Flags Affected**
None.

**Additional Itanium® System Environment Exceptions**
- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Protected Mode Exceptions**
- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real Address Mode Exceptions**
- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.

**Virtual 8086 Mode Exceptions**
- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code) If a page fault occurs.
MOVZX—Move with Zero-Extend

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F B6 /r</td>
<td>MOVZX r16,rm8</td>
<td>Move byte to word with zero-extension</td>
</tr>
<tr>
<td>0F B6 /r</td>
<td>MOVZX r32,rm8</td>
<td>Move byte to doubleword, zero-extension</td>
</tr>
<tr>
<td>0F B7 /r</td>
<td>MOVZX r32,rm16</td>
<td>Move word to doubleword, zero-extension</td>
</tr>
</tbody>
</table>

**Description**

Copies the contents of the source operand (register or memory location) to the destination operand (register) and sign extends the value to 16 or 32 bits. The size of the converted value depends on the operand-size attribute.

Copies the contents of the source operand (register or memory location) to the destination operand (register) and zero extends the value to 16 or 32 bits. The size of the converted value depends on the operand-size attribute.

**Operation**

DEST ← ZeroExtend(SRC);

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Protected Mode Exceptions**

- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real Address Mode Exceptions**

- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.
MOVZX—Move with Zero-Extend (Continued)

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
MUL—Unsigned Multiplication of AL, AX, or EAX

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /4</td>
<td>MUL r/m8</td>
<td>Unsigned multiply (AX ← AL * r/m8)</td>
</tr>
<tr>
<td>F7 /4</td>
<td>MUL r/m16</td>
<td>Unsigned multiply (DX:AX ← AX * r/m16)</td>
</tr>
<tr>
<td>F7 /4</td>
<td>MUL r/m32</td>
<td>Unsigned multiply (EDX:EAX ← EAX * r/m32)</td>
</tr>
</tbody>
</table>

Description

Performs an unsigned multiplication of the first operand (destination operand) and the second operand (source operand) and stores the result in the destination operand. The destination operand is an implied operand located in register AL, AX or EAX (depending on the size of the operand); the source operand is located in a general-purpose register or a memory location. The action of this instruction and the location of the result depends on the opcode and the operand size as shown in the following table:

<table>
<thead>
<tr>
<th>Operand Size</th>
<th>Source 1</th>
<th>Source 2</th>
<th>Destination</th>
</tr>
</thead>
<tbody>
<tr>
<td>Byte</td>
<td>AL</td>
<td>r/m8</td>
<td>AX</td>
</tr>
<tr>
<td>Word</td>
<td>AX</td>
<td>r/m16</td>
<td>DX:AX</td>
</tr>
<tr>
<td>Doubleword</td>
<td>EAX</td>
<td>r/m32</td>
<td>EDX:EAX</td>
</tr>
</tbody>
</table>

The AH, DX, or EDX registers (depending on the operand size) contain the high-order bits of the product. If the contents of one of these registers are 0, the CF and OF flags are cleared; otherwise, the flags are set.

Operation

IF byte operation
  THEN
  AX ← AL * SRC
  ELSE (* word or doubleword operation *)
    IF OperandSize = 16
      THEN
        DX:AX ← AX * SRC
        ELSE (* OperandSize = 32 *)
          EDX:EAX ← EAX * SRC
    FI;
  FI;

Flags Affected

The OF and CF flags are cleared to 0 if the upper half of the result is 0; otherwise, they are set to 1. The SF, ZF, AF, and PF flags are undefined.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
MUL—Unsigned Multiplication of AL, AX, or EAX (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
NEG—Two's Complement Negation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /3</td>
<td>NEG r/m8</td>
<td>Two's complement negate r/m8</td>
</tr>
<tr>
<td>F7 /3</td>
<td>NEG r/m16</td>
<td>Two's complement negate r/m16</td>
</tr>
<tr>
<td>F7 /3</td>
<td>NEG r/m32</td>
<td>Two's complement negate r/m32</td>
</tr>
</tbody>
</table>

**Description**

Replaces the value of operand (the destination operand) with its two's complement. The destination operand is located in a general-purpose register or a memory location.

**Operation**

\[
\text{IF } \text{DEST} = 0 \\
\quad \text{THEN CF} \leftarrow 0 \\
\quad \text{ELSE CF} \leftarrow 1; \\
\text{FI;} \\
\text{DEST} \leftarrow - (\text{DEST})
\]

**Flags Affected**

The CF flag cleared to 0 if the source operand is 0; otherwise it is set to 1. The OF, SF, ZF, AF, and PF flags are set according to the result.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Protected Mode Exceptions**

- #GP(0) If the destination is located in a nonwritable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real Address Mode Exceptions**

- #GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- #SS If a memory operand effective address is outside the SS segment limit.
NEG—Two's Complement Negation (Continued)

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
NOP—No Operation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>90</td>
<td>NOP</td>
<td>No operation</td>
</tr>
</tbody>
</table>

**Description**

Performs no operation. This instruction is a one-byte instruction that takes up space in the instruction stream but does not affect the machine context, except the EIP register.

The NOP instruction performs no operation, no registers are accessed and no faults are generated.

**Flags Affected**

None.

**Exceptions (All Operating Modes)**

None.
NOT—One’s Complement Negation

**Description**

Performs a bitwise NOT operation (1’s complement) on the destination operand and stores the result in the destination operand location. The destination operand can be a register or a memory location.

**Operation**

\[ \text{DEST} \leftarrow \text{NOT DEST}; \]

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>NaT Register Consumption Abort.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>

**Protected Mode Exceptions**

- **#GP(0)**
  - If the destination operand points to a nonwritable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.

- **#SS(0)**
  - If a memory operand effective address is outside the SS segment limit.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real Address Mode Exceptions**

- **#GP**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS**
  - If a memory operand effective address is outside the SS segment limit.

**Opcode Instruction Description**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F6 /2</td>
<td>NOT r/m8</td>
<td>Reverse each bit of r/m8</td>
</tr>
<tr>
<td>F7 /2</td>
<td>NOT r/m16</td>
<td>Reverse each bit of r/m16</td>
</tr>
<tr>
<td>F7 /2</td>
<td>NOT r/m32</td>
<td>Reverse each bit of r/m32</td>
</tr>
</tbody>
</table>
NOT—One’s Complement Negation (Continued)

Virtual 8086 Mode Exceptions

<table>
<thead>
<tr>
<th>Exception Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP(0)</td>
<td>If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.</td>
</tr>
<tr>
<td>#SS(0)</td>
<td>If a memory operand effective address is outside the SS segment limit.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#AC(0)</td>
<td>If alignment checking is enabled and an unaligned memory reference is made.</td>
</tr>
</tbody>
</table>
OR—Logical Inclusive OR

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0C ib</td>
<td>OR AL, imm8</td>
<td>AL OR imm8</td>
</tr>
<tr>
<td>0D iw</td>
<td>OR AX, imm16</td>
<td>AX OR imm16</td>
</tr>
<tr>
<td>0D id</td>
<td>OR EAX, imm32</td>
<td>EAX OR imm32</td>
</tr>
<tr>
<td>80 /1 ib</td>
<td>OR r/m8, imm8</td>
<td>r/m8 OR imm8</td>
</tr>
<tr>
<td>81 /1 iw</td>
<td>OR r/m16, imm16</td>
<td>r/m16 OR imm16</td>
</tr>
<tr>
<td>81 /1 id</td>
<td>OR r/m32, imm32</td>
<td>r/m32 OR imm32</td>
</tr>
<tr>
<td>83 /1 ib</td>
<td>OR r/m16, imm8</td>
<td>r/m16 OR imm8</td>
</tr>
<tr>
<td>83 /1 id</td>
<td>OR r/m32, imm8</td>
<td>r/m32 OR imm8</td>
</tr>
<tr>
<td>08 /r</td>
<td>OR r/m8, r8</td>
<td>r/m8 OR r8</td>
</tr>
<tr>
<td>09 /r</td>
<td>OR r/m16, r16</td>
<td>r/m16 OR r16</td>
</tr>
<tr>
<td>09 /r</td>
<td>OR r/m32, r32</td>
<td>r/m32 OR r32</td>
</tr>
<tr>
<td>0A /r</td>
<td>OR r8, r/m8</td>
<td>r8 OR r/m8</td>
</tr>
<tr>
<td>0B /r</td>
<td>OR r16, r/m16</td>
<td>r16 OR r/m16</td>
</tr>
<tr>
<td>0B /r</td>
<td>OR r32, r/m32</td>
<td>r32 OR r/m32</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise OR operation on the destination (first) and source (second) operands and stores the result in the destination operand location. The source operand can be an immediate, a register, or a memory location; the destination operand can be a register or a memory location.

**Operation**

DEST ← DEST OR SRC;

**Flags Affected**

The OF and CF flags are cleared; the SF, ZF, and PF flags are set according to the result. The state of the AF flag is undefined.

**Additional Itanium® System Environment Exceptions**

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>NaT Register Consumption Abort.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>
OR—Logical Inclusive OR (Continued)

Protected Mode Exceptions
#GP(0) If the destination operand points to a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
OUT—Output to Port

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E6 ib</td>
<td>OUT imm8, AL</td>
<td>Output byte AL to imm8 I/O port address</td>
</tr>
<tr>
<td>E7 ib</td>
<td>OUT imm8, AX</td>
<td>Output word AX to imm8 I/O port address</td>
</tr>
<tr>
<td>E7 ib</td>
<td>OUT imm8, EAX</td>
<td>Output doubleword EAX to imm8 I/O port address</td>
</tr>
<tr>
<td>EE</td>
<td>OUT DX, AL</td>
<td>Output byte AL to I/O port address in DX</td>
</tr>
<tr>
<td>EF</td>
<td>OUT DX, AX</td>
<td>Output word AX to I/O port address in DX</td>
</tr>
<tr>
<td>EF</td>
<td>OUT DX, EAX</td>
<td>Output doubleword EAX to I/O port address in DX</td>
</tr>
</tbody>
</table>

**Description**

Copies the value from the second operand (source operand) to the I/O port specified with the destination operand (first operand). The source operand can be register AL, AX, or EAX, depending on the size of the port being accessed (8, 16, or 32 bits, respectively); the destination operand can be a byte-immediate or the DX register. Using a byte immediate allows I/O port addresses 0 to 255 to be accessed; using the DX register as a source operand allows I/O ports from 0 to 65,535 to be accessed.

When accessing an 8-bit I/O port, the opcode determines the port size; when accessing a 16- and 32-bit I/O port, the operand-size attribute determines the port size.

At the machine code level, I/O instructions are shorter when accessing 8-bit I/O ports. Here, the upper eight bits of the port address will be 0.

This instruction is only useful for accessing I/O ports located in the processor’s I/O address space.

I/O transactions are performed after all prior data memory operations. No subsequent data memory operations can pass an I/O transaction.

In the Itanium System Environment, I/O port references are mapped into the 64-bit virtual address pointed to by the IOBase register, with four ports per 4K-byte virtual page. Operating systems can utilize TLBs in the Itanium architecture to grant or deny permission to any four I/O ports. The I/O port space can be mapped into any arbitrary 64-bit physical memory location by operating system code. If CFLG.io is 1 and CPL>IOPL, the TSS is consulted for I/O permission. If CFLG.io is 0 or CPL<=IOPL, permission is granted regardless of the state of the TSS I/O permission bitmap (the bitmap is not referenced).

If the referenced I/O port is mapped to an unimplemented virtual address (via the I/O Base register) or if data translations are disabled (PSR.dt is 0) a GPFault is generated on the referencing OUT instruction.

**Operation**

```
IF ((PE = 1) AND ((VM = 1) OR (CPL > IOPL)))
    THEN (* Protected mode or virtual-8086 mode with CPL > IOPL *)
        IF (CFLG.io AND Any I/O Permission Bit for I/O port being accessed = 1)
            THEN #GP(0);
    FI;
ELSE (* Real-address mode or protected mode with CPL ≤ IOPL *)
    (* or virtual-8086 mode with all I/O permission bits for I/O port cleared *)
```
OUT—Output to Port (Continued)

FI;
IF (Itanium_System_Environment) THEN
  DEST_VA = IOBase | (Port{15:2}<<12) | Port{11:0};
  DEST_PA = translate(DEST_VA);

  [DEST_PA] ← SRC; (* Writes to selected I/O port *)
FI;

memory_fence();
[DEST_PA] ← SRC; (* Writes to selected I/O port *)
memory_fence();

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults   NaT Register Consumption Abort.

Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

IA-32_Exception Debug traps for data breakpoints and single step
IA-32_Exception Alignment faults
#GP(0) Referenced Port is to an unimplemented virtual address or PSR.dt is zero.

Protected Mode Exceptions

#GP(0) If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1 and when CFLG.io is 1.

Real Address Mode Exceptions

None.

Virtual 8086 Mode Exceptions

#GP(0) If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.
OUTS/OUTSB/OUTSW/OUTSD—Output String to Port

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>6E</td>
<td>OUTS DX, DS:(E)SI</td>
<td>Output byte at address DS:(E)SI to I/O port in DX</td>
</tr>
<tr>
<td>6F</td>
<td>OUTS DX, DS:SI</td>
<td>Output word at address DS:SI to I/O port in DX</td>
</tr>
<tr>
<td>6F</td>
<td>OUTS DX, DS:ESI</td>
<td>Output doubleword at address DS:ESI to I/O port in DX</td>
</tr>
<tr>
<td>6E</td>
<td>OUTSB</td>
<td>Output byte at address DS:(E)SI to I/O port in DX</td>
</tr>
<tr>
<td>6F</td>
<td>OUTSW</td>
<td>Output word at address DS:SI to I/O port in DX</td>
</tr>
<tr>
<td>6F</td>
<td>OUTSD</td>
<td>Output doubleword at address DS:ESI to I/O port in DX</td>
</tr>
</tbody>
</table>

**Description**

Copies data from the second operand (source operand) to the I/O port specified with the first operand (destination operand). The source operand is a memory location at the address DS:ESI. (When the operand-size attribute is 16, the SI register is used as the source-index register.) The DS register may be overridden with a segment override prefix.

The destination operand must be the DX register, allowing I/O port addresses from 0 to 65,535 to be accessed. When accessing an 8-bit I/O port, the opcode determines the port size; when accessing a 16- and 32-bit I/O port, the operand-size attribute determines the port size.

The OUTSB, OUTSW and OUTSD mnemonics are synonyms of the byte, word, and doubleword versions of the OUTS instructions. (For the OUTS instruction, “DS:ESI” must be explicitly specified in the instruction.)

After the byte, word, or doubleword is transfer from the memory location to the I/O port, the ESI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the ESI register is incremented; if the DF flag is 1, the EDI register is decremented.) The ESI register is incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The OUTS, OUTSB, OUTSW, and OUTSD instructions can be preceded by the REP prefix for block input of ECX bytes, words, or doublewords. See “REP/REPE/REPZ/REPNE /REPNZ—Repeat String Operation Prefix” on page 3:685 for a description of the REP prefix.

After an OUTS, OUTSB, OUTSW, or OUTSD instruction is executed, the processor waits for the acknowledgment of the OUT transaction before beginning to execute the next instruction. Note that the next instruction may be prefetched, even if the OUT transaction has not completed.

This instruction is only useful for accessing I/O ports located in the processor’s I/O address space.

**I/O transactions are performed after all prior data memory operations. No subsequent data memory operations can pass an I/O transaction.**
OUTS/OUTSB/OUTSW/OUTSD—Output String to Port (Continued)

In the Itanium System Environment, I/O port references are mapped into the 64-bit virtual address pointed to by the IOBase register, with four ports per 4K-byte virtual page. Operating systems can utilize TLBs in the Itanium architecture to grant or deny permission to any four I/O ports. The I/O port space can be mapped into any arbitrary 64-bit physical memory location by operating system code. If CFLG.io is 1 and CPL>IOPL, the TSS is consulted for I/O permission. If CFLG.io is 0 or CPL<=IOPL, permission is granted regardless of the state of the TSS I/O permission bitmap (the bitmap is not referenced).

If the referenced I/O port is mapped to an unimplemented virtual address (via the I/O Base register) or if data translations are disabled (PSR.dt is 0) a GPFault is generated on the referencing OUTS instruction.

Operation

IF ((PE = 1) AND ((VM = 1) OR (CPL > IOPL)))
    THEN (* Protected mode or virtual-8086 mode with CPL > IOPL *)
        IF (CFLG.io AND Any I/O Permission Bit for I/O port being accessed = 1)
            THEN #GP(0);
        ELSE (* I/O operation is allowed *)
    FI;
ELSE (* I/O operation is allowed *)
FI;

IF (Itanium_System_Environment) THEN
    DEST_VA = IOBase | (Port{15:2}<<12) | Port{11:0};
    DEST_PA = translate(DEST_VA);
    [DEST_PA] ← SRC; (* Writes to selected I/O port *)
    FI;
    memory_fence();
    [DEST_PA] ← SRC; (* Writes to selected I/O port *)
    memory_fence();

IF (byte operation)
    THEN IF DF = 0
        THEN (E)DI ← 1;
        ELSE (E)DI ← –1;
    FI;
ELSE IF (word operation)
    THEN IF DF = 0
        THEN DI ← 2;
        ELSE DI ← –2;
    FI;
ELSE (* doubleword operation *)
    THEN IF DF = 0
        THEN EDI ← 4;
        ELSE EDI ← –4;
    FI;
    FI;
FI;
FI;

Flags Affected

None.
OUTS/OUTSB/OUTSW/OUTSD—Output String to Port (Continued)

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Exception Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Reg Faults</td>
<td>NaT Register Consumption Abort.</td>
</tr>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
<tr>
<td>IA-32_Exception</td>
<td>Debug traps for data breakpoints and single step</td>
</tr>
<tr>
<td>IA-32_Exception</td>
<td>Alignment faults</td>
</tr>
<tr>
<td>#GP(0)</td>
<td>Referenced Port is to an unimplemented virtual address or PSR.dt is zero.</td>
</tr>
</tbody>
</table>

Protected Mode Exceptions

- **#GP(0)**
  - If the CPL is greater than (has less privilege) the I/O privilege level (IOPL) and any of the corresponding I/O permission bits in TSS for the I/O port being accessed is 1 and when CFLG.io is 1.
  - If the destination is located in a nonwritable segment.
  - If a memory operand effective address is outside the limit of the ES segment.
  - If the ES register contains a null segment selector.
  - If an illegal memory operand effective address in the ES segments is given.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

- **#GP**
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS**
  - If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

- **#GP(0)**
  - If any of the I/O permission bits in the TSS for the I/O port being accessed is 1.

- **#PF(fault-code)**
  - If a page fault occurs.

- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made.
POP—Pop a Value from the Stack

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>8F /0</td>
<td>POP m16</td>
<td>Pop top of stack into m16; increment stack pointer</td>
</tr>
<tr>
<td>8F /0</td>
<td>POP m32</td>
<td>Pop top of stack into m32; increment stack pointer</td>
</tr>
<tr>
<td>58+ rw</td>
<td>POP r16</td>
<td>Pop top of stack into r16; increment stack pointer</td>
</tr>
<tr>
<td>58+ rd</td>
<td>POP r32</td>
<td>Pop top of stack into r32; increment stack pointer</td>
</tr>
<tr>
<td>1F</td>
<td>POP DS</td>
<td>Pop top of stack into DS; increment stack pointer</td>
</tr>
<tr>
<td>07</td>
<td>POP ES</td>
<td>Pop top of stack into ES; increment stack pointer</td>
</tr>
<tr>
<td>17</td>
<td>POP SS</td>
<td>Pop top of stack into SS; increment stack pointer</td>
</tr>
<tr>
<td>0F A1</td>
<td>POP FS</td>
<td>Pop top of stack into FS; increment stack pointer</td>
</tr>
<tr>
<td>0F A9</td>
<td>POP GS</td>
<td>Pop top of stack into GS; increment stack pointer</td>
</tr>
</tbody>
</table>

Description

Loads the value from the top of the procedure stack to the location specified with the destination operand and then increments the stack pointer. The destination operand can be a general-purpose register, memory location, or segment register.

The current address-size attribute for the stack segment and the operand-size attribute determine the amount the stack pointer is incremented (see the “Operation” below). For example, if 32-bit addressing and operands are being used, the ESP register (stack pointer) is incremented by 4 and, if 16-bit addressing and operands are being used, the SP register (stack pointer for 16-bit addressing) is incremented by 2. The B flag in the stack segment’s segment descriptor determines the stack’s address-size attribute.

If the destination operand is one of the segment registers DS, ES, FS, GS, or SS, the value loaded into the register must be a valid segment selector. In protected mode, popping a segment selector into a segment register automatically causes the descriptor information associated with that segment selector to be loaded into the hidden (shadow) part of the segment register and causes the selector and the descriptor information to be validated (see the “Operation” below).

A null value (0000-0003) may be popped into the DS, ES, FS, or SS register without causing a general protection fault. However, any subsequent attempt to reference a segment whose corresponding segment register is loaded with a null value causes a general protection exception (#GP). In this situation, no memory reference occurs and the saved value of the segment register is null.

The POP instruction cannot pop a value into the CS register. To load the CS register, use the RET instruction.

A POP SS instruction inhibits all external interrupts, including the NMI interrupt, and traps until after execution of the next instruction. in the IA-32 System Environment. For the Itanium System Environment, POP SS results in an IA-32_Intercept(SystemFlag) trap after the instruction completes. This operation allows a stack pointer to be loaded into the ESP register with the next instruction (MOV ESP, stack-pointer value) before an interrupt occurs. The LSS instruction offers a more efficient method of loading the SS and ESP registers.
POP—Pop a Value from the Stack (Continued)

This action allows sequential execution of POP SS and MOV ESP, EBP instructions without the danger of having an invalid stack during an interrupt. However, use of the LSS instruction is the preferred method of loading the SS and ESP registers.

If the ESP register is used as a base register for addressing a destination operand in memory, the POP instructions computes the effective address of the operand after it increments the ESP register.

The POP ESP instruction increments the stack pointer (ESP) before data at the old top of stack is written into the destination.

Operation

IF StackAddrSize = 32
THEN
  IF OperandSize = 32
  THEN
    DEST ← SS:ESP; (* copy a doubleword *)
    ESP ← ESP + 4;
  ELSE (* OperandSize = 16 *)
    DEST ← SS:ESP; (* copy a word *)
    ESP ← ESP + 2;
  FI;
  ELSE (* StackAddrSize = 16 * )
  IF OperandSize = 16
  THEN
    DEST ← SS:SP; (* copy a word *)
    SP ← SP + 2;
  ELSE (* OperandSize = 32 *)
    DEST ← SS:SP; (* copy a doubleword *)
    SP ← SP + 4;
  FI;
FI;

Loading a segment register while in protected mode results in special checks and actions, as described in the following listing. These checks are performed on the segment selector and the segment descriptor it points to.

IF SS is loaded;
THEN
  IF segment selector is null
  THEN #GP(0);
  FI;
  IF segment selector index is outside descriptor table limits
  OR segment selector's RPL ≠ CPL
  OR segment is not a writable data segment
  OR DPL ≠ CPL
  THEN #GP(selector);
  FI;
  IF segment not marked present
  THEN #SS(selector);
ELSE
  SS ← segment selector;
  SS ← segment descriptor;
FI;
POP—Pop a Value from the Stack (Continued)

FI;
IF DS, ES, FS or GS is loaded with non-null selector;
THEN
   IF segment selector index is outside descriptor table limits
      OR segment is not a data or readable code segment
      OR ((segment is a data or nonconforming code segment)
         AND (both RPL and CPL > DPL))
         THEN #GP(selector);
      IF segment not marked present
         THEN #NP(selector);
   ELSE
      SegmentRegister ← segment selector;
      SegmentRegister ← segment descriptor;
   FI;
FI;
IF DS, ES, FS or GS is loaded with a null selector;
THEN
   SegmentRegister ← null segment selector;
   SegmentRegister ← null segment descriptor;
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

IA-32_Intercept System Flag Intercept trap for POP SS
Itanium Reg Faults NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If attempt is made to load SS register with null segment selector.
   If the destination operand is in a nonwritable segment.
   If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#GP(selector) If segment selector index is outside descriptor table limits.
   If the SS register is being loaded and the segment selector's RPL and the segment descriptor’s DPL are not equal to the CPL.
   If the SS register is being loaded and the segment pointed to is a nonwritable data segment.
POP—Pop a Value from the Stack (Continued)

If the DS, ES, FS, or GS register is being loaded and the segment pointed to is not a data or readable code segment.

If the DS, ES, FS, or GS register is being loaded and the segment pointed to is a data or nonconforming code segment, but both the RPL and the CPL are greater than the DPL.

#SS(0) If the current top of stack is not within the stack segment.

If a memory operand effective address is outside the SS segment limit.

#SS(selector) If the SS register is being loaded and the segment pointed to is marked not present.

#NP If the DS, ES, FS, or GS register is being loaded and the segment pointed to is marked not present.

#PF(fault-code) If a page fault occurs.

#AC(0) If an unaligned memory reference is made while the current privilege level is 3 and alignment checking is enabled.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If an unaligned memory reference is made while alignment checking is enabled.
POPA/POPAD—Pop All General-Purpose Registers

Description

Pops doublewords (POPAD) or words (POPA) from the procedure stack into the general-purpose registers. The registers are loaded in the following order: EDI, ESI, EBP, EBX, EDX, ECX, and EAX (if the current operand-size attribute is 32) and DI, SI, BP, BX, DX, CX, and AX (if the operand-size attribute is 16). (These instructions reverse the operation of the PUSHA/PUSHAD instructions.) The value on the stack for the ESP or SP register is ignored. Instead, the ESP or SP register is incremented after each register is loaded (see the “Operation” below).

The POPA (pop all) and POPAD (pop all double) mnemonics reference the same opcode. The POPA instruction is intended for use when the operand-size attribute is 16 and the POPAD instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when POPA is used and to 32 when POPAD is used. Others may treat these mnemonics as synonyms (POPA/POPAD) and use the current setting of the operand-size attribute to determine the size of values to be popped from the stack, regardless of the mnemonic used.

Operation

IF OperandSize = 32 (* instruction = POPAD *)
THEN
  EDI ← Pop();
  ESI ← Pop();
  EBP ← Pop();
  increment ESP by 4 (* skip next 4 bytes of stack *)
  EBX ← Pop();
  EDX ← Pop();
  ECX ← Pop();
  EAX ← Pop();
ELSE (* OperandSize = 16, instruction = POPA *)
  DI ← Pop();
  SI ← Pop();
  BP ← Pop();
  increment ESP by 2 (* skip next 2 bytes of stack *)
  BX ← Pop();
  DX ← Pop();
  CX ← Pop();
  AX ← Pop();
FI;

Flags Affected

None.
POPA/POPAD—Pop All General-Purpose Registers (Continued)

Additional Itanium® System Environment Exceptions
Itanium Reg Faults NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions
#SS(0) If the starting or ending stack address is not within the stack segment.
#PF(fault-code) If a page fault occurs.

Real Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
POPF/POPFD—Pop Stack into EFLAGS Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9D</td>
<td>POPF</td>
<td>Pop top of stack into EFLAGS</td>
</tr>
<tr>
<td>9D</td>
<td>POPFD</td>
<td>Pop top of stack into EFLAGS</td>
</tr>
</tbody>
</table>

**Description**

Pops a doubleword (POPF) from the top of the stack (if the current operand-size attribute is 32) and stores the value in the EFLAGS register or pops a word from the top of the stack (if the operand-size attribute is 16) and stores it in the lower 16 bits of the EFLAGS register. (These instructions reverse the operation of the PUSHF/PUSHFD instructions.)

The POPF (pop flags) and POPFD (pop flags double) mnemonics reference the same opcode. The POPF instruction is intended for use when the operand-size attribute is 16 and the POPFD instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when POPF is used and to 32 when POPFD is used. Others may treat these mnemonics as synonyms (POPF/POPFD) and use the current setting of the operand-size attribute to determine the size of values to be popped from the stack, regardless of the mnemonic used.

The effect of the POPF/POPFD instructions on the EFLAGS register changes slightly, depending on the mode of operation of the processor. When the processor is operating in protected mode at privilege level 0 (or in real-address mode, which is equivalent to privilege level 0), all the non-reserved flags in the EFLAGS register except the VIP and VIF flags can be modified. The VIP and VIF flags are cleared.

When operating in protected mode, but with a privilege level greater an 0, all the flags can be modified except the IOPL field and the VIP and VIF flags. Here, the IOPL flags are masked and the VIP and VIF flags are cleared.

When operating in virtual-8086 mode, the I/O privilege level (IOPL) must be equal to 3 to use POPF/POPFD instructions and the VM, RF, IOPL, VIP, and VIF flags are masked. If the IOPL is less than 3, the POPF/POPFD instructions cause a general protection exception (#GP).

The IOPL is altered only when executing at privilege level 0. The interrupt flag is altered only when executing at a level at least as privileged as the IOPL. (Real-address mode is equivalent to privilege level 0.) If a POPF/POPFD instruction is executed with insufficient privilege, an exception does not occur, but the privileged bits do not change.

**Operation**

```plaintext
OLD_IF <- IF; OLD_AC <- AC; OLD_TF <- TF;
IF CR0.PE = 0 (*Real Mode *)
    THEN
        IF OperandSize = 32;
            THEN
                EFLAGS ← Pop();
                (* All non-reserved flags except VM, RF, VIP and VIF can be modified; *)
                ELSE (*OperandSize = 16 *)
                    EFLAGS[15:0] ← Pop(); (* All non-reserved flags can be modified; *)
                FI;
            ELSE (*In Protected Mode *)
                IF VM=0 (* Not in Virtual-8086 Mode *)
                    THEN
```
POPF/POPFD—Pop Stack into EFLAGS Register (Continued)

IF CPL=0
THEN
IF OperandSize = 32;
    THEN
        EFLAGS ← Pop();
        (* All non-reserved flags except VM, RF, VIP and VIF can be *)
        (* modified; *)
    ELSE (* OperandSize = 16 *)
        EFLAGS[15:0] ← Pop(); (* All non-reserved flags can be modified; *)
    FI;
ELSE (* CPL > 0 *)
IF OperandSize = 32;
THEN
    EFLAGS ← Pop()
    (* All non-reserved bits except IOPL, RF, VM, VIP, and VIF can *)
    (* be modified; *)
    (* IOPL is masked *)
ELSE (* OperandSize = 16 *)
    EFLAGS[15:0] ← Pop();
    (* All non-reserved bits except IOPL can be modified; IOPL is *)
    (* masked *)
    FI;
FI;
ELSE (* In Virtual-8086 Mode *)
IF IOPL=3
THEN
    IF OperandSize=32
    THEN
        EFLAGS ← Pop()
        (* All non-reserved bits except VM, RF, IOPL, VIP, and VIF *)
        (* can be modified; VM, RF, IOPL, VIP, and VIF are masked*)
    ELSE
        EFLAGS[15:0] ← Pop()
        (* All non-reserved bits except IOPL can be modified; IOPL is *)
        (* masked *)
    FI;
ELSE (* IOPL < 3 *)
IF CR4.VME = 0
    THEN #GP(0);
ELSE
    IF ((OperandSize = 32) OR (STACK.TF = 1) OR (EFLAGS.VIP = 1
    AND STACK.IF = 1))
        THEN #GP(0);
    ELSE
        TempFlags ← pop();
        FLAGS ← TempFlags; (*IF and IOPL bits are unchanged*)
        EFLAGS.VIF ← TempFlags.IF;
        FI;
    FI;
FI;
FI;
POPF/POPFD—Pop Stack into EFLAGS Register (Continued)

IF (Itanium System Environment AND (AC, TF != OLD_AC, OLD_TF))
THEN IA-32_Intercept(System_Flag,POPF);
IF Itanium System Environment AND CFLG.ii AND IF != OLD_IF
THEN IA-32_Intercept(System_Flag,POPF);

Flags Affected

All flags except the reserved bits.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB
Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data
Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data
Access Bit Fault, Data Dirty Bit Fault
IA-32_Intercept  System Flag Intercept Trap if CFLG.ii is 1 and the IF flag changes state or if
the AC, RF or TF changes state.

Protected Mode Exceptions

#SS(0)  If the top of stack is not within the stack segment.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.
If the I/O privilege level is less than 3.
If an attempt is made to execute the POPF/POPFD instruction with an
operand-size override prefix.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
PUSH—Push Word or Doubleword Onto the Stack

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FF /6</td>
<td>PUSH r/m16</td>
<td>Push r/m16</td>
</tr>
<tr>
<td>FF /6</td>
<td>PUSH r/m32</td>
<td>Push r/m32</td>
</tr>
<tr>
<td>50+/rw</td>
<td>PUSH r16</td>
<td>Push r16</td>
</tr>
<tr>
<td>50+/rd</td>
<td>PUSH r32</td>
<td>Push r32</td>
</tr>
<tr>
<td>6A</td>
<td>PUSH imm8</td>
<td>Push imm8</td>
</tr>
<tr>
<td>68</td>
<td>PUSH imm16</td>
<td>Push imm16</td>
</tr>
<tr>
<td>68</td>
<td>PUSH imm32</td>
<td>Push imm32</td>
</tr>
<tr>
<td>0E</td>
<td>PUSH CS</td>
<td>Push CS</td>
</tr>
<tr>
<td>16</td>
<td>PUSH SS</td>
<td>Push SS</td>
</tr>
<tr>
<td>1E</td>
<td>PUSH DS</td>
<td>Push DS</td>
</tr>
<tr>
<td>06</td>
<td>PUSH ES</td>
<td>Push ES</td>
</tr>
<tr>
<td>0F A0</td>
<td>PUSH FS</td>
<td>Push FS</td>
</tr>
<tr>
<td>0F A8</td>
<td>PUSH GS</td>
<td>Push GS</td>
</tr>
</tbody>
</table>

Description

Decrement the stack pointer and then stores the source operand on the top of the procedure stack. The current address-size attribute for the stack segment and the operand-size attribute determine the amount the stack pointer is decremented (see the “Operation” below). For example, if 32-bit addressing and operands are being used, the ESP register (stack pointer) is decremented by 4 and, if 16-bit addressing and operands are being used, the SP register (stack pointer for 16-bit addressing) is decremented by 2. Pushing 16-bit operands when the stack address-size attribute is 32 can result in a misaligned the stack pointer (that is, the stack pointer not aligned on a doubleword boundary).

The PUSH ESP instruction pushes the value of the ESP register as it existed before the instruction was executed. Thus, if a PUSH instruction uses a memory operand in which the ESP register is used as a base register for computing the operand address, the effective address of the operand is computed before the ESP register is decremented.

In the real-address mode, if the ESP or SP register is 1 when the PUSH instruction is executed, the processor shuts down due to a lack of stack space. No exception is generated to indicate this condition.

Operation

\[
\text{IF StackAddrSize = 32} \\
\text{THEN} \\
\hspace{1em} \text{IF OperandSize = 32} \\
\hspace{2em} \text{THEN} \\
\hspace{3em} \text{ESP ← ESP} - 4; \\
\hspace{3em} \text{SS:ESP ← SRC; (* push doubleword *)} \\
\hspace{2em} \text{ELSE (* OperandSize = 16*)} \\
\hspace{3em} \text{ESP ← ESP} - 2; \\
\hspace{3em} \text{SS:ESP ← SRC; (* push word *)} \\
\hspace{1em} \text{FI;} \\
\text{ELSE (* StackAddrSize = 16*)}
\]
PUSH—Push Word or Doubleword Onto the Stack (Continued)

IF OperandSize = 16
    THEN
        SP ← SP − 2;
        SS:SP ← SRC; (* push word *)
    ELSE (* OperandSize = 32*)
        SP ← SP − 4;
        SS:SP ← SRC; (* push doubleword *)
FI;
FI;

Flags Affected
None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults       NaT Register Consumption Abort.
Itanium Mem Faults      VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
         If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.
     If the new value of the SP or ESP register is outside the stack segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
PUSH—Push Word or Doubleword Onto the Stack (Continued)

#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Intel® Architecture Compatibility

For Intel architecture processors from the Intel 286 on, the PUSH ESP instruction pushes the value of the ESP register as it existed before the instruction was executed. (This is also true in the real-address and virtual-8086 modes.) For the Intel 8086 processor, the PUSH SP instruction pushes the new value of the SP register (that is the value after it has been decremented by 2).
PUSHA/PUSHAD—Push All General-Purpose Registers

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>PUSHAD</td>
<td>Push EAX, ECX, EDX, EBX, original ESP, EBP, ESI, and EDI</td>
</tr>
<tr>
<td>60</td>
<td>PUSHAD</td>
<td>Push AX, CX, DX, BX, original SP, BP, SI, and DI</td>
</tr>
</tbody>
</table>

Description

Push the contents of the general-purpose registers onto the procedure stack. The registers are stored on the stack in the following order: EAX, ECX, EDX, EBX, EBP, ESP (original value), EBP, ESI, and EDI (if the current operand-size attribute is 32) and AX, CX, DX, BX, SP (original value), BP, SI, and DI (if the operand-size attribute is 16). (These instructions perform the reverse operation of the POPA/POPAD instructions.) The value pushed for the ESP or SP register is its value before prior to pushing the first register (see the “Operation” below).

The PUSHA (push all) and PUSHAD (push all double) mnemonics reference the same opcode. The PUSHA instruction is intended for use when the operand-size attribute is 16 and the PUSHAD instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when PUSHA is used and to 32 when PUSHAD is used. Others may treat these mnemonics as synonyms (PUSHA/PUSHAD) and use the current setting of the operand-size attribute to determine the size of values to be pushed from the stack, regardless of the mnemonic used.

In the real-address mode, if the ESP or SP register is 1, 3, or 5 when the PUSHA/PUSHAD instruction is executed, the processor shuts down due to a lack of stack space. No exception is generated to indicate this condition.

Operation

IF OperandSize = 32 (* PUSHAD instruction *)
THEN
    Temp ← (ESP);
    Push(EAX);
    Push(ECX);
    Push(EDX);
    Push(EBX);
    Push(Temp);
    Push(EBP);
    Push(ESI);
    Push(EDI);
ELSE (* OperandSize = 16, PUSHA instruction *)
    Temp ← (SP);
    Push(AX);
    Push(CX);
    Push(DX);
    Push(BX);
    Push(Temp);
    Push(BP);
    Push(SI);
    Push(DI);
FI;
PUSHA/PUSHAD—Push All General-Purpose Registers (Continued)

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#SS(0)  If the starting or ending stack address is outside the stack segment limit.
#PF(fault-code)  If a page fault occurs.

Real Address Mode Exceptions

#GP  If the ESP or SP register contains 7, 9, 11, 13, or 15.

Virtual 8086 Mode Exceptions

#GP(0)  If the ESP or SP register contains 7, 9, 11, 13, or 15.
#PF(fault-code)  If a page fault occurs.
PUSHF/PUSHFD—Push EFLAGS Register onto the Stack

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
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</tr>
</thead>
<tbody>
<tr>
<td>9C</td>
<td>PUSHF</td>
<td>Push EFLAGS</td>
</tr>
<tr>
<td>9C</td>
<td>PUSHFD</td>
<td>Push EFLAGS</td>
</tr>
</tbody>
</table>

**Description**

Decrement the stack pointer by 4 (if the current operand-size attribute is 32) and push the entire contents of the EFLAGS register onto the procedure stack or decrement the stack pointer by 2 (if the operand-size attribute is 16) push the lower 16 bits of the EFLAGS register onto the stack. (These instructions reverse the operation of the POPF/POPFD instructions.)

When copying the entire EFLAGS register to the stack, bits 16 and 17, called the VM and RF flags, are not copied. Instead, the values for these flags are cleared in the EFLAGS image stored on the stack.

The PUSHF (push flags) and PUSHFD (push flags double) mnemonics reference the same opcode. The PUSHF instruction is intended for use when the operand-size attribute is 16 and the PUSHFD instruction for when the operand-size attribute is 32. Some assemblers may force the operand size to 16 when PUSHF is used and to 32 when PUSHFD is used. Others may treat these mnemonics as synonyms (PUSHF/PUSHFD) and use the current setting of the operand-size attribute to determine the size of values to be pushed from the stack, regardless of the mnemonic used.

When the I/O privilege level (IOPL) is less than 3 in virtual-8086 mode, the PUSHF/PUSHFD instructions causes a general protection exception (#GP). The IOPL is altered only when executing at privilege level 0. The interrupt flag is altered only when executing at a level at least as privileged as the IOPL. (Real-address mode is equivalent to privilege level 0.) If a PUSHF/PUSHFD instruction is executed with insufficient privilege, an exception does not occur, but the privileged bits do not change.

In the real-address mode, if the ESP or SP register is 1, 3, or 5 when the PUSHA/PUSHAD instruction is executed, the processor shuts down due to a lack of stack space. No exception is generated to indicate this condition.

**Operation**

IF VM=0 (* Not in Virtual-8086 Mode *)
THEN
IF OperandSize = 32
THEN
push(EFLAGS AND 00FCFFFFH); (* VM and RF EFLAG bits are cleared in image stored on the stack*)
ELSE
push(EFLAGS); (* Lower 16 bits only *)
FI;
ELSE (* In Virtual-8086 Mode *)
IF IOPL=3
THEN
IF OperandSize = 32
THEN push(EFLAGS AND 0FCFFFFH); (* VM and RF EFLAGS bits are cleared in image stored on the stack*)
ELSE push(EFLAGS); (* Lower 16 bits only *)

**Opcode Instruction Description**

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<tr>
<td>9C</td>
<td>PUSHF</td>
<td>Push EFLAGS</td>
</tr>
<tr>
<td>9C</td>
<td>PUSHFD</td>
<td>Push EFLAGS</td>
</tr>
</tbody>
</table>
PUSHF/PUSHFD—Push EFLAGS Register onto the Stack (Continued)

Fl;
ELSE (*IOPL < 3*)

IF OperandSize =32 OR CR$.VME=0
  THEN #GP(0); (* Trap to virtual-8086 monitor *)
ELSE
  TempFlags <- FLAGS OR 3000H; (*Set IOPL bits to 11B or IOPL 3 *)
  TempFlags.IF <- EFLAGS.VIF;
  push(TempFlags);
FI;
FI;
FI;

Flags Affected
None.

Additional Itanium® System Environment Exceptions

Protected Mode Exceptions
#SS(0) If the new value of the ESP register is outside the stack segment boundary.

Real Address Mode Exceptions
None.

Virtual 8086 Mode Exceptions
#GP(0) If the I/O privilege level is less than 3.
## RCL/RCR/ROL/ROR—Rotate

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0 /2</td>
<td>RCL r/m8,1</td>
<td>Rotate 9 bits (CF,r/m8) left once</td>
</tr>
<tr>
<td>D2 /2</td>
<td>RCL r/m8,CL</td>
<td>Rotate 9 bits (CF,r/m8) left CL times</td>
</tr>
<tr>
<td>C0 /2 ib</td>
<td>RCL r/m8,imm8</td>
<td>Rotate 9 bits (CF,r/m8) left imm8 times</td>
</tr>
<tr>
<td>D1 /2</td>
<td>RCL r/m16,1</td>
<td>Rotate 17 bits (CF,r/m16) left once</td>
</tr>
<tr>
<td>D3 /2</td>
<td>RCL r/m16,CL</td>
<td>Rotate 17 bits (CF,r/m16) left CL times</td>
</tr>
<tr>
<td>C1 /2 ib</td>
<td>RCL r/m16,imm8</td>
<td>Rotate 17 bits (CF,r/m16) left imm8 times</td>
</tr>
<tr>
<td>D1 /2</td>
<td>RCL r/m32,1</td>
<td>Rotate 33 bits (CF,r/m32) left once</td>
</tr>
<tr>
<td>D3 /2</td>
<td>RCL r/m32,CL</td>
<td>Rotate 33 bits (CF,r/m32) left CL times</td>
</tr>
<tr>
<td>C1 /2 ib</td>
<td>RCL r/m32,imm8</td>
<td>Rotate 33 bits (CF,r/m32) left imm8 times</td>
</tr>
<tr>
<td>D0 /3</td>
<td>RCR r/m8,1</td>
<td>Rotate 9 bits (CF,r/m8) right once</td>
</tr>
<tr>
<td>D2 /3</td>
<td>RCR r/m8,CL</td>
<td>Rotate 9 bits (CF,r/m8) right CL times</td>
</tr>
<tr>
<td>C0 /3 ib</td>
<td>RCR r/m8,imm8</td>
<td>Rotate 9 bits (CF,r/m8) right imm8 times</td>
</tr>
<tr>
<td>D1 /3</td>
<td>RCR r/m16,1</td>
<td>Rotate 17 bits (CF,r/m16) right once</td>
</tr>
<tr>
<td>D3 /3</td>
<td>RCR r/m16,CL</td>
<td>Rotate 17 bits (CF,r/m16) right CL times</td>
</tr>
<tr>
<td>C1 /3 ib</td>
<td>RCR r/m16,imm8</td>
<td>Rotate 17 bits (CF,r/m16) right imm8 times</td>
</tr>
<tr>
<td>D1 /3</td>
<td>RCR r/m32,1</td>
<td>Rotate 33 bits (CF,r/m32) right once</td>
</tr>
<tr>
<td>D3 /3</td>
<td>RCR r/m32,CL</td>
<td>Rotate 33 bits (CF,r/m32) right CL times</td>
</tr>
<tr>
<td>C1 /3 ib</td>
<td>RCR r/m32,imm8</td>
<td>Rotate 33 bits (CF,r/m32) right imm8 times</td>
</tr>
<tr>
<td>D0 /0</td>
<td>ROL r/m8,1</td>
<td>Rotate 8 bits r/m8 left once</td>
</tr>
<tr>
<td>D2 /0</td>
<td>ROL r/m8,CL</td>
<td>Rotate 8 bits r/m8 left CL times</td>
</tr>
<tr>
<td>C0 /0 ib</td>
<td>ROL r/m8,imm8</td>
<td>Rotate 8 bits r/m8 left imm8 times</td>
</tr>
<tr>
<td>D1 /0</td>
<td>ROL r/m16,1</td>
<td>Rotate 16 bits r/m16 left once</td>
</tr>
<tr>
<td>D3 /0</td>
<td>ROL r/m16,CL</td>
<td>Rotate 16 bits r/m16 left CL times</td>
</tr>
<tr>
<td>C1 /0 ib</td>
<td>ROL r/m16,imm8</td>
<td>Rotate 16 bits r/m16 left imm8 times</td>
</tr>
<tr>
<td>D1 /0</td>
<td>ROL r/m32,1</td>
<td>Rotate 32 bits r/m32 left once</td>
</tr>
<tr>
<td>D3 /0</td>
<td>ROL r/m32,CL</td>
<td>Rotate 32 bits r/m32 left CL times</td>
</tr>
<tr>
<td>C1 /0 ib</td>
<td>ROL r/m32,imm8</td>
<td>Rotate 32 bits r/m32 left imm8 times</td>
</tr>
<tr>
<td>D0 /1</td>
<td>ROR r/m8,1</td>
<td>Rotate 8 bits r/m8 right once</td>
</tr>
<tr>
<td>D2 /1</td>
<td>ROR r/m8,CL</td>
<td>Rotate 8 bits r/m8 right CL times</td>
</tr>
<tr>
<td>C0 /1 ib</td>
<td>ROR r/m8,imm8</td>
<td>Rotate 8 bits r/m8 right imm8 times</td>
</tr>
<tr>
<td>D1 /1</td>
<td>ROR r/m16,1</td>
<td>Rotate 16 bits r/m16 right once</td>
</tr>
<tr>
<td>D3 /1</td>
<td>ROR r/m16,CL</td>
<td>Rotate 16 bits r/m16 right CL times</td>
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<td>C1 /1 ib</td>
<td>ROR r/m16,imm8</td>
<td>Rotate 16 bits r/m16 right imm8 times</td>
</tr>
<tr>
<td>D1 /1</td>
<td>ROR r/m32,1</td>
<td>Rotate 32 bits r/m32 right once</td>
</tr>
<tr>
<td>D3 /1</td>
<td>ROR r/m32,CL</td>
<td>Rotate 32 bits r/m32 right CL times</td>
</tr>
<tr>
<td>C1 /1 ib</td>
<td>ROR r/m32,imm8</td>
<td>Rotate 32 bits r/m32 right imm8 times</td>
</tr>
</tbody>
</table>
RCL/RCR/ROL/ROR—Rotate (Continued)

Description

Shifts (rotates) the bits of the first operand (destination operand) the number of bit positions specified in the second operand (count operand) and stores the result in the destination operand. The destination operand can be a register or a memory location; the count operand is an unsigned integer that can be an immediate or a value in the CL register. The processor restricts the count to a number between 0 and 31 by masking all the bits in the count operand except the 5 least-significant bits.

The rotate left (ROL) and rotate through carry left (RCL) instructions shift all the bits toward more-significant bit positions, except for the most-significant bit, which is rotated to the least-significant bit location. The rotate right (ROR) and rotate through carry right (RCR) instructions shift all the bits toward less significant bit positions, except for the least-significant bit, which is rotated to the most-significant bit location.

The RCL and RCR instructions include the CF flag in the rotation. The RCL instruction shifts the CF flag into the least-significant bit and shifts the most-significant bit into the CF flag. The RCR instruction shifts the CF flag into the most-significant bit and shifts the least-significant bit into the CF flag. For the ROL and ROR instructions, the original value of the CF flag is not a part of the result, but the CF flag receives a copy of the bit that was shifted from one end to the other.

The OF flag is defined only for the 1-bit rotates; it is undefined in all other cases. For left rotates, the OF flag is set to the exclusive OR of the CF bit (after the rotate) and the most-significant bit of the result. For right rotates, the OF flag is set to the exclusive OR of the two most-significant bits of the result.

Operation

```
SIZE ← OperandSize
CASE (determine count) OF
    SIZE = 8: tempCOUNT ← (COUNT AND 1FH) MOD 9;
    SIZE = 16: tempCOUNT ← (COUNT AND 1FH) MOD 17;
    SIZE = 32: tempCOUNT ← COUNT AND 1FH;
ESAC;
(* ROL instruction operation *)
WHILE (tempCOUNT ≠ 0)
    DO
        tempCF ← MSB(DEST);
        DEST ← (DEST ∗ 2) + tempCF;
        tempCOUNT ← tempCOUNT – 1;
    OD;
ELIHW;
CF ← tempCF;
IF COUNT = 1
    THEN OF ← MSB(DEST) XOR CF;
    ELSE OF is undefined;
FI;
(* ROR instruction operation *)
WHILE (tempCOUNT ≠ 0)
    DO
        tempCF ← LSB(SRC);
        DEST ← (DEST / 2) + (tempCF ∗ 2^SIZE);
    OD;
```
RCL/RCR/ROL/ROR—Rotate (Continued)

```
   tempCOUNT ← tempCOUNT − 1;
   OD;
   IF COUNT = 1
    THEN OF ← MSB(DEST) XOR MSB − 1(DEST);
    ELSE OF is undefined;
   FI;
   (* RCL instruction operation *)
   WHILE (tempCOUNT ≠ 0)
    DO
     tempCF ← MSB(DEST);
     DEST ← (DEST * 2) + tempCF;
     tempCOUNT ← tempCOUNT − 1;
    OD;
   EIHW;
   CF ← tempCF;
   IF COUNT = 1
    THEN OF ← MSB(DEST) XOR CF;
    ELSE OF is undefined;
   FI;
   (* RCR instruction operation *)
   WHILE (tempCOUNT ≠ 0)
    DO
     tempCF ← LSB(SRC);
     DEST ← (DEST / 2) + (tempCF * 2^{SIZE});
     tempCOUNT ← tempCOUNT − 1;
    OD;
   IF COUNT = 1
   IF COUNT = 1
    THEN OF ← MSB(DEST) XOR MSB − 1(DEST);
    ELSE OF is undefined;
   FI;
```

Flags Affected

The CF flag contains the value of the bit shifted into it. The OF flag is affected only for single-bit rotates (see “Description” above); it is undefined for multi-bit rotates. The SF, ZF, AF, and PF flags are not affected.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>NaT Register Consumption Abort.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>
RCL/RCR/ROL/ROR—Rotate (Continued)

Protected Mode Exceptions

#GP(0) If the source operand is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

Intel® Architecture Compatibility

The 8086 does not mask the rotation count. All Intel architecture processors from the Intel386™ processor on do mask the rotation count in all operating modes.
RDMSR—Read from Model Specific Register

### Description

Loads the contents of a 64-bit model specific register (MSR) specified in the ECX register into registers EDX:EAX. The EDX register is loaded with the high-order 32 bits of the MSR and the EAX register is loaded with the low-order 32 bits. If less than 64 bits are implemented in the MSR being read, the values returned to EDX:EAX in unimplemented bit locations are undefined.

This instruction must be executed at privilege level 0 or in real-address mode; otherwise, a general protection exception #GP(0) will be generated. Specifying a reserved or unimplemented MSR address in ECX will also cause a general protection exception.

The MSRs control functions for testability, execution tracing, performance-monitoring and machine check errors.

The CPUID instruction should be used to determine whether MSRs are supported (EDX[5]=1) before using this instruction.

See model specific instructions for all the MSRs that can be written to with this instruction and their addresses.

### Operation

If Itanium System Environment THEN IA-32_Intercept(INST,RDMSR);

EDX:EAX ← MSR(ECX);

### Flags Affected

None.

### Additional Itanium® System Environment Exceptions

IA-32_Intercept  Mandatory Instruction Intercept.

### Protected Mode Exceptions

#GP(0)  If the current privilege level is not 0.

If the value in ECX specifies a reserved or unimplemented MSR address.

### Real Address Mode Exceptions

#GP  If the current privilege level is not 0

If the value in ECX specifies a reserved or unimplemented MSR address.

### Virtual 8086 Mode Exceptions

#GP(0)  The RDMSR instruction is not recognized in virtual 8086 mode.
RDMSR—Read from Model Specific Register (Continued)

Intel® Architecture Compatibility

The MSRs and the ability to read them with the RDMSR instruction were introduced into the Intel architecture with the Pentium processor. Execution of this instruction by an Intel architecture processor earlier than the Pentium processor results in an invalid opcode exception #UD.
RDPMC—Read Performance-Monitoring Counters

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 33</td>
<td>RDPMC</td>
<td>Read performance-monitoring counter specified by ECX into EDX:EAX</td>
</tr>
</tbody>
</table>

**Description**

Loads the contents of the N-bit performance-monitoring counter specified in the ECX register into registers EDX:EAX. The EDX register is loaded with the high-order N-32 bits of the counter and the EAX register is loaded with the low-order 32 bits.

The RDPMC instruction allows application code running at a privilege level of 1, 2, or 3 to read the performance-monitoring counters if the PCE flag in the CR4 register is set for IA-32 System Environment operation or in the Itanium System Environment if the performance counters have been configured as user level counters. This instruction is provided to allow performance monitoring by application code without incurring the overhead of a call to an operating-system procedure.

The performance-monitoring counters are event counters that can be programmed to count events such as the number of instructions decoded, number of interrupts received, or number of cache loads.

The RDPMC instruction does not serialize instruction execution. That is, it does not imply that all the events caused by the preceding instructions have been completed or that events caused by subsequent instructions have not begun. If an exact event count is desired, software must use a serializing instruction (such as the CPUID instruction) before and/or after the execution of the RDPMC instruction.

The RDPMC instruction can execute in 16-bit addressing mode or virtual 8086 mode; however, the full contents of the ECX register are used to determine the counter to access and a full N-bit result is returned (the low-order 32 bits in the EAX register and the high-order N-32 bits in the EDX register).

**Operation**

IF (ECX ! Implemented Counters) THEN #GP(0)
IF (Itanium System Environment) THEN
SECURED = PSR.sp || CR4.pce==0;
IF ((PSR.cpl ==0) || (PSR.cpl!=0 && ~PMC[ECX].pm && ~SECURED))) THEN
    EDX:EAX ← PMD[ECX+4];
ELSE
    #GP(0)
FI;
ELSE
IF ((CR4.PCE = 1 OR ((CR4.PCE = 0 ) AND (CPL=0))) THEN
    EDX:EAX ← PMD[ECX+4];
ELSE (* CR4.PCE is 0 and CPL is 1, 2, or 3 *)
    #GP(0)
FI;
FI;
RDPMC—Read Performance-Monitoring Counters (Continued)

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults NaT Register Consumption Abort.

#GP(0) If the current privilege level is not 0 and the selected PMD register’s PM bit is 1, or if PSR.sp is 1.

Protected Mode Exceptions

#GP(0) If the current privilege level is not 0 and the PCE flag in the CR4 register is clear.
/*In IA-32 System Environment*/.
If the value in the ECX register does not match an implemented performance counter.

Real Address Mode Exceptions

#GP If the PCE flag in the CR4 register is clear. /*In the IA-32 System Environment*/.
If the value in the ECX register does not match an implemented performance counter.

Virtual 8086 Mode Exceptions

#GP(0) If the PCE flag in the CR4 register is clear. /*In the IA-32 System Environment*/.
If the value in the ECX register does not match an implemented performance counter.
RDTSC—Read Time-Stamp Counter

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 31</td>
<td>RDTSC</td>
<td>Read time-stamp counter into EDX:EAX</td>
</tr>
</tbody>
</table>

**Description**

Loads the current value of the processor’s time-stamp counter into the EDX:EAX registers. The time-stamp counter is contained in a 64-bit MSR. The high-order 32 bits of the MSR are loaded into the EDX register, and the low-order 32 bits are loaded into the EAX register. The processor increments the time-stamp counter MSR every clock cycle and resets it to 0 whenever the processor is reset.

In the IA-32 System Environment, the time stamp disable (TSD) flag in register CR4 restricts the use of the RDTSC instruction. When the TSD flag is clear, the RDTSC instruction can be executed at any privilege level; when the flag is set, the instruction can only be executed at privilege level 0. The time-stamp counter can also be read with the RDMSR instruction.

In the Itanium System Environment, PSR.si and CR4.TSD restricts the use of the RDTSC instruction. When PSR.si is clear and CR4.TSD is clear, the RDTSC instruction can be executed at any privilege level; when PSR.si is set or CR4.TSD is set, the instruction can only be executed at privilege level 0.

The RDTSC instruction is not serializing instruction. Thus, it does not necessarily wait until all previous instructions have been executed before reading the counter. Similarly, subsequent instructions may begin execution before the read operation is performed.

This instruction was introduced into the Intel architecture in the Pentium processor.

**Operation**

IF (IA-32 System Environment)
   IF (CR4.TSD = 0) OR ((CR4.TSD = 1) AND (CPL=0))
      THEN
         EDX:EAX ← TimeStampCounter;
         ELSE (* CR4 is 1 and CPL is 1, 2, or 3 *)
            #GP(0)
      FI;
   ELSE /*Itanium System Environment*/
      SECURED = PSR.si || CR4.TSD;
      IF (!SECURED) OR (SECURED AND (CPL=0))
         THEN
            EDX:EAX ← TimeStampCounter;
            ELSE (* CR4 is 1 and CPL is 1, 2, or 3 *)
               #GP(0)
         FI;
   FI;

**Flags Affected**

None.
RDTSC—Read Time-Stamp Counter (Continued)

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults               NaT Register Consumption Abort.

#GP(0)          If PSR.si is 1 or CR4.TSD is 1 and the CPL is greater than 0.

**Protected Mode Exceptions**

#GP(0)          If the TSD flag in register CR4 is set and the CPL is greater than 0.
/*For the IA-32 System Environment only*/

**Real Address Mode Exceptions**

#GP          If the TSD flag in register CR4 is set. /*For the IA-32 System Environment only*/

**Virtual 8086 Mode Exceptions**

#GP(0)          If the TSD flag in register CR4 is set. /*For the IA-32 System Environment only*/
REP/REPE/REPZ/REPNE/REPNZ—Repeat String Operation Prefix

<table>
<thead>
<tr>
<th>Prefix</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3 6C</td>
<td>REP INS r/m8, DX</td>
<td>Input ECX bytes from port DX into ES:[EDI]</td>
</tr>
<tr>
<td>F3 6D</td>
<td>REP INS r/m16,DX</td>
<td>Input ECX words from port DX into ES:[EDI]</td>
</tr>
<tr>
<td>F3 6D</td>
<td>REP INS r/m32,DX</td>
<td>Input ECX doublewords from port DX into ES:[EDI]</td>
</tr>
<tr>
<td>F3 A4</td>
<td>REP MOVS m8,m8</td>
<td>Move ECX bytes from DS:[ESI] to ES:[EDI]</td>
</tr>
<tr>
<td>F3 A5</td>
<td>REP MOVS m16,m16</td>
<td>Move ECX words from DS:[ESI] to ES:[EDI]</td>
</tr>
<tr>
<td>F3 A5</td>
<td>REP MOVS m32,m32</td>
<td>Move ECX doublewords from DS:[ESI] to ES:[EDI]</td>
</tr>
<tr>
<td>F3 6E</td>
<td>REP OUTS DX,r/m8</td>
<td>Output ECX bytes from DS:[ESI] to port DX</td>
</tr>
<tr>
<td>F3 6F</td>
<td>REP OUTS DX,r/m16</td>
<td>Output ECX words from DS:[ESI] to port DX</td>
</tr>
<tr>
<td>F3 6F</td>
<td>REP OUTS DX,r/m32</td>
<td>Output ECX doublewords from DS:[ESI] to port DX</td>
</tr>
<tr>
<td>F3 AC</td>
<td>REP LODS AL</td>
<td>Load ECX bytes from DS:[ESI] to AL</td>
</tr>
<tr>
<td>F3 AD</td>
<td>REP LODS AX</td>
<td>Load ECX words from DS:[ESI] to AX</td>
</tr>
<tr>
<td>F3 AD</td>
<td>REP LODS EAX</td>
<td>Load ECX doublewords from DS:[ESI] to EAX</td>
</tr>
<tr>
<td>F3 AA</td>
<td>REP STOS m8</td>
<td>Fill ECX bytes at ES:[EDI] with AL</td>
</tr>
<tr>
<td>F3 AB</td>
<td>REP STOS m16</td>
<td>Fill ECX words at ES:[EDI] with AX</td>
</tr>
<tr>
<td>F3 AB</td>
<td>REP STOS m32</td>
<td>Fill ECX doublewords at ES:[EDI] with EAX</td>
</tr>
<tr>
<td>F3 A6</td>
<td>REPE CMPS m8,m8</td>
<td>Find nonmatching bytes in ES:[EDI] and DS:[ESI]</td>
</tr>
<tr>
<td>F3 A7</td>
<td>REPE CMPS m16,m16</td>
<td>Find nonmatching words in ES:[EDI] and DS:[ESI]</td>
</tr>
<tr>
<td>F3 A7</td>
<td>REPE CMPS m32,m32</td>
<td>Find nonmatching doublewords in ES:[EDI] and DS:[ESI]</td>
</tr>
<tr>
<td>F3 AE</td>
<td>REPNE CMPS m8,m8</td>
<td>Find matching bytes in ES:[EDI] and DS:[ESI]</td>
</tr>
<tr>
<td>F3 AF</td>
<td>REPNE CMPS m16,m16</td>
<td>Find matching words in ES:[EDI] and DS:[ESI]</td>
</tr>
<tr>
<td>F3 AF</td>
<td>REPNE CMPS m32,m32</td>
<td>Find matching doublewords in ES:[EDI] and DS:[ESI]</td>
</tr>
<tr>
<td>F2 A6</td>
<td>REPNE SCAS m8,m8</td>
<td>Find AL, starting at ES:[EDI]</td>
</tr>
<tr>
<td>F2 A6</td>
<td>REPNE SCAS m16,m16</td>
<td>Find AX, starting at ES:[EDI]</td>
</tr>
<tr>
<td>F2 A6</td>
<td>REPNE SCAS m32,m32</td>
<td>Find EAX, starting at ES:[EDI]</td>
</tr>
</tbody>
</table>

Description

Repeats a string instruction the number of times specified in the count register (ECX) or until the indicated condition of the ZF flag is no longer met. The REP (repeat), REPE (repeat while equal), REPNE (repeat while not equal), REPZ (repeat while zero), and REPNZ (repeat while not zero) mnemonics are prefixes that can be added to one of the string instructions. The REP prefix can be added to the INS, OUTS, MOVS, LODS, and STOS instructions, and the REPE, REPNE, REPZ, and REPNZ prefixes can be added to the CMPS and SCAS instructions. (The REPZ and REPNZ prefixes are synonymous forms of the REPE and REPNE prefixes, respectively.) The behavior of the REP prefix is undefined when used with non-string instructions.

The REP prefixes apply only to one string instruction at a time. To repeat a block of instructions, use the LOOP instruction or another looping construct.
REP/REPE/REPZ/REPNE/REPNZ—Repeat String Operation Prefix
(Continued)

All of these repeat prefixes cause the associated instruction to be repeated until the count in register ECX is decremented to 0 (see the following table). The REPE, REPNE, REPZ, and REPNZ prefixes also check the state of the ZF flag after each iteration and terminate the repeat loop if the ZF flag is not in the specified state. When both termination conditions are tested, the cause of a repeat termination can be determined either by testing the ECX register with a JECXZ instruction or by testing the ZF flag with a JZ, JNZ, and JNE instruction.

<table>
<thead>
<tr>
<th>Repeat Prefix</th>
<th>Termination Condition 1</th>
<th>Termination Condition 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>REP</td>
<td>ECX=0</td>
<td>None</td>
</tr>
<tr>
<td>REPE/REPZ</td>
<td>ECX=0</td>
<td>ZF=0</td>
</tr>
<tr>
<td>REPNE/REPNZ</td>
<td>ECX=0</td>
<td>ZF=1</td>
</tr>
</tbody>
</table>

When the REPE/REPZ and REPNE/REPNZ prefixes are used, the ZF flag does not require initialization because both the CMPS and SCAS instructions affect the ZF flag according to the results of the comparisons they make.

A repeating string operation can be suspended by an exception or interrupt. When this happens, the state of the registers is preserved to allow the string operation to be resumed upon a return from the exception or interrupt handler. The source and destination registers point to the next string elements to be operated on, the EIP register points to the string instruction, and the ECX register has the value it held following the last successful iteration of the instruction. This mechanism allows long string operations to proceed without affecting the interrupt response time of the system.

When a page fault occurs during CMPS or SCAS instructions that are prefixed with REPNE, the EFLAGS value may NOT be restored to the state prior to the execution of the instruction. Since SCAS and CMPS do not use EFLAGS as an input, the processor can resume the instruction after the page fault handler.

Use the REP INS and REP OUTS instructions with caution. Not all I/O ports can handle the rate at which these instructions execute.

A REP STOS instruction is the fastest way to initialize a large block of memory.

Operation

```
IF AddressSize = 16
  THEN
    use CX for CountReg;
  ELSE (* AddressSize = 32 *)
    use ECX for CountReg;
FI;
WHILE CountReg ≠ 0
  DO
    service pending interrupts (if any);
    execute associated string instruction;
    CountReg ← CountReg − 1;
    IF CountReg = 0
      THEN exit WHILE loop
    FI;
```
REP/REPE/REPZ/REPNE/REPNZ—Repeat String Operation Prefix
(Continued)

IF (repeat prefix is REPZ or REPE) AND (ZF=0)
OR (repeat prefix is REPNZ or REPNE) AND (ZF=1)

THEN exit WHILE loop
FI;
OD;

Flags Affected

None; however, the CMPS and SCAS instructions do set the status flags in the EFLAGS register.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults    NaT Register Consumption Abort.

Itanium Mem Faults   VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB
                      Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data
                      Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data
                      Access Bit Fault, Data Dirty Bit Fault

Exceptions (All Operating Modes)

None; however, exceptions can be generated by the instruction a repeat prefix is associated with.
RET—Return from Procedure

Transfers program control to a return address located on the top of the stack. The address is usually placed on the stack by a CALL instruction, and the return is made to the instruction that follows the CALL instruction.

The optional source operand specifies the number of stack bytes to be released after the return address is popped; the default is none. This operand can be used to release parameters from the stack that were passed to the called procedure and are no longer needed.

The RET instruction can be used to execute three different types of returns:

- **Near return** – A return to a calling procedure within the current code segment (the segment currently pointed to by the CS register), sometimes referred to as an intrasegment return.
- **Far return** – A return to a calling procedure located in a different segment than the current code segment, sometimes referred to as an intersegment return.
- **Inter-privilege-level far return** – A far return to a different privilege level than that of the currently executing program or procedure.

The inter-privilege-level return type can only be executed in protected mode.

When executing a near return, the processor pops the return instruction pointer (offset) from the top of the procedure stack into the EIP register and begins program execution at the new instruction pointer. The CS register is unchanged.

When executing a far return, the processor pops the return instruction pointer from the top of the procedure stack into the EIP register, then pops the segment selector from the top of the stack into the CS register. The processor then begins program execution in the new code segment at the new instruction pointer.

The mechanics of an inter-privilege-level far return are similar to an intersegment return, except that the processor examines the privilege levels and access rights of the code and stack segments being returned to determine if the control transfer is allowed to be made. The DS, ES, FS, and GS segment registers are cleared by the RET instruction during an inter-privilege-level return if they refer to segments that are not allowed to be accessed at the new privilege level. Since a stack switch also occurs on an inter-privilege level return, the ESP and SS registers are loaded from the stack.

### Opcode Instruction Description

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>C3</td>
<td>RET</td>
<td>Near return to calling procedure</td>
</tr>
<tr>
<td>CB</td>
<td>RET</td>
<td>Far return to calling procedure</td>
</tr>
<tr>
<td>C2 iw</td>
<td>RET imm16</td>
<td>Near return to calling procedure and pop imm16 bytes from stack</td>
</tr>
<tr>
<td>CA iw</td>
<td>RET imm16</td>
<td>Far return to calling procedure and pop imm16 bytes from stack</td>
</tr>
</tbody>
</table>
RET—Return from Procedure (Continued)

Operation

(* Near return *)
IF instruction = near return
THEN;
   IF OperandSize = 32
      THEN
         IF top 12 bytes of stack not within stack limits THEN #SS(0); FI;
         EIP ← Pop();
      ELSE (* OperandSize = 16 *)
         IF top 6 bytes of stack not within stack limits
            THEN #SS(0)
            FI;
         tempEIP ← Pop();
         tempEIP ← tempEIP AND 0000FFFFH;
         IF tempEIP not within code segment limits THEN #GP(0); FI;
         EIP ← tempEIP;
      FI;
   IF instruction has immediate operand
      THEN IF StackAddressSize=32
         THEN
            ESP ← ESP + SRC;
         ELSE (* StackAddressSize=16 *)
            SP ← SP + SRC;
         FI;
      FI;
      IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug); FI;
   FI;
(* Real-address mode or virtual-8086 mode *)
IF ((PE = 0) OR (PE = 1 AND VM = 1)) AND instruction = far return
THEN;
   IF OperandSize = 32
      THEN
         IF top 12 bytes of stack not within stack limits THEN #SS(0); FI;
         EIP ← Pop();
         CS ← Pop(); (* 32-bit pop, high-order 16-bits discarded *)
      ELSE (* OperandSize = 16 *)
         IF top 6 bytes of stack not within stack limits THEN #SS(0); FI;
         tempEIP ← Pop();
         tempEIP ← tempEIP AND 0000FFFFH;
         IF tempEIP not within code segment limits THEN #GP(0); FI;
         EIP ← tempEIP;
         CS ← Pop(); (* 16-bit pop *)
      FI;
      IF instruction has immediate operand THEN SP ← SP + (SRC AND FFFFH); FI;
      IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug); FI;
   FI;
(* Protected mode, not virtual 8086 mode *)
IF (PE = 1 AND VM = 0) AND instruction = far RET
THEN
   IF OperandSize = 32
      THEN
RET—Return from Procedure (Continued)

IF second doubleword on stack is not within stack limits THEN #SS(0); FI;
ELSE (* OperandSize = 16 *)
    IF second word on stack is not within stack limits THEN #SS(0); FI;
    FI;
IF return code segment selector is null THEN GP(0); FI;
IF return code segment selector addresses descriptor beyond descriptor table limit
    THEN GP(selector); FI;
Obtain descriptor to which return code segment selector points from descriptor table
IF return code segment descriptor is not a code segment THEN #GP(selector); FI;
if return code segment selector RPL < CPL THEN #GP(selector); FI;
IF return code segment descriptor is conforming
    AND return code segment DPL > return code segment selector RPL
    THEN #GP(selector); FI;
IF return code segment descriptor is not present THEN #NP(selector); FI;
IF return code segment selector RPL > CPL
    THEN GOTO RETURN-OUTER-PRIVILEGE-LEVEL;
ELSE GOTO RETURN-TO-SAME-PRIVILEGE-LEVEL
FI;
END;FI;

RETURN-SAME-PRIVILEGE-LEVEL:
IF the return instruction pointer is not within the return code segment limit
    THEN #GP(0);
FI;
IF OperandSize=32
    THEN
        EIP ← Pop();
        CS ← Pop(); (* 32-bit pop, high-order 16-bits discarded *)
        ESP ← ESP + SRC;
    ELSE (* OperandSize=16 *)
        EIP ← Pop();
        EIP ← EIP AND 0000FFFFH;
        CS ← Pop(); (* 16-bit pop *)
        ESP ← ESP + SRC;
    FI;
IF Itanium System Environment AND PSR.tb THEN IA-32_Exception(Debug);

RETURN-OUTER-PRIVILEGE-LEVEL:
IF top (16 + SRC) bytes of stack are not within stack limits (OperandSize=32)
    OR top (8 + SRC) bytes of stack are not within stack limits (OperandSize=16)
    THEN #SS(0); FI;
FI;
Read return segment selector;
IF stack segment selector is null THEN #GP(0); FI;
IF return stack segment selector index is not within its descriptor table limits
    THEN #GP(selector); FI;
Read segment descriptor pointed to by return segment selector;
IF stack segment selector RPL ≠ RPL of the return code segment selector
    OR stack segment is not a writable data segment
    OR stack segment descriptor DPL ≠ RPL of the return code segment selector
    THEN #GP(selector); FI;
IF stack segment not present THEN #SS(StackSegmentSelector); FI;
RET—Return from Procedure (Continued)

IF the return instruction pointer is not within the return code segment limit THEN #GP(0); FI:
CPL ← ReturnCodeSegmentSelector(RPL);
IF OperandSize=32
    THEN
      EIP ← Pop();
      CS ← Pop(); (* 32-bit pop, high-order 16-bits discarded *)
      (* segment descriptor information also loaded *)
      CS(RPL) ← CPL;
      ESP ← ESP + SRC;
      tempESP ← Pop();
      tempSS ← Pop(); (* 32-bit pop, high-order 16-bits discarded *)
      (* segment descriptor information also loaded *)
      ESP ← tempESP;
      SS ← tempSS;
    ELSE (* OperandSize=16 *)
      EIP ← Pop();
      EIP ← EIP AND 0000FFFFH;
      CS ← Pop(); (* 16-bit pop; segment descriptor information also loaded *)
      CS(RPL) ← CPL;
      ESP ← ESP + SRC;
      tempESP ← Pop();
      tempSS ← Pop(); (* 16-bit pop; segment descriptor information also loaded *)
      (* segment descriptor information also loaded *)
      ESP ← tempESP;
      SS ← tempSS;
    FI;
FOR each of segment register (ES, FS, GS, and DS)
  DO:
    IF segment register points to data or non-conforming code segment
    AND CPL > segment descriptor DPL; (* DPL in hidden part of segment register *)
    THEN (* segment register invalid *)
      SegmentSelector/Descriptor ← 0; (* null segment selector *)
    FI;
  OD;
For each of ES, FS, GS, and DS
DO
  IF segment descriptor indicates the segment is not a data or readable code segment
  OR if the segment is a data or non-conforming code segment and the segment
  descriptor's DPL < CPL or RPL of code segment's segment selector
  THEN
    segment selector register ← null selector;
  OD;

Flags Affected

None.
RET—Return from Procedure  (Continued)

**Additional Itanium® System Environment Exceptions**
- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
- **IA-32_Exception**: Taken Branch Debug Exception if PSR.tb is 1

**Protected Mode Exceptions**
- **#GP(0)**: If the return code or stack segment selector null.
- **#GP(selector)**: If the return instruction pointer is not within the return code segment limit.
- **#GP(selector)**: If the RPL of the return code segment selector is less than the CPL.
- **#GP(selector)**: If the return code or stack segment selector index is not within its descriptor table limits.
- **#GP(selector)**: If the return code segment descriptor does not indicate a code segment.
- **#GP(selector)**: If the return code segment is non-conforming and the segment selector’s DPL is not equal to the RPL of the code segment’s segment selector.
- **#GP(selector)**: If the return code segment is conforming and the segment selector’s DPL greater than the RPL of the code segment’s segment selector.
- **#GP(selector)**: If the stack segment is not a writable data segment.
- **#GP(selector)**: If the return code segment selector RPL is not equal to the RPL of the return code segment selector.
- **#GP(selector)**: If the stack segment descriptor DPL is not equal to the RPL of the return code segment selector.
- **#SS(0)**: If the top bytes of stack are not within stack limits.
- **#SS(0)**: If the return stack segment is not present.
- **#NP(selector)**: If the return code segment is not present.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If an unaligned memory access occurs when the CPL is 3 and alignment checking is enabled.

**Real Address Mode Exceptions**
- **#GP**: If the return instruction pointer is not within the return code segment limit.
- **#SS**: If the top bytes of stack are not within stack limits.

**Virtual 8086 Mode Exceptions**
- **#GP(0)**: If the return instruction pointer is not within the return code segment limit.
- **#SS(0)**: If the top bytes of stack are not within stack limits.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If an unaligned memory access occurs when alignment checking is enabled.
ROL/ROR—Rotate

See entry for RCL/RCR/ROL/ROR.
RSM—Resume from System Management Mode

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AA</td>
<td>RSM</td>
<td>Resume operation of interrupted program</td>
</tr>
</tbody>
</table>

**Description**

Returns program control from system management mode (SMM) to the application program or operating system procedure that was interrupted when the processor received an SSM interrupt. The processor’s state is restored from the dump created upon entering SMM. If the processor detects invalid state information during state restoration, it enters the shutdown state. The following invalid information can cause a shutdown:

- Any reserved bit of CR4 is set to 1.
- Any illegal combination of bits in CR0, such as (PG=1 and PE=0) or (NW=1 and CD=0).
- (Intel Pentium and Intel486 only.) The value stored in the state dump base field is not a 32-KByte aligned address.

The contents of the model-specific registers are not affected by a return from SMM.

See Chapter 9 in the *IA-32 Intel® Architecture Software Developer’s Manual, Volume 3* for more information about SMM and the behavior of the RSM instruction.

**Operation**

```plaintext
IF Itanium System Environment THEN IA-32_Intercept(INST,RSM);
ReturnFromSSM;
ProcessorState ← Restore(SSMDump);
```

**Flags Affected**

All.

**Additional Itanium® System Environment Exceptions**

IA-32_Intercept Mandatory Instruction Intercept.

**Protected Mode Exceptions**

- **#UD** If an attempt is made to execute this instruction when the processor is not in SMM.

**Real Address Mode Exceptions**

- **#UD** If an attempt is made to execute this instruction when the processor is not in SMM.

**Virtual 8086 Mode Exceptions**

- **#UD** If an attempt is made to execute this instruction when the processor is not in SMM.
SAHF—Store AH into Flags

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Clocks</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9E</td>
<td>SAHF</td>
<td>2</td>
<td>Loads SF, ZF, AF, PF, and CF from AH into EFLAGS register</td>
</tr>
</tbody>
</table>

**Description**

Loads the SF, ZF, AF, PF, and CF flags of the EFLAGS register with values from the corresponding bits in the AH register (bits 7, 6, 4, 2, and 0, respectively). Bits 1, 3, and 5 of register AH are ignored; the corresponding reserved bits (1, 3, and 5) in the EFLAGS registers are set as shown in the “Operation” below.

**Operation**

\[ \text{EFLAGS(SF:ZF:AF:PF:CF)} \gets \text{AH}; \]

**Flags Affected**

The SF, ZF, AF, PF, and CF flags are loaded with values from the AH register. Bits 1, 3, and 5 of the EFLAGS register are set to 1, 0, and 0, respectively.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults  NaT Register Consumption Abort.

**Exceptions (All Operating Modes)**

None.
### SAL/SAR/SHL/SHR—Shift Instructions

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D0 /4</td>
<td>SAL r/m8,1</td>
<td>Multiply r/m8 by 2, once</td>
</tr>
<tr>
<td>D2 /4</td>
<td>SAL r/m8,CL</td>
<td>Multiply r/m8 by 2, CL times</td>
</tr>
<tr>
<td>C0 /4 ib</td>
<td>SAL r/m8,imm8</td>
<td>Multiply r/m8 by 2, imm8 times</td>
</tr>
<tr>
<td>D1 /4</td>
<td>SAL r/m16,1</td>
<td>Multiply r/m16 by 2, once</td>
</tr>
<tr>
<td>D3 /4</td>
<td>SAL r/m16,CL</td>
<td>Multiply r/m16 by 2, CL times</td>
</tr>
<tr>
<td>C1 /4 ib</td>
<td>SAL r/m16,imm8</td>
<td>Multiply r/m16 by 2, imm8 times</td>
</tr>
<tr>
<td>D1 /4</td>
<td>SAL r/m32,1</td>
<td>Multiply r/m32 by 2, once</td>
</tr>
<tr>
<td>D3 /4</td>
<td>SAL r/m32,CL</td>
<td>Multiply r/m32 by 2, CL times</td>
</tr>
<tr>
<td>C1 /4 ib</td>
<td>SAL r/m32,imm8</td>
<td>Multiply r/m32 by 2, imm8 times</td>
</tr>
<tr>
<td>D0 /7</td>
<td>SAR r/m8,1</td>
<td>Signed divide* r/m8 by 2, once</td>
</tr>
<tr>
<td>D2 /7</td>
<td>SAR r/m8,CL</td>
<td>Signed divide* r/m8 by 2, CL times</td>
</tr>
<tr>
<td>C0 /7 ib</td>
<td>SAR r/m8,imm8</td>
<td>Signed divide* r/m8 by 2, imm8 times</td>
</tr>
<tr>
<td>D1 /7</td>
<td>SAR r/m16,1</td>
<td>Signed divide* r/m16 by 2, once</td>
</tr>
<tr>
<td>D3 /7</td>
<td>SAR r/m16,CL</td>
<td>Signed divide* r/m16 by 2, CL times</td>
</tr>
<tr>
<td>C1 /7 ib</td>
<td>SAR r/m16,imm8</td>
<td>Signed divide* r/m16 by 2, imm8 times</td>
</tr>
<tr>
<td>D1 /7</td>
<td>SAR r/m32,1</td>
<td>Signed divide* r/m32 by 2, once</td>
</tr>
<tr>
<td>D3 /7</td>
<td>SAR r/m32,CL</td>
<td>Signed divide* r/m32 by 2, CL times</td>
</tr>
<tr>
<td>C1 /7 ib</td>
<td>SAR r/m32,imm8</td>
<td>Signed divide* r/m32 by 2, imm8 times</td>
</tr>
<tr>
<td>D0 /4</td>
<td>SHL r/m8,1</td>
<td>Multiply r/m8 by 2, once</td>
</tr>
<tr>
<td>D2 /4</td>
<td>SHL r/m8,CL</td>
<td>Multiply r/m8 by 2, CL times</td>
</tr>
<tr>
<td>C0 /4 ib</td>
<td>SHL r/m8,imm8</td>
<td>Multiply r/m8 by 2, imm8 times</td>
</tr>
<tr>
<td>D1 /4</td>
<td>SHL r/m16,1</td>
<td>Multiply r/m16 by 2, once</td>
</tr>
<tr>
<td>D3 /4</td>
<td>SHL r/m16,CL</td>
<td>Multiply r/m16 by 2, CL times</td>
</tr>
<tr>
<td>C1 /4 ib</td>
<td>SHL r/m16,imm8</td>
<td>Multiply r/m16 by 2, imm8 times</td>
</tr>
<tr>
<td>D1 /4</td>
<td>SHL r/m32,1</td>
<td>Multiply r/m32 by 2, once</td>
</tr>
<tr>
<td>D3 /4</td>
<td>SHL r/m32,CL</td>
<td>Multiply r/m32 by 2, CL times</td>
</tr>
<tr>
<td>C1 /4 ib</td>
<td>SHL r/m32,imm8</td>
<td>Multiply r/m32 by 2, imm8 times</td>
</tr>
<tr>
<td>D0 /5</td>
<td>SHR r/m8,1</td>
<td>Unsigned divide r/m8 by 2, once</td>
</tr>
<tr>
<td>D2 /5</td>
<td>SHR r/m8,CL</td>
<td>Unsigned divide r/m8 by 2, CL times</td>
</tr>
<tr>
<td>C0 /5 ib</td>
<td>SHR r/m8,imm8</td>
<td>Unsigned divide r/m8 by 2, imm8 times</td>
</tr>
<tr>
<td>D1 /5</td>
<td>SHR r/m16,1</td>
<td>Unsigned divide r/m16 by 2, once</td>
</tr>
<tr>
<td>D3 /5</td>
<td>SHR r/m16,CL</td>
<td>Unsigned divide r/m16 by 2, CL times</td>
</tr>
<tr>
<td>C1 /5 ib</td>
<td>SHR r/m16,imm8</td>
<td>Unsigned divide r/m16 by 2, imm8 times</td>
</tr>
<tr>
<td>D1 /5</td>
<td>SHR r/m32,1</td>
<td>Unsigned divide r/m32 by 2, once</td>
</tr>
<tr>
<td>D3 /5</td>
<td>SHR r/m32,CL</td>
<td>Unsigned divide r/m32 by 2, CL times</td>
</tr>
<tr>
<td>C1 /5 ib</td>
<td>SHR r/m32,imm8</td>
<td>Unsigned divide r/m32 by 2, imm8 times</td>
</tr>
</tbody>
</table>

**Note:**

* Not the same form of division as IDIV; rounding is toward negative infinity.
SAL/SAR/SHL/SHR—Shift Instructions (Continued)

Description
Shift the bits in the first operand (destination operand) to the left or right by the number of bits specified in the second operand (count operand). Bits shifted beyond the destination operand boundary are first shifted into the CF flag, then discarded. At the end of the shift operation, the CF flag contains the last bit shifted out of the destination operand.

The destination operand can be a register or a memory location. The count operand can be an immediate value or register CL. The count is masked to 5 bits, which limits the count range to from 0 to 31. A special opcode encoding is provide for a count of 1.

The shift arithmetic left (SAL) and shift logical left (SHL) instructions perform the same operation; they shift the bits in the destination operand to the left (toward more significant bit locations). For each shift count, the most significant bit of the destination operand is shifted into the CF flag, and the least significant bit is cleared.

The shift arithmetic right (SAR) and shift logical right (SHR) instructions shift the bits of the destination operand to the right (toward less significant bit locations). For each shift count, the least significant bit of the destination operand is shifted into the CF flag, and the most significant bit is either set or cleared depending on the instruction type. The SHR instruction clears the most significant bit; the SAR instruction sets or clears the most significant bit to correspond to the sign (most significant bit) of the original value in the destination operand. In effect, the SAR instruction fills the empty bit position’s shifted value with the sign of the unshifted value.

The SAR and SHR instructions can be used to perform signed or unsigned division, respectively, of the destination operand by powers of 2. For example, using the SAR instruction shift a signed integer 1 bit to the right divides the value by 2.

Using the SAR instruction to perform a division operation does not produce the same result as the IDIV instruction. The quotient from the IDIV instruction is rounded toward zero, whereas the “quotient” of the SAR instruction is rounded toward negative infinity. This difference is apparent only for negative numbers. For example, when the IDIV instruction is used to divide -9 by 4, the result is -2 with a remainder of -1. If the SAR instruction is used to shift -9 right by two bits, the result is -3 and the “remainder” is +3; however, the SAR instruction stores only the most significant bit of the remainder (in the CF flag).

The OF flag is affected only on 1-bit shifts. For left shifts, the OF flag is cleared to 0 if the most-significant bit of the result is the same as the CF flag (that is, the top two bits of the original operand were the same); otherwise, it is set to 1. For the SAR instruction, the OF flag is cleared for all 1-bit shifts. For the SHR instruction, the OF flag is set to the most-significant bit of the original operand.

Operation
\[
\text{tempCOUNT} \leftarrow \text{COUNT}; \\
\text{tempDEST} \leftarrow \text{DEST}; \\
\text{WHILE} (\text{tempCOUNT} \neq 0) \\
\text{DO} \\
\quad \text{IF instruction is SAL or SHL} \\
\quad \quad \text{THEN} \\
\quad \quad \quad \text{CF} \leftarrow \text{MSB(DEST)};
\]
SAL/SAR/SHL/SHR—Shift Instructions (Continued)

ELSE (* instruction is SAR or SHR *)
    CF ← LSB(DEST);
FI;
IF instruction is SAL or SHL
    THEN
        DEST ← DEST * 2;
    ELSE
        IF instruction is SAR
            THEN
                DEST ← DEST / 2 (*Signed divide, rounding toward negative infinity*);
            ELSE (* instruction is SHR *)
                DEST ← DEST / 2 ; (* Unsigned divide *);
            FI;
        FI;
        temp ← temp – 1;
    OD;
(* Determine overflow for the various instructions *)
IF COUNT = 1
    THEN
        IF instruction is SAL or SHL
            THEN
                OF ← MSB(DEST) XOR CF;
            ELSE
                IF instruction is SAR
                    THEN
                        OF ← 0;
                    ELSE (* instruction is SHR *)
                        OF ← MSB(tempDEST);
                    FI;
                FI;
        ELSE
            OF ← undefined;
        FI;
FI;

Flags Affected

The CF flag contains the value of the last bit shifted out of the destination operand; it is undefined for SHL and SHR instructions count is greater than or equal to the size of the destination operand. The OF flag is affected only for 1-bit shifts (see “Description” above); otherwise, it is undefined. The SF, ZF, and PF flags are set according to the result. If the count is 0, the flags are not affected.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
SAL/SAR/SHL/SHR—Shift Instructions (Continued)

Protected Mode Exceptions

#GP(0)  If the destination is located in a nonwritable segment.
        If a memory operand effective address is outside the CS, DS, ES, FS, or GS
        segment limit.
        If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made
        while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
     segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
        segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.

Intel® Architecture Compatibility

The 8086 does not mask the shift count. All Intel architecture processors from the Intel386
processor on do mask the rotation count in all operating modes.
SBB—Integer Subtraction with Borrow

### Description

Adds the source operand (second operand) and the carry (CF) flag, and subtracts the result from the destination operand (first operand). The result of the subtraction is stored in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location. The state of the CF flag represents a borrow from a previous subtraction.

When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The SBB instruction does not distinguish between signed or unsigned operands. Instead, the processor evaluates the result for both data types and sets the OF and CF flags to indicate a borrow in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

The SBB instruction is usually executed as part of a multibyte or multiword subtraction in which a SUB instruction is followed by a SBB instruction.

### Operation

\[
\text{DEST} \leftarrow \text{DEST} - (\text{SRC} + \text{CF});
\]

### Flags Affected

The OF, SF, ZF, AF, PF, and CF flags are set according to the result.

### Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1C ib</td>
<td>SBB AL,imm8</td>
<td>Subtract with borrow imm8 from AL</td>
</tr>
<tr>
<td>1D iw</td>
<td>SBB AX,imm16</td>
<td>Subtract with borrow imm16 from AX</td>
</tr>
<tr>
<td>1D id</td>
<td>SBB EAX,imm32</td>
<td>Subtract with borrow imm32 from EAX</td>
</tr>
<tr>
<td>80 /3 ib</td>
<td>SBB r/m8,imm8</td>
<td>Subtract with borrow imm8 from r/m8</td>
</tr>
<tr>
<td>81 /3 iw</td>
<td>SBB r/m16,imm16</td>
<td>Subtract with borrow imm16 from r/m16</td>
</tr>
<tr>
<td>81 /3 id</td>
<td>SBB r/m32,imm32</td>
<td>Subtract with borrow imm32 from r/m32</td>
</tr>
<tr>
<td>83 /3 ib</td>
<td>SBB r/m16,imm8</td>
<td>Subtract with borrow sign-extended imm8 from r/m16</td>
</tr>
<tr>
<td>83 /3 ib</td>
<td>SBB r/m32,imm8</td>
<td>Subtract with borrow sign-extended imm8 from r/m32</td>
</tr>
<tr>
<td>18 r</td>
<td>SBB r/m8,r8</td>
<td>Subtract with borrow r8 from r/m8</td>
</tr>
<tr>
<td>19 r</td>
<td>SBB r/m16,r16</td>
<td>Subtract with borrow r16 from r/m16</td>
</tr>
<tr>
<td>19 r</td>
<td>SBB r/m32,r32</td>
<td>Subtract with borrow r32 from r/m32</td>
</tr>
<tr>
<td>1A r</td>
<td>SBB r8,r/m8</td>
<td>Subtract with borrow r/m8 from r8</td>
</tr>
<tr>
<td>1B r</td>
<td>SBB r16,r/m16</td>
<td>Subtract with borrow r/m16 from r16</td>
</tr>
<tr>
<td>1B r</td>
<td>SBB r32,r/m32</td>
<td>Subtract with borrow r/m32 from r32</td>
</tr>
</tbody>
</table>
SBB—Integer Subtraction with Borrow (Continued)

Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If the destination is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
SCAS/SCASB/SCASW/SCASD—Scan String Data

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AE</td>
<td>SCAS ES:(E)DI</td>
<td>Compare AL with byte at ES:(E)DI and set status flags</td>
</tr>
<tr>
<td>AF</td>
<td>SCAS ES:DI</td>
<td>Compare AX with word at ES:DI and set status flags</td>
</tr>
<tr>
<td>AF</td>
<td>SCAS ES:EDI</td>
<td>Compare EAX with doubleword at ES:EDI and set status flags</td>
</tr>
<tr>
<td>AE</td>
<td>SCASB</td>
<td>Compare AL with byte at ES:(E)DI and set status flags</td>
</tr>
<tr>
<td>AF</td>
<td>SCASW</td>
<td>Compare AX with word at ES:DI and set status flags</td>
</tr>
<tr>
<td>AF</td>
<td>SCASD</td>
<td>Compare EAX with doubleword at ES:EDI and set status flags</td>
</tr>
</tbody>
</table>

Description

Compress the byte, word, or double word specified with the source operand with the value in the AL, AX, or EAX register, respectively, and sets the status flags in the EFLAGS register according to the results. The source operand specifies the memory location at the address ES:EDI. (When the operand-size attribute is 16, the DI register is used as the source-index register.) The ES segment cannot be overridden with a segment override prefix.

The SCASB, SCASW, and SCASD mnemonics are synonyms of the byte, word, and doubleword versions of the SCAS instructions. They are simpler to use, but provide no type or segment checking. (For the SCAS instruction, “ES:EDI” must be explicitly specified in the instruction.)

After the comparison, the EDI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the EDI register is incremented; if the DF flag is 1, the EDI register is decremented.) The EDI register is incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The SCAS, SCASB, SCASW, and SCASD instructions can be preceded by the REP prefix for block comparisons of ECX bytes, words, or doublewords. More often, however, these instructions will be used in a LOOP construct that takes some action based on the setting of the status flags before the next comparison is made. See “REP/REPE/REPZ/REPNE/REPNZ—Repeat String Operation Prefix” on page 3:685 for a description of the REP prefix.

Operation

IF (byte comparison)
THEN
  temp ← AL − SRC;
  SetStatusFlags(temp);
  THEN IF DF = 0
  THEN (E)DI ← 1;
  ELSE (E)DI ← −1;
  FI;
ELSE IF (word comparison)
THEN
  temp ← AX − SRC;
  SetStatusFlags(temp)
  THEN IF DF = 0
SCAS/SCASB/SCASW/SCASD—Scan String Data (Continued)

THEN DI ← 2;
ELSE DI ← –2;
FI;
ELSE (* doubleword comparison *)
temp ← EAX – SRC;
SetStatusFlags(temp)
THEN IF DF = 0
THEN EDI ← 4;
ELSE EDI ← −4;
FI;
FI;

Flags Affected

The OF, SF, ZF, AF, PF, and CF flags are set according to the temporary result of the comparison.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults      NaT Register Consumption Abort.
Itanium Mem Faults      VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)     If a memory operand effective address is outside the limit of the ES segment.
If the ES register contains a null segment selector.
If an illegal memory operand effective address in the ES segment is given.

#PF(fault-code) If a page fault occurs.

#AC(0)     If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP     If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS     If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0)     If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0)     If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0)     If alignment checking is enabled and an unaligned memory reference is made.
SETcc—Set Byte on Condition

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 97</td>
<td>SETA r/m8</td>
<td>Set byte if above (CF=0 and ZF=0)</td>
</tr>
<tr>
<td>0F 93</td>
<td>SETAE r/m8</td>
<td>Set byte if above or equal (CF=0)</td>
</tr>
<tr>
<td>0F 92</td>
<td>SETB r/m8</td>
<td>Set byte if below (CF=1)</td>
</tr>
<tr>
<td>0F 96</td>
<td>SETBE r/m8</td>
<td>Set byte if below or equal (CF=1 or (ZF=1)</td>
</tr>
<tr>
<td>0F 92</td>
<td>SETC r/m8</td>
<td>Set if carry (CF=1)</td>
</tr>
<tr>
<td>0F 94</td>
<td>SETE r/m8</td>
<td>Set byte if equal (ZF=1)</td>
</tr>
<tr>
<td>0F 9F</td>
<td>SETG r/m8</td>
<td>Set byte if greater (ZF=0 and SF=OF)</td>
</tr>
<tr>
<td>0F 9D</td>
<td>SETGE r/m8</td>
<td>Set byte if greater or equal (SF=OF)</td>
</tr>
<tr>
<td>0F 9C</td>
<td>SETL r/m8</td>
<td>Set byte if less (SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 9E</td>
<td>SETLE r/m8</td>
<td>Set byte if less or equal (ZF=1 or SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 96</td>
<td>SETNA r/m8</td>
<td>Set byte if not above (CF=1 or ZF=1)</td>
</tr>
<tr>
<td>0F 92</td>
<td>SETNAE r/m8</td>
<td>Set byte if not above or equal (CF=1)</td>
</tr>
<tr>
<td>0F 93</td>
<td>SETNB r/m8</td>
<td>Set byte if not below (CF=0)</td>
</tr>
<tr>
<td>0F 97</td>
<td>SETNBE r/m8</td>
<td>Set byte if not below or equal (CF=0 and ZF=0)</td>
</tr>
<tr>
<td>0F 93</td>
<td>SETNC r/m8</td>
<td>Set byte if not carry (CF=0)</td>
</tr>
<tr>
<td>0F 95</td>
<td>SETNE r/m8</td>
<td>Set byte if not equal (ZF=0)</td>
</tr>
<tr>
<td>0F 9E</td>
<td>SETNG r/m8</td>
<td>Set byte if not greater (ZF=0 or SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 9C</td>
<td>SETNGE r/m8</td>
<td>Set byte if not greater or equal (SF&lt;&gt;OF)</td>
</tr>
<tr>
<td>0F 9D</td>
<td>SETNL r/m8</td>
<td>Set byte if not less (SF=OF)</td>
</tr>
<tr>
<td>0F 9F</td>
<td>SETNLE r/m8</td>
<td>Set byte if not less or equal (ZF=0 and SF=OF)</td>
</tr>
<tr>
<td>0F 91</td>
<td>SETNO r/m8</td>
<td>Set byte if not overflow (OF=0)</td>
</tr>
<tr>
<td>0F 9B</td>
<td>SETNP r/m8</td>
<td>Set byte if not parity (PF=0)</td>
</tr>
<tr>
<td>0F 99</td>
<td>SETNS r/m8</td>
<td>Set byte if not sign (SF=0)</td>
</tr>
<tr>
<td>0F 95</td>
<td>SETNZ r/m8</td>
<td>Set byte if not zero (ZF=0)</td>
</tr>
<tr>
<td>0F 90</td>
<td>SETO r/m8</td>
<td>Set byte if overflow (OF=1)</td>
</tr>
<tr>
<td>0F 9A</td>
<td>SETP r/m8</td>
<td>Set byte if parity (PF=1)</td>
</tr>
<tr>
<td>0F 9A</td>
<td>SETPE r/m8</td>
<td>Set byte if parity even (PF=1)</td>
</tr>
<tr>
<td>0F 9B</td>
<td>SETPO r/m8</td>
<td>Set byte if parity odd (PF=0)</td>
</tr>
<tr>
<td>0F 98</td>
<td>SETS r/m8</td>
<td>Set byte if sign (SF=1)</td>
</tr>
<tr>
<td>0F 94</td>
<td>SETZ r/m8</td>
<td>Set byte if zero (ZF=1)</td>
</tr>
</tbody>
</table>

**Description**

Set the destination operand to the value 0 or 1, depending on the settings of the status flags (CF, SF, OF, ZF, and PF) in the EFLAGS register. The destination operand points to a byte register or a byte in memory. The condition code suffix \(cc\) indicates the condition being tested for.

The terms “above” and “below” are associated with the CF flag and refer to the relationship between two unsigned integer values. The terms “greater” and “less” are associated with the SF and OF flags and refer to the relationship between two signed integer values.
SETcc—Set Byte on Condition (Continued)

Many of the SETcc instruction opcodes have alternate mnemonics. For example, the SETG (set byte if greater) and SETNLE (set if not less or equal) both have the same opcode and test for the same condition: ZF equals 0 and SF equals OF. These alternate mnemonics are provided to make code more intelligible.

Some languages represent a logical one as an integer with all bits set. This representation can be arrived at by choosing the mutually exclusive condition for the SETcc instruction, then decrementing the result. For example, to test for overflow, use the SETNO instruction, then decrement the result.

Operation

IF condition
   THEN DEST ← 1
   ELSE DEST ← 0;
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If the destination is located in a nonwritable segment.
   If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.
SETcc—Set Byte on Condition (Continued)

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
SGDT/SIDT—Store Global/Interrupt Descriptor Table Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 /0</td>
<td>SGDT m</td>
<td>Store GDTR to m</td>
</tr>
<tr>
<td>0F 01 /1</td>
<td>SIDT m</td>
<td>Store IDTR to m</td>
</tr>
</tbody>
</table>

Description

Stores the contents of the global descriptor table register (GDTR) or the interrupt descriptor table register (IDTR) in the destination operand. The destination operand is a pointer to 6-byte memory location. If the operand-size attribute is 32 bits, the 16-bit limit field of the register is stored in the lower 2 bytes of the memory location and the 32-bit base address is stored in the upper 4 bytes. If the operand-size attribute is 16 bits, the limit is stored in the lower 2 bytes and the 24-bit base address is stored in the third, fourth, and fifth byte, with the sixth byte filled with 0s.

The SGDT and SIDT instructions are useful only in operating-system software; however, they can be used in application programs.

Operation

IF Itanium System Environment THEN IA-32_Intercept(INST,SGDT/SIDT);

IF instruction is IDTR THEN
  IF OperandSize = 16 THEN
    DEST[0:15] ← IDTR(Limit);
    DEST[16:39] ← IDTR(Base); (* 24 bits of base address loaded; *)
    DEST[40:47] ← 0;
  ELSE (* 32-bit Operand Size *)
    DEST[0:15] ← IDTR(Limit);
    DEST[16:47] ← IDTR(Base); (* full 32-bit base address loaded *)
  FI;
ELSE (* instruction is SGDT *)
  IF OperandSize = 16 THEN
    DEST[0:15] ← GDTR(Limit);
    DEST[16:39] ← GDTR(Base); (* 24 bits of base address loaded; *)
    DEST[40:47] ← 0;
  ELSE (* 32-bit Operand Size *)
    DEST[0:15] ← GDTR(Limit);
    DEST[16:47] ← GDTR(Base); (* full 32-bit base address loaded *)
  FI;
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

IA-32_Intercept Instruction Intercept for SIDT and SGDT.
SGDT/SIDT—Store Global/Interrupt Descriptor Table Register (Continued)

**Protected Mode Exceptions**

<table>
<thead>
<tr>
<th>Exception Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#UD</td>
<td>If the destination operand is a register.</td>
</tr>
<tr>
<td>#GP(0)</td>
<td>If the destination is located in a nonwritable segment.</td>
</tr>
<tr>
<td></td>
<td>If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.</td>
</tr>
<tr>
<td></td>
<td>If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.</td>
</tr>
<tr>
<td>#SS(0)</td>
<td>If a memory operand effective address is outside the SS segment limit.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#AC(0)</td>
<td>If an unaligned memory access occurs when the CPL is 3 and alignment checking is enabled.</td>
</tr>
</tbody>
</table>

**Real Address Mode Exceptions**

<table>
<thead>
<tr>
<th>Exception Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#UD</td>
<td>If the destination operand is a register.</td>
</tr>
<tr>
<td>#GP</td>
<td>If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.</td>
</tr>
<tr>
<td>#SS</td>
<td>If a memory operand effective address is outside the SS segment limit.</td>
</tr>
</tbody>
</table>

**Virtual 8086 Mode Exceptions**

<table>
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<tr>
<th>Exception Code</th>
<th>Description</th>
</tr>
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<tr>
<td>#UD</td>
<td>If the destination operand is a register.</td>
</tr>
<tr>
<td>#GP(0)</td>
<td>If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.</td>
</tr>
<tr>
<td>#SS(0)</td>
<td>If a memory operand effective address is outside the SS segment limit.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#AC(0)</td>
<td>If an unaligned memory access occurs when alignment checking is enabled.</td>
</tr>
</tbody>
</table>

**Intel® Architecture Compatibility**

The 16-bit forms of the SGDT and SIDT instructions are compatible with the Intel 286 processor, if the upper 8 bits are not referenced. The Intel 286 processor fills these bits with 1s; the Pentium Pro processor fills these bits with 0s.
SHL/SHR—Shift Instructions

See entry for SAL/SAR/SHL/SHR.
SHLD—Double Precision Shift Left

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F A4</td>
<td>SHLD r/m16,r16,imm8</td>
<td>Shift r/m16 to left imm8 places while shifting bits from r16 in from the right</td>
</tr>
<tr>
<td>0F A5</td>
<td>SHLD r/m16,r16,CL</td>
<td>Shift r/m16 to left CL places while shifting bits from r16 in from the right</td>
</tr>
<tr>
<td>0F A4</td>
<td>SHLD r/m32,r32,imm8</td>
<td>Shift r/m32 to left imm8 places while shifting bits from r32 in from the right</td>
</tr>
<tr>
<td>0F A5</td>
<td>SHLD r/m32,r32,CL</td>
<td>Shift r/m32 to left CL places while shifting bits from r32 in from the right</td>
</tr>
</tbody>
</table>

Description

Shifts the first operand (destination operand) to the left the number of bits specified by the third operand (count operand). The second operand (source operand) provides bits to shift in from the right (starting with bit 0 of the destination operand). The destination operand can be a register or a memory location; the source operand is a register. The count operand is an unsigned integer that can be an immediate byte or the contents of the CL register. Only bits 0 through 4 of the count are used, which masks the count to a value between 0 and 31. If the count is greater than the operand size, the result in the destination operand is undefined.

If the count is 1 or greater, the CF flag is filled with the last bit shifted out of the destination operand. For a 1-bit shift, the OF flag is set if a sign change occurred; otherwise, it is cleared. If the count operand is 0, the flags are not affected.

The SHLD instruction is useful for multi-precision shifts of 64 bits or more.

Operation

COUNT ← COUNT MOD 32;
SIZE ← OperandSize
IF COUNT = 0
    THEN
        no operation
    ELSE
        IF COUNT ≥ SIZE
            THEN (* Bad parameters *)
                DEST is undefined;
                CF, OF, SF, ZF, AF, PF are undefined;
            ELSE (* Perform the shift *)
                CF ← BIT[DEST, SIZE – COUNT];
                (* Last bit shifted out on exit *)
                FOR i ← SIZE – 1 DOWNTO COUNT
                    DO
                        BIT(Dest, i) ← BIT(Dest, i – COUNT);
                        OD;
                    FOR i ← COUNT – 1 DOWNTO 0
                        OD;
                    OD;
SHLD—Double Precision Shift Left (Continued)

\[
\text{DO}
\begin{align*}
\text{BIT}[\text{DEST, } i] & \leftarrow \text{BIT}[\text{SRC, } i - \text{COUNT} + \text{SIZE}] ; \\
\text{OD} ;
\end{align*}
\]

\[\text{FI} ;\]
\[\text{FI} ;\]

Flags Affected

If the count is 1 or greater, the CF flag is filled with the last bit shifted out of the destination operand and the SF, ZF, and PF flags are set according to the value of the result. For a 1-bit shift, the OF flag is set if a sign change occurred; otherwise, it is cleared. For shifts greater than 1 bit, the OF flag is undefined. If a shift occurs, the AF flag is undefined. If the count operand is 0, the flags are not affected. If the count is greater than the operand size, the flags are undefined.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>NaT Register Consumption Abort.</th>
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</thead>
<tbody>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault</td>
</tr>
</tbody>
</table>

Protected Mode Exceptions

- **#GP(0)** If the destination is located in a nonwritable segment.
  - If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.

- **#SS(0)** If a memory operand effective address is outside the SS segment limit.

- **#PF(fault-code)** If a page fault occurs.

- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

- **#GP** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS** If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

- **#GP(0)** If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

- **#SS(0)** If a memory operand effective address is outside the SS segment limit.

- **#PF(fault-code)** If a page fault occurs.

- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made.
**SHRD—Double Precision Shift Right**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F AC</td>
<td>SHRD r/m16,r16,imm8</td>
<td>Shift r16 to right imm8 places while shifting bits from r16 in from the left</td>
</tr>
<tr>
<td>0F AD</td>
<td>SHRD r/m16,r16,CL</td>
<td>Shift r16 to right CL places while shifting bits from r16 in from the left</td>
</tr>
<tr>
<td>0F AC</td>
<td>SHRD r/m32,r32,imm8</td>
<td>Shift r32 to right imm8 places while shifting bits from r32 in from the left</td>
</tr>
<tr>
<td>0F AD</td>
<td>SHRD r/m32,r32,CL</td>
<td>Shift r32 to right CL places while shifting bits from r32 in from the left</td>
</tr>
</tbody>
</table>

**Description**

Shifts the first operand (destination operand) to the right the number of bits specified by the third operand (count operand). The second operand (source operand) provides bits to shift in from the left (starting with the most significant bit of the destination operand). The destination operand can be a register or a memory location; the source operand is a register. The count operand is an unsigned integer that can be an immediate byte or the contents of the CL register. Only bits 0 through 4 of the count are used, which masks the count to a value between 0 and 31. If the count is greater than the operand size, the result in the destination operand is undefined.

If the count is 1 or greater, the CF flag is filled with the last bit shifted out of the destination operand. For a 1-bit shift, the OF flag is set if a sign change occurred; otherwise, it is cleared. If the count operand is 0, the flags are not affected.

The SHRD instruction is useful for multiprecision shifts of 64 bits or more.

**Operation**

COUNT ← COUNT MOD 32;
SIZE ← OperandSize
IF COUNT = 0
    THEN
        no operation
    ELSE
        IF COUNT ≥ SIZE
            THEN (* Bad parameters *)
                DEST is undefined;
                CF, OF, SF, ZF, AF, PF are undefined;
            ELSE (* Perform the shift *)
                CF ← BIT[DEST, COUNT − 1]; (* last bit shifted out on exit *)
                FOR i ← 0 TO SIZE − 1 − COUNT
                    DO
                        BIT[DEST, i] ← BIT[DEST, i − COUNT];
                        OD;
                FOR i ← SIZE − COUNT TO SIZE − 1
                    DO
                        BIT[DEST, i] ← BIT[inBits,i+COUNT − SIZE];
                        OD;
            FI;
        FI;
SHRD—Double Precision Shift Right (Continued)

Flags Affected

If the count is 1 or greater, the CF flag is filled with the last bit shifted out of the destination operand and the SF, ZF, and PF flags are set according to the value of the result. For a 1-bit shift, the OF flag is set if a sign change occurred; otherwise, it is cleared. For shifts greater than 1 bit, the OF flag is undefined. If a shift occurs, the AF flag is undefined. If the count operand is 0, the flags are not affected. If the count is greater than the operand size, the flags are undefined.

Additional Itanium® System Environment Exceptions

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<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>

Protected Mode Exceptions

#GP(0) If the destination is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
SIDT—Store Interrupt Descriptor Table Register

See entry for SGDT/SIDT.
SLDT—Store Local Descriptor Table Register

### Description
Stores the segment selector from the local descriptor table register (LDTR) in the destination operand. The destination operand can be a general-purpose register or a memory location. The segment selector stored with this instruction points to the LDT.

When the destination operand is a 32-bit register, the 16-bit segment selector is copied into the lower 16 bits of the register and the upper 16 bits of the register are cleared to 0s. With the destination operand is a memory location, the segment selector is written to memory as a 16-bit quantity, regardless of the operand size.

The SLDT instruction is only useful in operating-system software; however, it can be used in application programs. Also, this instruction can only be executed in protected mode.

### Operation
**IF Itanium System Environment THEN IA-32_Intercept(INST,SLDT);**

```plaintext
DEST ← LDTR(SegmentSelector);
```

### Flags Affected
None.

### Additional Itanium® System Environment Exceptions
**IA-32_Intercept**
SLDT results in an IA-32 Intercept

### Protected Mode Exceptions
- **#GP(0)**
  If the destination is located in a nonwritable segment.
  If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
- **#SS(0)**
  If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)**
  If a page fault occurs.
- **#AC(0)**
  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

### Opcode

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /0</td>
<td>SLDT rm16</td>
<td>Stores segment selector from LDTR in rm16</td>
</tr>
<tr>
<td>0F 00 /0</td>
<td>SLDT rm32</td>
<td>Store segment selector from LDTR in low-order 16 bits of rm32; high-order 16 bits are undefined</td>
</tr>
</tbody>
</table>
SLDT—Store Local Descriptor Table Register (Continued)

**Real Address Mode Exceptions**

#UD The SLDT instruction is not recognized in real address mode.

**Virtual 8086 Mode Exceptions**

#UD The SLDT instruction is not recognized in virtual 8086 mode.
SMSW—Store Machine Status Word

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 01 /4</td>
<td>SMSW r32/m16</td>
<td>Store machine status word in low-order 16 bits of r32/m16; high-order 16 bits of r32 are undefined</td>
</tr>
</tbody>
</table>

**Description**

Stores the machine status word (bits 0 through 15 of control register CR0) into the destination operand. The destination operand can be a 16-bit general-purpose register or a memory location.

When the destination operand is a 32-bit register, the low-order 16 bits of register CR0 are copied into the low-order 16 bits of the register and the upper 16 bits of the register are undefined. With the destination operand is a memory location, the low-order 16 bits of register CR0 are written to memory as a 16-bit quantity, regardless of the operand size.

The SMSW instruction is only useful in operating-system software; however, it is not a privileged instruction and can be used in application programs.

This instruction is provided for compatibility with the Intel 286 processor; programs and procedures intended to run on processors more recent than the Intel 286 should use the MOV (control registers) instruction to load the machine status word.

**Operation**

IF Itanium System Environment THEN IA-32_Intercept(INST,SMSW);
DEST ← CR0[15:0]; (* MachineStatusWord *);

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

IA-32_Intercept Mandatory Instruction Intercept.

**Protected Mode Exceptions**

#GP(0) If the destination is located in a nonwritable segment.

If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
SMSW—Store Machine Status Word (Continued)

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
STC—Set Carry Flag

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F9</td>
<td>STC</td>
<td>Set CF flag</td>
</tr>
</tbody>
</table>

Description

Sets the CF flag in the EFLAGS register.

Operation

\[ CF \leftarrow 1; \]

Flags Affected

The CF flag is set. The OF, ZF, SF, AF, and PF flags are unaffected.

Exceptions (All Operating Modes)

None.
STD—Set Direction Flag

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FD</td>
<td>STD</td>
<td>Set DF flag</td>
</tr>
</tbody>
</table>

**Description**

Sets the DF flag in the EFLAGS register. When the DF flag is set to 1, string operations decrement the index registers (ESI and/or EDI).

**Operation**

\[
DF \leftarrow 1;
\]

**Flags Affected**

The DF flag is set. The CF, OF,ZF, SF, AF, and PF flags are unaffected.

**Operation**

\[
DF \leftarrow 1;
\]

**Exceptions (All Operating Modes)**

None.
STI—Set Interrupt Flag

Description

Sets the interrupt flag (IF) in the EFLAGS register. In the IA-32 System Environment, after the IF flag is set, the processor begins responding to external maskable interrupts after the next instruction is executed. If the STI instruction is followed by a CLI instruction (which clears the IF flag) the effect of the STI instruction is negated. In the Itanium System Environment, the processor will immediately respond do interrupts after STI, unless execution of STI results in a trap or intercept. External interrupts are enabled for IA-32 instructions if PSR.i and (~CFLG.if or EFLAG.if).

The IF flag and the STI and CLI instruction have no affect on the generation of exceptions and NMI interrupts.

The following decision table indicates the action of the STI instruction (bottom of the table) depending on the processor’s mode of operating and the CPL and IOPL of the currently running program or procedure (top of the table).

<table>
<thead>
<tr>
<th>PE</th>
<th>VM</th>
<th>CPL</th>
<th>IOPL</th>
<th>IF ← 1</th>
<th>#GP(0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>Y</td>
<td>N</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>≤ IOPL</td>
<td>&gt; IOPL</td>
<td>0</td>
<td>Y</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>3</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>X</td>
<td>3</td>
<td>N</td>
<td>N</td>
</tr>
</tbody>
</table>

Notes:
X Don’t care.
N Action in Column 1 not taken.
Y Action in Column 1 taken.

Operation

OLD_IF ← IF;
IF PE=0 (* Executing in real-address mode *)
THEN
  IF ← 1; (* Set Interrupt Flag *)
ELSE (* Executing in protected mode or virtual-8086 mode *)
  IF VM=0 (* Executing in protected mode*)
  THEN
    IF CR4.PVI = 0
    THEN
      IF CPL <= IOPL
      THEN IF ← 1
      ELSE #GP(0);
    FI;
    ELSE (*PVI is 1 *)
STI—Set Interrupt Flag (Continued)

IF CPL = 3
THEN STI—Set Interrupt Flag (Continued)

IF IOPL < 3
THEN
IF VIP = 0
THEN VIF <- 1;
ELSE #GP(0);
FI;
ELSE (*IOPL = 3 *)
IF <- 1;
FI;
ELSE (*CPL < 3*)
IF IOPL < CPL THEN #GP(0); FI;
IF IOPL>=CPL OR IOPL=3 THEN IF <-1; FI;
FI;
FI;
ELSE (*Executing in Virtual-8086 Mode*)
IF IOPL = 3
THEN IF <- 1;
ELSE
IF CR4.VME = 0
THEN #GP(0);
ELSE
IF VIP = 1 (*virtual interrupt is pending*)
THEN #GP(0);
ELSE VIF <- 1;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;
FI;

IF Itanium System Environment AND CFLG.ii AND IF != OLD_IF
THEN IA-32_Interceptor(System_Flag,STI);

Flags Affected
The IF flag is set to 1.

Additional Itanium® System Environment Exceptions
IA-32_Interceptor System Flag Intercept Trap if CFLG.ii is 1 and the IF flag changes state.

Protected Mode Exceptions
#GP(0) If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.
STI—Set Interrupt Flag (Continued)

Real Address Mode Exceptions
None.

Virtual 8086 Mode Exceptions

#GP(0) If the CPL is greater (has less privilege) than the IOPL of the current program or procedure.
STOS/STOSB/STOSW/STOSD—Store String Data

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AA</td>
<td>STOS ES:(E)DI</td>
<td>Store AL at address ES:(E)DI</td>
</tr>
<tr>
<td>AB</td>
<td>STOS ES:DI</td>
<td>Store AX at address ES:DI</td>
</tr>
<tr>
<td>AB</td>
<td>STOS ES:EDI</td>
<td>Store EAX at address ES:EDI</td>
</tr>
<tr>
<td>AA</td>
<td>STOSB</td>
<td>Store AL at address ES:(E)DI</td>
</tr>
<tr>
<td>AB</td>
<td>STOSW</td>
<td>Store AX at address ES:DI</td>
</tr>
<tr>
<td>AB</td>
<td>STOSD</td>
<td>Store EAX at address ES:EDI</td>
</tr>
</tbody>
</table>

**Description**

Stores a byte, word, or doubleword from the AL, AX, or EAX register, respectively, into the destination operand. The destination operand is a memory location at the address ES:EDI. (When the operand-size attribute is 16, the DI register is used as the source-index register.) The ES segment cannot be overridden with a segment override prefix.

The STOSB, STOSW, and STOSD mnemonics are synonyms of the byte, word, and doubleword versions of the STOS instructions. They are simpler to use, but provide no type or segment checking. (For the STOS instruction, “ES:EDI” must be explicitly specified in the instruction.)

After the byte, word, or doubleword is transferred from the AL, AX, or EAX register to the memory location, the EDI register is incremented or decremented automatically according to the setting of the DF flag in the EFLAGS register. (If the DF flag is 0, the EDI register is incremented; if the DF flag is 1, the EDI register is decremented.) The EDI register is incremented or decremented by 1 for byte operations, by 2 for word operations, or by 4 for doubleword operations.

The STOS, STOSB, STOSW, and STOSD instructions can be preceded by the REP prefix for block loads of ECX bytes, words, or doublewords. More often, however, these instructions are used within a LOOP construct, because data needs to be moved into the AL, AX, or EAX register before it can be stored. See “REP/REPE/REPZ/REPNE/REPNZ—Repeat String Operation Prefix” on page 3:685 for a description of the REP prefix.

**Operation**

IF (byte store)
  THEN
    DEST ← AL;
    THEN IF DF = 0
      THEN (E)DI ← 1;
      ELSE (E)DI ← −1;
    FI;
  ELSE IF (word store)
    THEN
      DEST ← AX;
      THEN IF DF = 0
        THEN DI ← 2;
        ELSE DI ← −2;
      FI;
    ELSE (* doubleword store *)
      DEST ← EAX;
      THEN IF DF = 0
        THEN DI ← 4;
        ELSE DI ← −4;
      FI;
STOS/STOSB/STOSW/STOSD—Store String Data (Continued)

THEN EDI ← 4;
ELSE EDI ← −4;
FI;
FI;
FI;
FI;

Flags Affected
None.

Additional Itanium® System Environment Exceptions
Itanium Reg Faults NaT Register Consumption Abort.
Itanium Mem Faults VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions
#GP(0) If the destination is located in a nonwritable segment.
If a memory operand effective address is outside the limit of the ES segment.
If the ES register contains a null segment selector.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions
#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
STR—Store Task Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /1</td>
<td>STR r/m16</td>
<td>Stores segment selector from TR in r/m16</td>
</tr>
</tbody>
</table>

**Description**

Stores the segment selector from the task register (TR) in the destination operand. The destination operand can be a general-purpose register or a memory location. The segment selector stored with this instruction points to the task state segment (TSS) for the currently running task.

When the destination operand is a 32-bit register, the 16-bit segment selector is copied into the lower 16 bits of the register and the upper 16 bits of the register are cleared to 0s. With the destination operand is a memory location, the segment selector is written to memory as a 16-bit quantity, regardless of operand size.

The STR instruction is useful only in operating-system software. It can only be executed in protected mode.

**Operation**

IF Itanium System Environment THEN IA-32_Intercept(INST,STR);
DEST ← TR(SegmentSelector);

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

IA-32_Intercept Mandatory Instruction Intercept.

**Protected Mode Exceptions**

- **#GP(0)** If the destination is a memory operand that is located in a nonwritable segment or if the effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#SS(0)** If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)** If a page fault occurs.
- **#AC(0)** If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real Address Mode Exceptions**

- **#UD** The STR instruction is not recognized in real address mode.

**Virtual 8086 Mode Exceptions**

- **#UD** The STR instruction is not recognized in virtual 8086 mode.
SUB—Integer Subtraction

Description

Subtracts the second operand (source operand) from the first operand (destination operand) and stores the result in the destination operand. The destination operand can be a register or a memory location; the source operand can be an immediate, register, or memory location. When an immediate value is used as an operand, it is sign-extended to the length of the destination operand format.

The SUB instruction does not distinguish between signed or unsigned operands. Instead, the processor evaluates the result for both data types and sets the OF and CF flags to indicate a borrow in the signed or unsigned result, respectively. The SF flag indicates the sign of the signed result.

Operation

\[ \text{DEST} \leftarrow \text{DEST} - \text{SRC}; \]

Flags Affected

The OF, SF, ZF, AF, PF, and CF flags are set according to the result.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>NaT Register Consumption Abort.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>
SUB—Integer Subtraction (Continued)

Protected Mode Exceptions

#GP(0) If the destination is located in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
TEST—Logical Compare

**Description**

Computes the bit-wise logical AND of first operand (source 1 operand) and the second operand (source 2 operand) and sets the SF, ZF, and PF status flags according to the result. The result is then discarded.

**Operation**

\[
\begin{align*}
\text{TEMP} & \leftarrow \text{SRC1 AND SRC2;} \\
\text{SF} & \leftarrow \text{MSB(TEMP);} \\
\text{IF TEMP = 0} & \\
\text{THEN ZF} & \leftarrow 0; \\
\text{ELSE ZF} & \leftarrow 1; \\
\text{FI;} \\
\text{PF} & \leftarrow \text{BitwiseXNOR(TEMP[0:7]);} \\
\text{CF} & \leftarrow 0; \\
\text{OF} & \leftarrow 0; \\
(*AF is Undefined*)
\end{align*}
\]

**Flags Affected**

The OF and CF flags are cleared to 0. The SF, ZF, and PF flags are set according to the result (see “Operation” above). The state of the AF flag is undefined.

**Additional Itanium® System Environment Exceptions**

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>NaT Register Consumption Abort.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>
TEST—Logical Compare (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
   If the DS, ES, FS, or GS register contains a null segment selector.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
UD2—Undefined Instruction

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 0B</td>
<td>UD2</td>
<td>Raise invalid opcode exception</td>
</tr>
</tbody>
</table>

Description

Generates an invalid opcode. This instruction is provided for software testing to explicitly generate an invalid opcode. The opcode for this instruction is reserved for this purpose.

Other than raising the invalid opcode exception, this instruction is the same as the NOP instruction.

Operation

IF Itanium System Environment THEN IA-32_Intercept(INST,0F0B);
#UD (* Generates invalid opcode exception *);

Flags Affected

None.

Additional Itanium® System Environment Exceptions

IA-32_Intercept  Mandatory Instruction Intercept.

Exceptions (All Operating Modes)

#UD  Instruction is guaranteed to raise an invalid opcode exception in all operating modes).
VERR, VERW—Verify a Segment for Reading or Writing

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 00 /4</td>
<td>VERR r/m16</td>
<td>Set ZF=1 if segment specified with r/m16 can be read</td>
</tr>
<tr>
<td>0F 00 /5</td>
<td>VERW r/m16</td>
<td>Set ZF=1 if segment specified with r/m16 can be written</td>
</tr>
</tbody>
</table>

**Description**

Verifies whether the code or data segment specified with the source operand is readable (VERR) or writable (VERW) from the current privilege level (CPL). The source operand is a 16-bit register or a memory location that contains the segment selector for the segment to be verified. If the segment is accessible and readable (VERR) or writable (VERW), the ZF flag is set; otherwise, the ZF flag is cleared. Code segments are never verified as writable. This check cannot be performed on system segments.

To set the ZF flag, the following conditions must be met:

- The segment selector is not null.
- The selector must denote a descriptor within the bounds of the descriptor table (GDT or LDT).
- The selector must denote the descriptor of a code or data segment (not that of a system segment or gate).
- For the VERR instruction, the segment must be readable; the VERW instruction, the segment must be a writable data segment.
- If the segment is not a conforming code segment, the segment’s DPL must be greater than or equal to (have less or the same privilege as) both the CPL and the segment selector's RPL.

The validation performed is the same as if the segment were loaded into the DS, ES, FS, or GS register, and the indicated access (read or write) were performed. The selector's value cannot result in a protection exception, enabling the software to anticipate possible segment access problems.

**Operation**

```assembly
IF SRC(Offset) > (GDTR(Limit) OR (LDTR(Limit))
    THEN
        ZF ← 0

Read segment descriptor;
IF SegmentDescriptor(DescriptorType) = 0 (* system segment *)
    OR (SegmentDescriptor(Type) ≠ conforming code segment)
    AND (CPL > DPL) OR (RPL > DPL)
    THEN
        ZF ← 0
    ELSE
        IF ((Instruction = VERR) AND (segment = readable))
            OR ((Instruction = VERW) AND (segment = writable))
            THEN
                ZF ← 1;
        FI;
    FI;
```
VERR, VERW—Verify a Segment for Reading or Writing (Continued)

Flags Affected

The ZF flag is set to 1 if the segment is accessible and readable (VERR) or writable (VERW); otherwise, it is cleared to 0.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

The only exceptions generated for these instructions are those related to illegal addressing of the source operand.

#GP(0)    If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
          If the DS, ES, FS, or GS register is used to access memory and it contains a null segment selector.
#SS(0)    If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)    If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real Address Mode Exceptions

#UD  The VERR and VERW instructions are not recognized in real address mode.

Virtual 8086 Mode Exceptions

#UD  The VERR and VERW instructions are not recognized in virtual 8086 mode.
## WAIT/FWAIT—Wait

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9B</td>
<td>WAIT</td>
<td>Check pending unmasked floating-point exceptions.</td>
</tr>
<tr>
<td>9B</td>
<td>FWAIT</td>
<td>Check pending unmasked floating-point exceptions.</td>
</tr>
</tbody>
</table>

### Description

Causes the processor to check for and handle pending unmasked floating-point exceptions before proceeding. (FWAIT is an alternate mnemonic for the WAIT). This instruction is useful for synchronizing exceptions in critical sections of code. Coding a WAIT instruction after a floating-point instruction insures that any unmasked floating-point exceptions the instruction may raise are handled before the processor can modify the instruction’s results.

### Operation

```
CheckPendingUnmaskedFloatingPointExceptions;
```

### FPU Flags Affected

The C0, C1, C2, and C3 flags are undefined.

### Floating-point Exceptions

None.

### Protected Mode Exceptions

- **#NM**: MP and TS in CR0 is set.

### Real Address Mode Exceptions

- **#NM**: MP and TS in CR0 is set.

### Virtual 8086 Mode Exceptions

- **#NM**: MP and TS in CR0 is set.
WBINVD—Write-Back and Invalidate Cache

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 09</td>
<td>WBINVD</td>
<td>Write-back and flush Internal caches; initiate writing-back and flushing of external caches.</td>
</tr>
</tbody>
</table>

**Description**

Writes back all modified cache lines in the processor’s internal cache to main memory, invalidates (flushes) the internal caches, and issues a special-function bus cycle that directs external caches to also write back modified data.

After executing this instruction, the processor does not wait for the external caches to complete their write-back and flushing operations before proceeding with instruction execution. It is the responsibility of hardware to respond to the cache write-back and flush signals.

The WBINVD instruction is a privileged instruction. When the processor is running in protected mode, the CPL of a program or procedure must be 0 to execute this instruction. This instruction is also a serializing instruction.

In situations where cache coherency with main memory is not a concern, software can use the INVD instruction.

**Operation**

```plaintext
IF Itanium System Environment THEN IA-32_Intercept(INST,WBINVD);
WriteBack(InternalCaches);
Flush(InternalCaches);
SignalWriteBack(ExternalCaches);
SignalFlush(ExternalCaches);
Continue (* Continue execution);
```

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

IA-32_Intercept Mandatory Instruction Intercept.

**Protected Mode Exceptions**

#GP(0) If the current privilege level is not 0.

**Real Address Mode Exceptions**

None.
Virtual 8086 Mode Exceptions

#GP(0) The WBINVD instruction cannot be executed at the virtual 8086 mode.

Intel® Architecture Compatibility

The WDINVD instruction implementation-dependent; its function may be implemented differently on future Intel architecture processors. The instruction is not supported on Intel architecture processors earlier than the Intel486 processor.
**WRMSR—Write to Model Specific Register**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 30</td>
<td>WRMSR</td>
<td>Write the value in EDX:EAX to MSR specified by ECX</td>
</tr>
</tbody>
</table>

**Description**

Writes the contents of registers EDX:EAX into the 64-bit model specific register (MSR) specified in the ECX register. The high-order 32 bits are copied from EDX and the low-order 32 bits are copied from EAX. Always set undefined or reserved bits in an MSR to the values previously read.

This instruction must be executed at privilege level 0 or in real-address mode; otherwise, a general protection exception #GP(0) will be generated. Specifying a reserved or unimplemented MSR address in ECX will also cause a general protection exception.

When the WRMSR instruction is used to write to an MTRR, the TLBs are invalidated, including the global entries see the *IA-32 Intel® Architecture Software Developer’s Manual, Volume 3*).

The MSRs control functions for testability, execution tracing, performance-monitoring and machine check errors. See model specific instructions for all the MSRs that can be written to with this instruction and their addresses.

The WRMSR instruction is a serializing instruction.

The CPUID instruction should be used to determine whether MSRs are supported (EDX[5]=1) before using this instruction.

**Operation**

```plaintext
IF Itanium System Environment THEN IA-32_Intercept(INST,WRMSR);
MSR[ECX] ← EDX:EAX;
```

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

IA-32_Interceptor Mandatory Instruction Intercept.

**Protected Mode Exceptions**

- #GP(0) If the current privilege level is not 0.
  
  If the value in ECX specifies a reserved or unimplemented MSR address.

**Real Address Mode Exceptions**

- #GP If the current privilege level is not 0.
  
  If the value in ECX specifies a reserved or unimplemented MSR address.
WRMSR—Write to Model Specific Register (Continued)

Virtual 8086 Mode Exceptions

#GP(0) The WRMSR instruction is not recognized in virtual 8086 mode.

Intel® Architecture Compatibility

The MSRs and the ability to read them with the WRMSR instruction were introduced into the Intel architecture with the Pentium processor. Execution of this instruction by an Intel architecture processor earlier than the Pentium processor results in an invalid opcode exception #UD.
XADD—Exchange and Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F C0/r</td>
<td>XADD r/m8,r8</td>
<td>Exchange r8 and r/m8; load sum into r/m8.</td>
</tr>
<tr>
<td>0F C1/r</td>
<td>XADD r/m16,r16</td>
<td>Exchange r16 and r/m16; load sum into r/m16.</td>
</tr>
<tr>
<td>0F C1/r</td>
<td>XADD r/m32,r32</td>
<td>Exchange r32 and r/m32; load sum into r/m32.</td>
</tr>
</tbody>
</table>

Description

Exchanges the first operand (destination operand) with the second operand (source operand), then loads the sum of the two values into the destination operand. The destination operand can be a register or a memory location; the source operand is a register.

This instruction can be used with a LOCK prefix.

Operation

\[
\text{IF Itanium System Environment AND External Bus Lock Required AND DCR.lc}\]
\[
\text{THEN IA-32 Intercept(LOCK,XADD);}\]
\[
\text{TEMP} \leftarrow \text{SRC + DEST}\]
\[
\text{SRC} \leftarrow \text{DEST}\]
\[
\text{DEST} \leftarrow \text{TEMP}\]

Flags Affected

The CF, PF, AF, SF, ZF, and OF flags are set according to the result stored in the destination operand.

Additional Itanium® System Environment Exceptions

- **Itanium Reg Faults**: NaT Register Consumption Abort.
- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
- **IA-32 Intercept**: Lock Intercept - If an external atomic bus lock is required to complete this operation and DCR.lc is 1, no atomic transaction occurs, this instruction is faulted and an IA-32Interceptor (Lock) fault is generated. The software lock handler is responsible for the emulation of this instruction.

Protected Mode Exceptions

- **#GP(0)**: If the destination is located in a nonwritable segment.
- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
- **#GP(0)**: If the DS, ES, FS, or GS register contains a null segment selector.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
XADD—Exchange and Add (Continued)

**Real Address Mode Exceptions**

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

**Virtual 8086 Mode Exceptions**

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.

**Intel® Architecture Compatibility**

Intel architecture processors earlier than the Intel486 processor do not recognize this instruction. If this instruction is used, you should provide an equivalent code sequence that runs on earlier processors.
XCHG—Exchange Register/Memory with Register

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>90+rw</td>
<td>XCHG AX,r16</td>
<td>Exchange r16 with AX</td>
</tr>
<tr>
<td>90+rw</td>
<td>XCHG r16,AX</td>
<td>Exchange r16 with AX</td>
</tr>
<tr>
<td>90+rd</td>
<td>XCHG EAX,r32</td>
<td>Exchange r32 with EAX</td>
</tr>
<tr>
<td>90+rd</td>
<td>XCHG r32,EAX</td>
<td>Exchange r32 with EAX</td>
</tr>
<tr>
<td>86 /r</td>
<td>XCHG r/m8,r8</td>
<td>Exchange byte register with EA byte</td>
</tr>
<tr>
<td>86 /r</td>
<td>XCHG r8,r/m8</td>
<td>Exchange byte register with EA byte</td>
</tr>
<tr>
<td>87 /r</td>
<td>XCHG r/m16,r16</td>
<td>Exchange r16 with EA word</td>
</tr>
<tr>
<td>87 /r</td>
<td>XCHG r16,r/m16</td>
<td>Exchange r16 with EA word</td>
</tr>
<tr>
<td>87 /r</td>
<td>XCHG r/m32,r32</td>
<td>Exchange r32 with EA doubleword</td>
</tr>
<tr>
<td>87 /r</td>
<td>XCHG r32,r/m32</td>
<td>Exchange r32 with EA doubleword</td>
</tr>
</tbody>
</table>

Description

Exchanges the contents of the destination (first) and source (second) operands. The operands can be two general-purpose registers or a register and a memory location. When the operands are two registers, one of the registers must be the EAX or AX register. If a memory operand is referenced, the LOCK# signal is automatically asserted for the duration of the exchange operation, regardless of the presence or absence of the LOCK prefix or of the value of the IOPL.

This instruction is useful for implementing semaphores or similar data structures for process synchronization. (See Chapter 5, *Processor Management and Initialization*, in the IA-32 Intel® Architecture Software Developer’s Manual, Volume 3 for more information on bus locking.)

The XCHG instruction can also be used instead of the BSWAP instruction for 16-bit operands.

Operation

\[
\text{IF Itanium System Environment AND External\_Atomic\_Lock\_Required AND DCR.lc THEN IA-32\_Intercept(LOCK,XCHG);}
\]

\[
\text{TEMP } \leftarrow \text{ DEST}
\]

\[
\text{DEST } \leftarrow \text{ SRC}
\]

\[
\text{SRC } \leftarrow \text{ TEMP}
\]

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults: NaT Register Consumption Abort.

Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

IA-32_Interceptor: Lock Intercept - If an external atomic bus lock is required to complete this operation and DCR.lc is 1, no atomic transaction occurs, this instruction is faulted and an IA-32_Interceptor(Lock) fault is generated. The software lock handler is responsible for the emulation of this instruction.
XCHG—Exchange Register/Memory with Register (Continued)

Protected Mode Exceptions

#GP(0) If either operand is in a nonwritable segment.
       If a memory operand effective address is outside the CS, DS, ES, FS, or GS
       segment limit.
       If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made
       while the current privilege level is 3.

Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.
#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS
segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
**XLAT/XLATB—Table Look-up Translation**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D7</td>
<td>XLAT m8</td>
<td>Set AL to memory byte DS:[(E)BX + unsigned AL]</td>
</tr>
<tr>
<td>D7</td>
<td>XLATB</td>
<td>Set AL to memory byte DS:[(E)BX + unsigned AL]</td>
</tr>
</tbody>
</table>

**Description**

Locates a byte entry in a table in memory, using the contents of the AL register as a table index, then copies the contents of the table entry back into the AL register. The index in the AL register is treated as unsigned integer. The XLAT and XLATB instructions get the base address of the table in memory from the DS:EBX registers (or the DS:BX registers when the address-size attribute of 16 bits.) The XLAT instruction allows a different segment register to be specified with a segment override. When assembled, the XLAT and XLATB instructions produce the same machine code.

**Operation**

```plaintext
IF AddressSize = 16
    THEN
        AL ← (DS:BX + ZeroExtend(AL))
    ELSE (* AddressSize = 32 *)
        AL ← (DS:EBX + ZeroExtend(AL));
FI;
```

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Protected Mode Exceptions**

- #GP(0): If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.
  - If the DS, ES, FS, or GS register contains a null segment selector.
- #SS(0): If a memory operand effective address is outside the SS segment limit.
- #PF(fault-code): If a page fault occurs.
- #AC(0): If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
Real Address Mode Exceptions

#GP If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS, or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
XOR—Logical Exclusive OR

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>34 ib</td>
<td>XOR AL,imm8</td>
<td>AL XOR imm8</td>
</tr>
<tr>
<td>35 iw</td>
<td>XOR AX,imm16</td>
<td>AX XOR imm16</td>
</tr>
<tr>
<td>35 id</td>
<td>XOR EAX,imm32</td>
<td>EAX XOR imm32</td>
</tr>
<tr>
<td>80 /6 ib</td>
<td>XOR r/m8,imm8</td>
<td>r/m8 XOR imm8</td>
</tr>
<tr>
<td>81 /6 iw</td>
<td>XOR r/m16,imm16</td>
<td>r/m16 XOR imm16</td>
</tr>
<tr>
<td>81 /6 id</td>
<td>XOR r/m32,imm32</td>
<td>r/m32 XOR imm32</td>
</tr>
<tr>
<td>83 /6 ib</td>
<td>XOR r/m16,imm8</td>
<td>r/m16 XOR imm8</td>
</tr>
<tr>
<td>83 /6 ib</td>
<td>XOR r/m32,imm8</td>
<td>r/m32 XOR imm8</td>
</tr>
<tr>
<td>30 lr</td>
<td>XOR r/m8,r8</td>
<td>r/m8 XOR r8</td>
</tr>
<tr>
<td>31 lr</td>
<td>XOR r/m16,r16</td>
<td>r/m16 XOR r16</td>
</tr>
<tr>
<td>31 lr</td>
<td>XOR r/m32,r32</td>
<td>r/m32 XOR r32</td>
</tr>
<tr>
<td>32 lr</td>
<td>XOR r8,rim8</td>
<td>r8 XOR rim8</td>
</tr>
<tr>
<td>33 lr</td>
<td>XOR r16,rim16</td>
<td>r8 XOR rim8</td>
</tr>
<tr>
<td>33 lr</td>
<td>XOR r32,rim32</td>
<td>r8 XOR rim8</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise exclusive-OR (XOR) operation on the destination (first) and source (second) operands and stores the result in the destination operand location. The source operand can be an immediate, a register, or a memory location; the destination operand can be a register or a memory location.

**Operation**

DEST ← DEST XOR SRC;

**Flags Affected**

The OF and CF flags are cleared; the SF, ZF, and PF flags are set according to the result. The state of the AF flag is undefined.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
XOR—Logical Exclusive OR (Continued)

Protected Mode Exceptions

#GP(0)  If the destination operand points to a nonwritable segment.
        If a memory operand effective address is outside the CS, DS, ES, FS, or GS
        segment limit.
        If the DS, ES, FS, or GS register contains a null segment selector.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made
        while the current privilege level is 3.

Real Address Mode Exceptions

#GP  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
      segment limit.
#SS  If a memory operand effective address is outside the SS segment limit.

Virtual 8086 Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS, or GS
        segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
This section lists the IA-32 MMX technology instructions designed to increase performance of multimedia intensive applications.
EMMS—Empty MMX State

### Description

Sets the values of all the tags in the FPU tag word to empty (all ones). This operation marks the MMX technology registers as available, so they can subsequently be used by floating-point instructions. (See Figure 7-11 in the *IA-32 Intel® Architecture Software Developer’s Manual*, for the format of the FPU tag word.) All other MMX instructions (other than the EMMS instruction) set all the tags in FPU tag word to valid (all zeros).

The EMMS instruction must be used to clear the MMX technology state at the end of all MMX technology routines and before calling other procedures or subroutines that may execute floating-point instructions. If a floating-point instruction loads one of the registers in the FPU register stack before the FPU tag word has been reset by the EMMS instruction, a floating-point stack overflow can occur that will result in a floating-point exception or incorrect result.

### Operation

\[
\text{FPUTagWord} \leftarrow \text{FFFFH} ;
\]

### Flags Affected

None.

### Additional Itanium® System Environment Exceptions

*Itanium Reg Faults* Disabled FP Register Fault if PSR.dfl is 1.

### Protected Mode Exceptions

- **#UD** If EM in CR0 is set.
- **#NM** If TS in CR0 is set.
- **#MF** If there is a pending FPU exception.

### Real-Address Mode Exceptions

- **#UD** If EM in CR0 is set.
- **#NM** If TS in CR0 is set.
- **#MF** If there is a pending FPU exception.

### Virtual-8086 Mode Exceptions

- **#UD** If EM in CR0 is set.
- **#NM** If TS in CR0 is set.
- **#MF** If there is a pending FPU exception.
MOVD—Move 32 Bits

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 6E/r</td>
<td>MOVD mm, r/m32</td>
<td>Move doubleword from r/m32 to mm.</td>
</tr>
<tr>
<td>0F 7E/r</td>
<td>MOVD r/m32, mm</td>
<td>Move doubleword from mm to r/m32.</td>
</tr>
</tbody>
</table>

**Description**

Copies doubleword from the source operand (second operand) to the destination operand (first operand). Source and destination operands can be MMX technology registers, memory locations, or 32-bit general-purpose registers; however, data cannot be transferred from an MMX technology register to an MMX technology register, from one memory location to another memory location, or from one general-purpose register to another general-purpose register.

When the destination operand is an MMX technology register, the 32-bit source value is written to the low-order 32 bits of the 64-bit MMX technology register and zero-extended to 64 bits (see Figure 2-1). When the source operand is an MMX technology register, the low-order 32 bits of the MMX technology register are written to the 32-bit general-purpose register or 32-bit memory location selected with the destination operand.

**Figure 2-1. Operation of the MOVD Instruction**

![Operation of the MOVD Instruction](image)

**Operation**

If DEST is MMX register

Then

DEST ← ZeroExtend(SRC);

Else (* SRC is MMX register *)

DEST ← LowOrderDoubleword(SRC);
MOVD—Move 32 Bits (Continued)

Flags Affected

None.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Issue Type</th>
<th>Exception Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Reg Faults</td>
<td>Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.</td>
</tr>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault,</td>
</tr>
<tr>
<td></td>
<td>Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss</td>
</tr>
<tr>
<td></td>
<td>Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit</td>
</tr>
<tr>
<td></td>
<td>Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>

Protected Mode Exceptions

#GP(0) If the destination operand is in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.

#SS(0) If a memory operand effective address is outside the SS segment limit.

#UD If EM in CR0 is set.

#NM If TS in CR0 is set.

#MF If there is a pending FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.

#UD If EM in CR0 is set.

#NM If TS in CR0 is set.

#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.

#UD If EM in CR0 is set.

#NM If TS in CR0 is set.

#MF If there is a pending FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
MOVQ—Move 64 Bits

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 6F</td>
<td>MOVQ mm, mm/m64</td>
<td>Move quadword from mm/m64 to mm.</td>
</tr>
<tr>
<td>0F 7F</td>
<td>MOVQ mm/m64, mm</td>
<td>Move quadword from mm to mm/m64.</td>
</tr>
</tbody>
</table>

Description

Copies quadword from the source operand (second operand) to the destination operand (first operand). (See Figure 2-2.) A source or destination operand can be either an MMX technology register or a memory location; however, data cannot be transferred from one memory location to another memory location. Data can be transferred from one MMX technology register to another MMX technology register.

Figure 2-2. Operation of the MOVQ Instruction

![Figure 2-2. Operation of the MOVQ Instruction](image)

Operation

DEST ← SRC;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
MOVQ—Move 64 Bits (Continued)

Protected Mode Exceptions

#GP(0) If the destination operand is in a nonwritable segment.
If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PACKSSWB/PACKSSDW—Pack with Signed Saturation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 63</td>
<td>PACKSSWB mm, mm/ m64</td>
<td>Packs and saturates pack 4 signed words from mm and 4 signed words from mm/m64 into 8 signed bytes in mm.</td>
</tr>
<tr>
<td>0F 6B</td>
<td>PACKSSDW mm, mm/ m64</td>
<td>Pack and saturate 2 signed doublewords from mm and 2 signed doublewords from mm/m64 into 4 signed words in mm.</td>
</tr>
</tbody>
</table>

**Description**

Packs and saturates signed words into bytes (PACKSSWB) or signed doublewords into words (PACKSSDW). The PACKSSWB instruction packs 4 signed words from the destination operand (first operand) and 4 signed words from the source operand (second operand) into 8 signed bytes in the destination operand. If the signed value of a word is beyond the range of a signed byte (that is, greater than 7FH or less than 80H), the saturated byte value of 7FH or 80H, respectively, is stored into the destination.

The PACKSSDW instruction packs 2 signed doublewords from the destination operand (first operand) and 2 signed doublewords from the source operand (second operand) into 4 signed words in the destination operand (see Figure 2-3). If the signed value of a doubleword is beyond the range of a signed word (that is, greater than 7FFFH or less than 8000H), the saturated word value of 7FFFH or 8000H, respectively, is stored into the destination.

The destination operand for either the PACKSSWB or PACKSSDW instruction must be an MMX technology register; the source operand may be either an MMX technology register or a quadword memory location.

**Figure 2-3. Operation of the PACKSSDW Instruction**

![Figure 2-3. Operation of the PACKSSDW Instruction](image)

**Operation**

IF instruction is PACKSSWB

THEN

- DEST(7..0) ← SaturateSignedWordToSignedByte DEST(15..0);
- DEST(15..8) ← SaturateSignedWordToSignedByte DEST(31..16);
- DEST(23..16) ← SaturateSignedWordToSignedByte DEST(47..32);
- DEST(31..24) ← SaturateSignedWordToSignedByte DEST(63..48);
- DEST(39..32) ← SaturateSignedWordToSignedByte SRC(15..0);
- DEST(47..40) ← SaturateSignedWordToSignedByte SRC(31..16);
- DEST(55..48) ← SaturateSignedWordToSignedByte SRC(47..32);
- DEST(63..56) ← SaturateSignedWordToSignedByte SRC(63..48);
PACKSSWB/PACKSSDW—Pack with Signed Saturation  (Continued)

ELSE (* instruction is PACKSSDW *)
  DEST(15..0) ← SaturateSignedDoublewordToSignedWord DEST(31..0);
  DEST(31..16) ← SaturateSignedDoublewordToSignedWord DEST(63..32);
  DEST(47..32) ← SaturateSignedDoublewordToSignedWord SRC(31..0);
  DEST(63..48) ← SaturateSignedDoublewordToSignedWord SRC(63..32);
FI;

Flags Affected
None.

Additional Itanium® System Environment Exceptions
Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
PACKSSWB/PACKSSDW—Pack with Signed Saturation (Continued)

Virtual-8086 Mode Exceptions

<table>
<thead>
<tr>
<th>Exception Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP</td>
<td>If any part of the operand lies outside of the effective address space from 0 to FFFFH.</td>
</tr>
<tr>
<td>#UD</td>
<td>If EM in CR0 is set.</td>
</tr>
<tr>
<td>#NM</td>
<td>If TS in CR0 is set.</td>
</tr>
<tr>
<td>#MF</td>
<td>If there is a pending FPU exception.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#AC(0)</td>
<td>If alignment checking is enabled and an unaligned memory reference is made.</td>
</tr>
</tbody>
</table>
PACKUSWB—Pack with Unsigned Saturation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 67 /i</td>
<td>PACKUSWB mm, mm/m64</td>
<td>Pack and saturate 4 signed words from mm and 4 signed words from mm/m64 into 8 unsigned bytes in mm.</td>
</tr>
</tbody>
</table>

**Description**

Packs and saturates 4 signed words from the destination operand (first operand) and 4 signed words from the source operand (second operand) into 8 unsigned bytes in the destination operand (see Figure 2-4). If the signed value of a word is beyond the range of an unsigned byte (that is, greater than FFH or less than 00H), the saturated byte value of FFH or 00H, respectively, is stored into the destination.

The destination operand must be an MMX technology register; the source operand may be either an MMX technology register or a quadword memory location.

**Figure 2-4. Operation of the PACKUSWB Instruction**

![Figure 2-4. Operation of the PACKUSWB Instruction](3006014)

**Operation**

\[
\text{DEST}(.7..0) \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}(15..0);
\]

\[
\text{DEST}(15..8) \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}(31..16);
\]

\[
\text{DEST}(23..16) \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}(47..32);
\]

\[
\text{DEST}(31..24) \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{DEST}(63..48);
\]

\[
\text{DEST}(39..32) \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}(15..0);
\]

\[
\text{DEST}(47..40) \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}(31..16);
\]

\[
\text{DEST}(55..48) \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}(47..32);
\]

\[
\text{DEST}(63..56) \leftarrow \text{SaturateSignedWordToUnsignedByte} \text{SRC}(63..48);
\]

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

- **Itanium Reg Faults**: Disabled FP Register Fault if PSR.df1 is 1, NaT Register Consumption Abort.
- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
PACKUSWB—Pack with Unsigned Saturation (Continued)

Protected Mode Exceptions

- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#UD**: If EM in CR0 is set.
- **#NM**: If TS in CR0 is set.
- **#MF**: If there is a pending FPU exception.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

- **#GP**: If any part of the operand lies outside of the effective address space from 0 to FFFFH.
- **#UD**: If EM in CR0 is set.
- **#NM**: If TS in CR0 is set.
- **#MF**: If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

- **#GP**: If any part of the operand lies outside of the effective address space from 0 to FFFFH.
- **#UD**: If EM in CR0 is set.
- **#NM**: If TS in CR0 is set.
- **#MF**: If there is a pending FPU exception.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made.
PADDB/PADDW/PADDD—Packed Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F FC /r</td>
<td>PADDB mm, mm/m64</td>
<td>Add packed bytes from mm/m64 to packed bytes in mm.</td>
</tr>
<tr>
<td>0F FD /r</td>
<td>PADDW mm, mm/m64</td>
<td>Add packed words from mm/m64 to packed words in mm.</td>
</tr>
<tr>
<td>0F FE /r</td>
<td>PADDD mm, mm/m64</td>
<td>Add packed doublewords from mm/m64 to packed doublewords in mm.</td>
</tr>
</tbody>
</table>

Description

Adds the individual data elements (bytes, words, or doublewords) of the source operand (second operand) to the individual data elements of the destination operand (first operand). (See Figure 2-5.) If the result of an individual addition exceeds the range for the specified data type (overflows), the result is wrapped around, meaning that the result is truncated so that only the lower (least significant) bits of the result are returned (that is, the carry is ignored).

The destination operand must be an MMX technology register; the source operand can be either an MMX technology register or a quadword memory location.

Figure 2-5. Operation of the PADDW Instruction

The PADDB instruction adds the bytes of the source operand to the bytes of the destination operand and stores the results to the destination operand. When an individual result is too large to be represented in 8 bits, the lower 8 bits of the result are written to the destination operand and therefore the result wraps around.

The PADDW instruction adds the words of the source operand to the words of the destination operand and stores the results to the destination operand. When an individual result is too large to be represented in 16 bits, the lower 16 bits of the result are written to the destination operand and therefore the result wraps around.

The PADDD instruction adds the doublewords of the source operand to the doublewords of the destination operand and stores the results to the destination operand. When an individual result is too large to be represented in 32 bits, the lower 32 bits of the result are written to the destination operand and therefore the result wraps around.
PADDB/PADDW/PADDD—Packed Add (Continued)

Note that like the integer ADD instruction, the PADDB, PADDW, and PADDD instructions can operate on either unsigned or signed (two’s complement notation) packed integers. Unlike the integer instructions, none of the MMX instructions affect the EFLAGS register. With MMX instructions, there are no carry or overflow flags to indicate when overflow has occurred, so the software must control the range of values or else use the “with saturation” MMX instructions.

Operation

IF instruction is PADDB
THEN
  DEST(7..0) ← DEST(7..0) + SRC(7..0);
  DEST(15..8) ← DEST(15..8) + SRC(15..8);
  DEST(23..16) ← DEST(23..16) + SRC(23..16);
  DEST(31..24) ← DEST(31..24) + SRC(31..24);
  DEST(39..32) ← DEST(39..32) + SRC(39..32);
  DEST(47..40) ← DEST(47..40) + SRC(47..40);
  DEST(55..48) ← DEST(55..48) + SRC(55..48);
  DEST(63..56) ← DEST(63..56) + SRC(63..56);
ELSEIF instruction is PADDW
THEN
  DEST(15..0) ← DEST(15..0) + SRC(15..0);
  DEST(31..16) ← DEST(31..16) + SRC(31..16);
  DEST(47..32) ← DEST(47..32) + SRC(47..32);
  DEST(63..48) ← DEST(63..48) + SRC(63..48);
ELSE (* instruction is PADDD *)
  DEST(31..0) ← DEST(31..0) + SRC(31..0);
  DEST(63..32) ← DEST(63..32) + SRC(63..32);
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>Itanium Mem Faults</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>
PADDB/PADDW/PADDD—Packed Add (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
**PADDSB/PADDSW—Packed Add with Saturation**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F EC /r</td>
<td>PADDSB mm, mm/m64</td>
<td>Add signed packed bytes from mm/m64 to signed packed bytes in mm and saturate.</td>
</tr>
<tr>
<td>0F ED /r</td>
<td>PADDSW mm, mm/m64</td>
<td>Add signed packed words from mm/m64 to signed packed words in mm and saturate.</td>
</tr>
</tbody>
</table>

**Description**

Adds the individual signed data elements (bytes or words) of the source operand (second operand) to the individual signed data elements of the destination operand (first operand). (See Figure 2-6.) If the result of an individual addition exceeds the range for the specified data type, the result is saturated. The destination operand must be an MMX technology register; the source operand can be either an MMX technology register or a quadword memory location.

**Figure 2-6. Operation of the PADDSW Instruction**

The PADDSB instruction adds the signed bytes of the source operand to the signed bytes of the destination operand and stores the results to the destination operand. When an individual result is beyond the range of a signed byte (that is, greater than 7FH or less than 80H), the saturated byte value of 7FH or 80H, respectively, is written to the destination operand.

The PADDSW instruction adds the signed words of the source operand to the signed words of the destination operand and stores the results to the destination operand. When an individual result is beyond the range of a signed word (that is, greater than 7FFFH or less than 8000H), the saturated word value of 7FFFH or 8000H, respectively, is written to the destination operand.

**Operation**

IF instruction is PADDSB

THEN

DEST(7..0) ← SaturateToSignedByte(Dest(7..0) + SRC (7..0)) ;
DEST(15..8) ← SaturateToSignedByte(Dest(15..8) + SRC(15..8) );
DEST(23..16) ← SaturateToSignedByte(Dest(23..16)+ SRC(23..16) );
DEST(31..24) ← SaturateToSignedByte(Dest(31..24) + SRC(31..24) );
DEST(39..32) ← SaturateToSignedByte(Dest(39..32) + SRC(39..32) );
DEST(47..40) ← SaturateToSignedByte(Dest(47..40) + SRC(47..40) );
DEST(55..48) ← SaturateToSignedByte(Dest(55..48) + SRC(55..48) );
DEST(63..56) ← SaturateToSignedByte(Dest(63..56) + SRC(63..56) );
ELSE { (* instruction is PADDSW *) }


PADDSB/PADDSW—Packed Add with Saturation (Continued)

DEST(15..0) ← SaturateToSignedWord(DEST(15..0) + SRC(15..0) );

DEST(31..16) ← SaturateToSignedWord(DEST(31..16) + SRC(31..16) );
DEST(47..32) ← SaturateToSignedWord(DEST(47..32) + SRC(47..32) );
DEST(63..48) ← SaturateToSignedWord(DEST(63..48) + SRC(63..48) );
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#UD  If EM in CR0 is set.
#NM  If TS in CR0 is set.
#MF  If there is a pending FPU exception.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP  If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD  If EM in CR0 is set.
#NM  If TS in CR0 is set.
#MF  If there is a pending FPU exception.
PADDSB/PADDSW—Packed Add with Saturation (Continued)

**Virtual-8086 Mode Exceptions**

- **#GP**
  - If any part of the operand lies outside of the effective address space from 0 to FFFFH.
- **#UD**
  - If EM in CR0 is set.
- **#NM**
  - If TS in CR0 is set.
- **#MF**
  - If there is a pending FPU exception.
- **#PF(fault-code)**
  - If a page fault occurs.
- **#AC(0)**
  - If alignment checking is enabled and an unaligned memory reference is made.
PADDUSB/PADDUSW—Packed Add Unsigned with Saturation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F DC r</td>
<td>PADDUSB mm, mm/m64</td>
<td>Add unsigned packed bytes from mm/m64 to unsigned packed bytes in mm and saturate.</td>
</tr>
<tr>
<td>0F DD r</td>
<td>PADDUSW mm, mm/m64</td>
<td>Add unsigned packed words from mm/m64 to unsigned packed words in mm and saturate.</td>
</tr>
</tbody>
</table>

Description

Adds the individual unsigned data elements (bytes or words) of the packed source operand (second operand) to the individual unsigned data elements of the packed destination operand (first operand). (See Figure 2-7.) If the result of an individual addition exceeds the range for the specified unsigned data type, the result is saturated. The destination operand must be an MMX technology register; the source operand can be either an MMX technology register or a quadword memory location.

Figure 2-7. Operation of the PADDUSB Instruction

The PADDUSB instruction adds the unsigned bytes of the source operand to the unsigned bytes of the destination operand and stores the results to the destination operand. When an individual result is beyond the range of an unsigned byte (that is, greater than FFH), the saturated unsigned byte value of FFH is written to the destination operand.

The PADDUSW instruction adds the unsigned words of the source operand to the unsigned words of the destination operand and stores the results to the destination operand. When an individual result is beyond the range of an unsigned word (that is, greater than FFFFH), the saturated unsigned word value of FFFFH is written to the destination operand.
PADDUSB/PADDUSW—Packed Add Unsigned with Saturation (Continued)

**Operation**

IF instruction is PADDUSB
THEN

\[
\begin{align*}
\text{DEST}(7..0) & \gets \text{SaturateToUnsignedByte} (\text{DEST}(7..0) + \text{SRC}(7..0)) ; \\
\text{DEST}(15..8) & \gets \text{SaturateToUnsignedByte} (\text{DEST}(15..8) + \text{SRC}(15..8)) ; \\
\text{DEST}(23..16) & \gets \text{SaturateToUnsignedByte} (\text{DEST}(23..16) + \text{SRC}(23..16)) ; \\
\text{DEST}(31..24) & \gets \text{SaturateToUnsignedByte} (\text{DEST}(31..24) + \text{SRC}(31..24)) ; \\
\text{DEST}(39..32) & \gets \text{SaturateToUnsignedByte} (\text{DEST}(39..32) + \text{SRC}(39..32)) ; \\
\text{DEST}(47..40) & \gets \text{SaturateToUnsignedByte} (\text{DEST}(47..40) + \text{SRC}(47..40)) ; \\
\text{DEST}(55..48) & \gets \text{SaturateToUnsignedByte} (\text{DEST}(55..48) + \text{SRC}(55..48)) ; \\
\text{DEST}(63..56) & \gets \text{SaturateToUnsignedByte} (\text{DEST}(63..56) + \text{SRC}(63..56)) ; \\
\end{align*}
\]

ELSE { (* instruction is PADDUSW *)

\[
\begin{align*}
\text{DEST}(15..0) & \gets \text{SaturateToUnsignedWord} (\text{DEST}(15..0) + \text{SRC}(15..0)) ; \\
\text{DEST}(31..16) & \gets \text{SaturateToUnsignedWord} (\text{DEST}(31..16) + \text{SRC}(31..16)) ; \\
\text{DEST}(47..32) & \gets \text{SaturateToUnsignedWord} (\text{DEST}(47..32) + \text{SRC}(47..32)) ; \\
\text{DEST}(63..48) & \gets \text{SaturateToUnsignedWord} (\text{DEST}(63..48) + \text{SRC}(63..48)) ; \\
\end{align*}
\]

FI;

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

- *Itanium Reg Faults*: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- *Itanium Mem Faults*: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Protected Mode Exceptions**

- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#UD**: If EM in CR0 is set.
- **#NM**: If TS in CR0 is set.
- **#MF**: If there is a pending FPU exception.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
**PADDUSB/PADDUSW—Packed Add Unsigned with Saturation** (Continued)

**Real-Address Mode Exceptions**

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP</td>
<td>If any part of the operand lies outside of the effective address space from 0 to FFFFH.</td>
</tr>
<tr>
<td>#UD</td>
<td>If EM in CR0 is set.</td>
</tr>
<tr>
<td>#NM</td>
<td>If TS in CR0 is set.</td>
</tr>
<tr>
<td>#MF</td>
<td>If there is a pending FPU exception.</td>
</tr>
</tbody>
</table>

**Virtual-8086 Mode Exceptions**

<table>
<thead>
<tr>
<th>Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP</td>
<td>If any part of the operand lies outside of the effective address space from 0 to FFFFH.</td>
</tr>
<tr>
<td>#UD</td>
<td>If EM in CR0 is set.</td>
</tr>
<tr>
<td>#NM</td>
<td>If TS in CR0 is set.</td>
</tr>
<tr>
<td>#MF</td>
<td>If there is a pending FPU exception.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#AC(0)</td>
<td>If alignment checking is enabled and an unaligned memory reference is made.</td>
</tr>
</tbody>
</table>
PAND—Logical AND

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F DB /r</td>
<td>PAND mm, mm/m64</td>
<td>AND quadword from mm/m64 to quadword in mm.</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical AND operation on the quadword source (second) and destination (first) operands and stores the result in the destination operand location (see Figure 2-8). The source operand can be an MMX technology register or a quadword memory location; the destination operand must be an MMX technology register. Each bit of the result of the PAND instruction is set to 1 if the corresponding bits of the operands are both 1; otherwise it is made zero.

**Figure 2-8. Operation of the PAND Instruction**

```
        PAND mm, mm/m64
        mm  1111111111111000000000010110111010110001000011101110111011111
        &   0001000011011001010100000011000100011110111011100001011110011101
        mm  00010000110110000000000001000100100010101000100100010100000010110011
```

**Operation**

```
DEST ← DEST AND SRC;
```

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- Itanium Mem Faults: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
PAND—Logical AND (Continued)

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#UD    If EM in CR0 is set.
#NM    If TS in CR0 is set.
#MF    If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP    If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD    If EM in CR0 is set.
#NM    If TS in CR0 is set.
#MF    If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP    If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD    If EM in CR0 is set.
#NM    If TS in CR0 is set.
#MF    If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PANDN—Logical AND NOT

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F DF /r</td>
<td>PANDN mm, mm/m64</td>
<td>AND quadword from mm/m64 to NOT quadword in mm.</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical NOT on the quadword destination operand (first operand). Then, the instruction performs a bitwise logical AND operation on the inverted destination operand and the quadword source operand (second operand). (See Figure 2-9.) Each bit of the result of the AND operation is set to one if the corresponding bits of the source and inverted destination bits are one; otherwise it is set to zero. The result is stored in the destination operand location.

The source operand can be an MMX technology register or a quadword memory location; the destination operand must be an MMX technology register.

**Figure 2-9. Operation of the PANDN Instruction**

```
<table>
<thead>
<tr>
<th>opcode Instruction Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PANDN mm, mm/m64</td>
</tr>
<tr>
<td>~</td>
</tr>
<tr>
<td>mm</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>m/m64</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>mm</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>
```

**Operation**

DEST ← (NOT DEST) AND SRC;

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

<table>
<thead>
<tr>
<th>Itanium Reg Faults</th>
<th>Itanium Mem Faults</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>
PANDN—Logical AND NOT (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS
segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made
while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to
FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to
FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PCMPEQB/PCMPEQW/PCMPEQD—Packed Compare for Equal

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 74 <code>/r</code></td>
<td>PCMPEQB <code>mm, mm/m64</code></td>
<td>Compare packed bytes in <code>mm/m64</code> with packed bytes in <code>mm</code> for equality.</td>
</tr>
<tr>
<td>0F 75 <code>/r</code></td>
<td>PCMPEQW <code>mm, mm/m64</code></td>
<td>Compare packed words in <code>mm/m64</code> with packed words in <code>mm</code> for equality.</td>
</tr>
<tr>
<td>0F 76 <code>/r</code></td>
<td>PCMPEQD <code>mm, mm/m64</code></td>
<td>Compare packed doublewords in <code>mm/m64</code> with packed doublewords in <code>mm</code> for equality.</td>
</tr>
</tbody>
</table>

Description

Compares the individual data elements (bytes, words, or doublewords) in the destination operand (first operand) to the corresponding data elements in the source operand (second operand). (See Figure 2-10.) If a pair of data elements are equal, the corresponding data element in the destination operand is set to all ones; otherwise, it is set to all zeros. The destination operand must be an MMX technology register; the source operand may be either an MMX technology register or a 64-bit memory location.

Figure 2-10. Operation of the PCMPEQW Instruction

The PCMPEQB instruction compares the bytes in the destination operand to the corresponding bytes in the source operand, with the bytes in the destination operand being set according to the results.

The PCMPEQW instruction compares the words in the destination operand to the corresponding words in the source operand, with the words in the destination operand being set according to the results.

The PCMPEQD instruction compares the doublewords in the destination operand to the corresponding doublewords in the source operand, with the doublewords in the destination operand being set according to the results.
PCMPEQB/PCMPEQW/PCMPEQD—Packed Compare for Equal (Continued)

Operation

IF instruction is PCMPEQB

THEN

IF DEST(7..0) = SRC(7..0)

THEN DEST(7 0) ← FFH;
ELSE DEST(7..0) ← 0;

* Continue comparison of second through seventh bytes in DEST and SRC *

IF DEST(63..56) = SRC(63..56)

THEN DEST(63..56) ← FFH;
ELSE DEST(63..56) ← 0;

ELSE IF instruction is PCMPEQW

THEN

IF DEST(15..0) = SRC(15..0)

THEN DEST(15..0) ← FFFFH;
ELSE DEST(15..0) ← 0;

* Continue comparison of second and third words in DEST and SRC *

IF DEST(63..48) = SRC(63..48)

THEN DEST(63..48) ← FFFFH;
ELSE DEST(63..48) ← 0;

ELSE (* instruction is PCMPEQD *)

IF DEST(31..0) = SRC(31..0)

THEN DEST(31..0) ← FFFFFFFFH;
ELSE DEST(31..0) ← 0;

IF DEST(63..32) = SRC(63..32)

THEN DEST(63..32) ← FFFFFFFFH;
ELSE DEST(63..32) ← 0;

FI;

Flags Affected

None:

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.

#SS(0)  If a memory operand effective address is outside the SS segment limit.

#UD  If EM in CR0 is set.

#NM  If TS in CR0 is set.

#MF  If there is a pending FPU exception.

#PF(fault-code)  If a page fault occurs.
PCMP_EQB/PCMP_EQW/PCMP_EQD—Packed Compare for Equal (Continued)

#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PCMPGTB/PCMPGTW/PCMPGTD—Packed Compare for Greater Than

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 64 /r</td>
<td>PCMPGTB mm, mm/m64</td>
<td>Compare packed bytes in mm with packed bytes in mm/m64 for greater value.</td>
</tr>
<tr>
<td>0F 65 /r</td>
<td>PCMPGTW mm, mm/m64</td>
<td>Compare packed words in mm with packed words in mm/m64 for greater value.</td>
</tr>
<tr>
<td>0F 66 /r</td>
<td>PCMPGTD mm, mm/m64</td>
<td>Compare packed doublewords in mm with packed doublewords in mm/m64 for greater value.</td>
</tr>
</tbody>
</table>

Description

Compare the individual signed data elements (bytes, words, or doublewords) in the destination operand (first operand) to the corresponding signed data elements in the source operand (second operand). (See Figure 2-11.) If a data element in the destination operand is greater than its corresponding data element in the source operand, the data element in the destination operand is set to all ones; otherwise, it is set to all zeros. The destination operand must be an MMX technology register; the source operand may be either an MMX technology register or a 64-bit memory location.

Figure 2-11. Operation of the PCMPGTW Instruction

The PCMPGTB instruction compares the signed bytes in the destination operand to the corresponding signed bytes in the source operand, with the bytes in the destination operand being set according to the results.

The PCMPGTW instruction compares the signed words in the destination operand to the corresponding signed words in the source operand, with the words in the destination operand being set according to the results.

The PCMPGTD instruction compares the signed doublewords in the destination operand to the corresponding signed doublewords in the source operand, with the doublewords in the destination operand being set according to the results.
PCMPGTB/PCMPGTW/PCMPGTD—Packed Compare for Greater Than
(Continued)

Operation

IF instruction is PCMPGTB
THEN
  IF DEST(7..0) > SRC(7..0)
    THEN DEST(7..0) ← FFH;
    ELSE DEST(7..0) ← 0;
    * Continue comparison of second through seventh bytes in DEST and SRC *
    IF DEST(63..56) > SRC(63..56)
      THEN DEST(63..56) ← FFH;
      ELSE DEST(63..56) ← 0;
ELSE IF instruction is PCMPGTW
THEN
  IF DEST(15..0) > SRC(15..0)
    THEN DEST(15..0) ← FFFFH;
    ELSE DEST(15..0) ← 0;
    * Continue comparison of second and third bytes in DEST and SRC *
    IF DEST(63..48) > SRC(63..48)
      THEN DEST(63..48) ← FFFFH;
      ELSE DEST(63..48) ← 0;
ELSE { (* instruction is PCMPGTD *)
  IF DEST(31..0) > SRC(31..0)
    THEN DEST(31..0) ← FFFFFFFFH;
    ELSE DEST(31..0) ← 0;
    IF DEST(63..32) > SRC(63..32)
      THEN DEST(63..32) ← FFFFFFFFH;
      ELSE DEST(63..32) ← 0;
  FI;
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.df1 is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
PCMPGTB/PCMPGTW/PCMPGTD—Packed Compare for Greater Than
(Continued)

**Protected Mode Exceptions**

- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #UD If EM in CR0 is set.
- #NM If TS in CR0 is set.
- #MF If there is a pending FPU exception.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- #GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
- #UD If EM in CR0 is set.
- #NM If TS in CR0 is set.
- #MF If there is a pending FPU exception.

**Virtual-8086 Mode Exceptions**

- #GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
- #UD If EM in CR0 is set.
- #NM If TS in CR0 is set.
- #MF If there is a pending FPU exception.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PMADDWD—Packed Multiply and Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F F5 /r</td>
<td>PMADDWD mm, mm/m64</td>
<td>Multiply the packed words in mm by the packed words in mm/m64. Add the 32-bit pairs of results and store in mm as doubleword</td>
</tr>
</tbody>
</table>

**Description**

Multiplies the individual signed words of the destination operand by the corresponding signed words of the source operand, producing four signed, doubleword results (see Figure 2-12). The two doubleword results from the multiplication of the high-order words are added together and stored in the upper doubleword of the destination operand; the two doubleword results from the multiplication of the low-order words are added together and stored in the lower doubleword of the destination operand. The destination operand must be an MMX technology register; the source operand may be either an MMX technology register or a 64-bit memory location.

The PMADDWD instruction wraps around to 80000000H only when all four words of both the source and destination operands are 8000H.

**Figure 2-12. Operation of the PMADDWD Instruction**

```
<table>
<thead>
<tr>
<th>mm</th>
<th>0111000111000111</th>
<th>0111000111000111</th>
</tr>
</thead>
<tbody>
<tr>
<td>*</td>
<td>*</td>
<td>*</td>
</tr>
<tr>
<td>mm/m64</td>
<td>1000000000000000</td>
<td>0000010000000000</td>
</tr>
<tr>
<td>+</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>mm</td>
<td>1100100011100011</td>
<td>1001110000000000</td>
</tr>
</tbody>
</table>
```

**Operation**

\[
\text{DEST}(31..0) \leftarrow (\text{DEST}(15..0) \times \text{SRC}(15..0)) + (\text{DEST}(31..16) \times \text{SRC}(31..16));
\]

\[
\text{DEST}(63..32) \leftarrow (\text{DEST}(47..32) \times \text{SRC}(47..32)) + (\text{DEST}(63..48) \times \text{SRC}(63..48));
\]

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

- **Itanium Reg Faults**: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
PMADDWD—Packed Multiply and Add (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PMULHW—Packed Multiply High

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F E5 /r</td>
<td>PMULHW mm, mm/m64</td>
<td>Multiply the signed packed words in mm by the signed packed words in mm/m64, then store the high-order word of each doubleword result in mm.</td>
</tr>
</tbody>
</table>

**Description**

Multiplies the four signed words of the source operand (second operand) by the four signed words of the destination operand (first operand), producing four signed, doubleword, intermediate results (see Figure 2-13). The high-order word of each intermediate result is then written to its corresponding word location in the destination operand. The destination operand must be an MMX technology register; the source operand may be either an MMX technology register or a 64-bit memory location.

**Figure 2-13. Operation of the PMULHW Instruction**

```
PMULHW mm, mm/m64
```

<table>
<thead>
<tr>
<th>mm</th>
<th>mm/m64</th>
<th>mm</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0111000111000111</td>
<td>0111000111000111</td>
<td>11000111000111</td>
</tr>
<tr>
<td></td>
<td>1000000000000000</td>
<td>0000000111000111</td>
</tr>
<tr>
<td>High Order</td>
<td>High Order</td>
<td>High Order</td>
</tr>
<tr>
<td>High Order</td>
<td>High Order</td>
<td>High Order</td>
</tr>
</tbody>
</table>

**Operation**

\[
\text{DEST}(15..0) \leftarrow \text{HighOrderWord}(\text{DEST}(15..0) \times \text{SRC}(15..0));
\]
\[
\text{DEST}(31..16) \leftarrow \text{HighOrderWord}(\text{DEST}(31..16) \times \text{SRC}(31..16));
\]
\[
\text{DEST}(47..32) \leftarrow \text{HighOrderWord}(\text{DEST}(47..32) \times \text{SRC}(47..32));
\]
\[
\text{DEST}(63..48) \leftarrow \text{HighOrderWord}(\text{DEST}(63..48) \times \text{SRC}(63..48));
\]

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

- **Itanium Reg Faults**
  - Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- **Itanium Mem Faults**
  - VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
PMULHW—Packed Multiply High (Continued)

Protected Mode Exceptions

- #GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
- #SS(0) If a memory operand effective address is outside the SS segment limit.
- #UD If EM in CR0 is set.
- #NM If TS in CR0 is set.
- #MF If there is a pending FPU exception.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

- #GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
- #UD If EM in CR0 is set.
- #NM If TS in CR0 is set.
- #MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

- #GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
- #UD If EM in CR0 is set.
- #NM If TS in CR0 is set.
- #MF If there is a pending FPU exception.
- #PF(fault-code) If a page fault occurs.
- #AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PMULLW—Packed Multiply Low

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F D5 /r</td>
<td>PMULLW mm, mm/m64</td>
<td>Multiply the packed words in mm with the packed words in mm/m64, then store the low-order word of each doubleword result in mm.</td>
</tr>
</tbody>
</table>

**Description**

Multiplies the four signed or unsigned words of the source operand (second operand) with the four signed or unsigned words of the destination operand (first operand), producing four doubleword, intermediate results (see Figure 2-14). The low-order word of each intermediate result is then written to its corresponding word location in the destination operand. The destination operand must be an MMX technology register; the source operand may be either an MMX technology register or a 64-bit memory location.

**Figure 2-14. Operation of the PMULLW Instruction**

![Figure 2-14](image)

**Operation**

DEST(15..0) ← LowOrderWord(DEST(15..0) × SRC(15..0));
DEST(31..16) ← LowOrderWord(DEST(31..16) × SRC(31..16));
DEST(47..32) ← LowOrderWord(DEST(47..32) × SRC(47..32));
DEST(63..48) ← LowOrderWord(DEST(63..48) × SRC(63..48));

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, Nat Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data Nat Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
PMULLW—Packed Multiply Low (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
POR—Bitwise Logical OR

### Description

Performs a bitwise logical OR operation on the quadword source (second) and destination (first) operands and stores the result in the destination operand location (see Figure 2-15). The source operand can be an MMX technology register or a quadword memory location; the destination operand must be an MMX technology register. Each bit of the result is made 0 if the corresponding bits of both operands are 0; otherwise the bit is set to 1.

### Figure 2-15. Operation of the POR Instruction.

![ POR mm, mm/m64

<table>
<thead>
<tr>
<th>mm</th>
<th>mm/m64</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111111111111000000000000000010110110101100010001111011101110111</td>
<td>0001000011011001010100000011000100011110111011110001010110010101</td>
</tr>
<tr>
<td></td>
<td>111111111111100101010000001101011011111111101110111011111110111</td>
</tr>
</tbody>
</table>

### Operation

DEST ← DEST OR SRC;

### Flags Affected

None.

### Additional Itanium® System Environment Exceptions

- **Itanium Reg Faults**: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

---

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POR—Bitwise Logical OR (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PSLLW/PSLLD/PSLLQ—Packed Shift Left Logical

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F F1/r</td>
<td>PSLLW mm, mm/m64</td>
<td>Shift words in mm left by amount specified in mm/m64, while shifting in zeros.</td>
</tr>
<tr>
<td>0F 71 /6, ib</td>
<td>PSLLW mm, imm8</td>
<td>Shift words in mm left by imm8, while shifting in zeros.</td>
</tr>
<tr>
<td>0F F2/r</td>
<td>PSLLD mm, mm/m64</td>
<td>Shift doublewords in mm left by amount specified in mm/m64, while shifting in zeros.</td>
</tr>
<tr>
<td>0F 72 /6 ib</td>
<td>PSLLD mm, imm8</td>
<td>Shift doublewords in mm by imm8, while shifting in zeros.</td>
</tr>
<tr>
<td>0F F3 /r</td>
<td>PSLLQ mm, mm/m64</td>
<td>Shift mm left by amount specified in mm/m64, while shifting in zeros.</td>
</tr>
<tr>
<td>0F 73 /6 ib</td>
<td>PSLLQ mm, imm8</td>
<td>Shift mm left by Imm8, while shifting in zeros.</td>
</tr>
</tbody>
</table>

Description

Shifts the bits in the data elements (words, doublewords, or quadword) in the destination operand (first operand) to the left by the number of bits specified in the unsigned count operand (second operand). (See Figure 2-16.) The result of the shift operation is written to the destination operand. As the bits in the data elements are shifted left, the empty low-order bits are cleared (set to zero). If the value specified by the count operand is greater than 15 (for words), 31 (for doublewords), or 63 (for a quadword), then the destination operand is set to all zeros.

The destination operand must be an MMX technology register; the count operand can be either an MMX technology register, a 64-bit memory location, or an 8-bit immediate.

The PSLLW instruction shifts each of the four words of the destination operand to the left by the number of bits specified in the count operand; the PSLLD instruction shifts each of the two doublewords of the destination operand; and the PSLLQ instruction shifts the 64-bit quadword in the destination operand. As the individual data elements are shifted left, the empty low-order bit positions are filled with zeros.

Figure 2-16. Operation of the PSLLW Instruction
PSLLW/PSLLD/PSLLQ—Packed Shift Left Logical (Continued)

**Operation**

IF instruction is PSLLW

THEN

\[
\begin{align*}
\text{DEST}(15..0) & \leftarrow \text{DEST}(15..0) \ll \text{COUNT}; \\
\text{DEST}(31..16) & \leftarrow \text{DEST}(31..16) \ll \text{COUNT}; \\
\text{DEST}(47..32) & \leftarrow \text{DEST}(47..32) \ll \text{COUNT}; \\
\text{DEST}(63..48) & \leftarrow \text{DEST}(63..48) \ll \text{COUNT};
\end{align*}
\]

ELSE IF instruction is PSLLD

THEN {

\[
\begin{align*}
\text{DEST}(31..0) & \leftarrow \text{DEST}(31..0) \ll \text{COUNT}; \\
\text{DEST}(63..32) & \leftarrow \text{DEST}(63..32) \ll \text{COUNT};
\end{align*}
\]

ELSE (* instruction is PSLLQ *)

\[
\text{DEST} \leftarrow \text{DEST} \ll \text{COUNT};
\]

FI;

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

<table>
<thead>
<tr>
<th>Category</th>
<th>Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>Itanium Reg Faults</td>
<td>Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.</td>
</tr>
<tr>
<td>Itanium Mem Faults</td>
<td>VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault</td>
</tr>
</tbody>
</table>

**Protected Mode Exceptions**

- **#GP(0)**: If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
- **#SS(0)**: If a memory operand effective address is outside the SS segment limit.
- **#UD**: If EM in CR0 is set.
- **#NM**: If TS in CR0 is set.
- **#MF**: If there is a pending FPU exception.
- **#PF(fault-code)**: If a page fault occurs.
- **#AC(0)**: If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

**Real-Address Mode Exceptions**

- **#GP**: If any part of the operand lies outside of the effective address space from 0 to FFFFFFFH.
- **#UD**: If EM in CR0 is set.
- **#NM**: If TS in CR0 is set.
- **#MF**: If there is a pending FPU exception.
PSLLW/PSLLD/PSLLQ—Packed Shift Left Logical (Continued)

Virtual-8086 Mode Exceptions

<table>
<thead>
<tr>
<th>Exception Code</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP</td>
<td>If any part of the operand lies outside of the effective address space from 0 to FFFFH.</td>
</tr>
<tr>
<td>#UD</td>
<td>If EM in CR0 is set.</td>
</tr>
<tr>
<td>#NM</td>
<td>If TS in CR0 is set.</td>
</tr>
<tr>
<td>#MF</td>
<td>If there is a pending FPU exception.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#AC(0)</td>
<td>If alignment checking is enabled and an unaligned memory reference is made.</td>
</tr>
</tbody>
</table>
PSRAW/PSRAD—Packed Shift Right Arithmetic

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F E1 /r</td>
<td>PSRAW mm, mm/m64</td>
<td>Shift words in mm right by amount specified in mm/m64 while shifting in sign bits.</td>
</tr>
<tr>
<td>0F 71 /4 ib</td>
<td>PSRAW mm, imm8</td>
<td>Shift words in mm right by imm8 while shifting in sign bits</td>
</tr>
<tr>
<td>0F E2 /r</td>
<td>PSRAD mm, mm/m64</td>
<td>Shift doublewords in mm right by amount specified in mm/m64 while shifting in sign bits.</td>
</tr>
<tr>
<td>0F 72 /4 ib</td>
<td>PSRAD mm, imm8</td>
<td>Shift doublewords in mm right by imm8 while shifting in sign bits.</td>
</tr>
</tbody>
</table>

**Description**

Shifts the bits in the data elements (words or doublewords) in the destination operand (first operand) to the right by the amount of bits specified in the unsigned count operand (second operand). (See Figure 2-17.) The result of the shift operation is written to the destination operand. The empty high-order bits of each element are filled with the initial value of the sign bit of the data element. If the value specified by the count operand is greater than 15 (for words) or 31 (for doublewords), each destination data element is filled with the initial value of the sign bit of the element.

The destination operand must be an MMX technology register; the count operand (source operand) can be either an MMX technology register, a 64-bit memory location, or an 8-bit immediate.

The PSRAW instruction shifts each of the four words in the destination operand to the right by the number of bits specified in the count operand; the PSRAD instruction shifts each of the two doublewords in the destination operand. As the individual data elements are shifted right, the empty high-order bit positions are filled with the sign value.

**Figure 2-17. Operation of the PSRAW Instruction**

![Figure 2-17. Operation of the PSRAW Instruction](image_url)
PSRAW/PSRAD—Packed Shift Right Arithmetic (Continued)

Operation
IF instruction is PSRAW
THEN
    DEST(15..0) ← SignExtend (DEST(15..0) >> COUNT);
    DEST(31..16) ← SignExtend (DEST(31..16) >> COUNT);
    DEST(47..32) ← SignExtend (DEST(47..32) >> COUNT);
    DEST(63..48) ← SignExtend (DEST(63..48) >> COUNT);
ELSE ( "instruction is PSRAD ")
    DEST(31..0) ← SignExtend (DEST(31..0) >> COUNT);
    DEST(63..32) ← SignExtend (DEST(63..32) >> COUNT);
FI;

Flags Affected
None.

Additional Itanium® System Environment Exceptions
Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions
#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions
#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
**PSRAW/PSRAD—Packed Shift Right Arithmetic (Continued)**

**Virtual-8086 Mode Exceptions**

<table>
<thead>
<tr>
<th>Code</th>
<th>Exception Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>#GP</td>
<td>If any part of the operand lies outside of the effective address space from 0 to FFFFH.</td>
</tr>
<tr>
<td>#UD</td>
<td>If EM in CR0 is set.</td>
</tr>
<tr>
<td>#NM</td>
<td>If TS in CR0 is set.</td>
</tr>
<tr>
<td>#MF</td>
<td>If there is a pending FPU exception.</td>
</tr>
<tr>
<td>#PF(fault-code)</td>
<td>If a page fault occurs.</td>
</tr>
<tr>
<td>#AC(0)</td>
<td>If alignment checking is enabled and an unaligned memory reference is made.</td>
</tr>
</tbody>
</table>
PSRLW/PSRLD/PSRLQ—Packed Shift Right Logical

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F D1 /r</td>
<td>PSRLW mm, mm/m64</td>
<td>Shift words in mm right by amount specified in mm/m64 while shifting in zeros.</td>
</tr>
<tr>
<td>0F 71 /2ib</td>
<td>PSRLW mm, imm8</td>
<td>Shift words in mm right by imm8.</td>
</tr>
<tr>
<td>0F D2 /r</td>
<td>PSRLD mm, mm/m64</td>
<td>Shift doublewords in mm right by amount specified in mm/m64 while shifting in zeros.</td>
</tr>
<tr>
<td>0F 72 /2ib</td>
<td>PSRLD mm, imm8</td>
<td>Shift doublewords in mm right by imm8.</td>
</tr>
<tr>
<td>0F D3 /r</td>
<td>PSRLQ mm, mm/m64</td>
<td>Shift mm right by amount specified in mm/m64 while shifting in zeros.</td>
</tr>
<tr>
<td>0F 73 /2ib</td>
<td>PSRLQ mm, imm8</td>
<td>Shift mm right by imm8 while shifting in zeros.</td>
</tr>
</tbody>
</table>

Description

Shifts the bits in the data elements (words, doublewords, or quadword) in the destination operand (first operand) to the right by the number of bits specified in the unsigned count operand (second operand). (See Figure 2-18.) The result of the shift operation is written to the destination operand. As the bits in the data elements are shifted right, the empty high-order bits are cleared (set to zero). If the value specified by the count operand is greater than 15 (for words), 31 (for doublewords), or 63 (for a quadword), then the destination operand is set to all zeros.

The destination operand must be an MMX technology register; the count operand can be either an MMX technology register, a 64-bit memory location, or an 8-bit immediate.

The PSRLW instruction shifts each of the four words of the destination operand to the right by the number of bits specified in the count operand; the PSRLD instruction shifts each of the two doublewords of the destination operand; and the PSRLQ instruction shifts the 64-bit quadword in the destination operand. As the individual data elements are shifted right, the empty high-order bit positions are filled with zeros.

Figure 2-18. Operation of the PSRLW Instruction
PSRLW/PSRLD/PSRLQ—Packed Shift Right Logical (Continued)

Operation

IF instruction is PSRLW
THEN {
    DEST(15..0) ← DEST(15..0) >> COUNT;
    DEST(31..16) ← DEST(31..16) >> COUNT;
    DEST(47..32) ← DEST(47..32) >> COUNT;
    DEST(63..48) ← DEST(63..48) >> COUNT;
}
ELSE IF instruction is PSRLD
THEN {
    DEST(31..0) ← DEST(31..0) >> COUNT;
    DEST(63..32) ← DEST(63..32) >> COUNT;
}
ELSE (* instruction is PSRLQ *)
    DEST ← DEST >> COUNT;
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#UD     If EM in CR0 is set.
#NM     If TS in CR0 is set.
#MF     If there is a pending FPU exception.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP     If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD     If EM in CR0 is set.
#NM     If TS in CR0 is set.
#MF     If there is a pending FPU exception.
Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.

#UD If EM in CR0 is set.

#NM If TS in CR0 is set.

#MF If there is a pending FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PSUBB/PSUBW/PSUBD—Packed Subtract

### Description

Subtracts the individual data elements (bytes, words, or doublewords) of the source operand (second operand) from the individual data elements of the destination operand (first operand). (See Figure 2-19.) If the result of a subtraction exceeds the range for the specified data type (overflows), the result is wrapped around, meaning that the result is truncated so that only the lower (least significant) bits of the result are returned (that is, the carry is ignored).

The destination operand must be an MMX technology register; the source operand can be either an MMX technology register or a quadword memory location.

#### Figure 2-19. Operation of the PSUBW Instruction

The PSUBB instruction subtracts the bytes of the source operand from the bytes of the destination operand and stores the results to the destination operand. When an individual result is too large to be represented in 8 bits, the lower 8 bits of the result are written to the destination operand and therefore the result wraps around.

The PSUBW instruction subtracts the words of the source operand from the words of the destination operand and stores the results to the destination operand. When an individual result is too large to be represented in 16 bits, the lower 16 bits of the result are written to the destination operand and therefore the result wraps around.

The PSUBD instruction subtracts the doublewords of the source operand from the doublewords of the destination operand and stores the results to the destination operand. When an individual result is too large to be represented in 32 bits, the lower 32 bits of the result are written to the destination operand and therefore the result wraps around.

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F F8 /r</td>
<td>PSUBB mm, mm/m64</td>
<td>Subtract packed bytes in mm/m64 from packed bytes in mm.</td>
</tr>
<tr>
<td>0F F9 /r</td>
<td>PSUBW mm, mm/m64</td>
<td>Subtract packed words in mm/m64 from packed words in mm.</td>
</tr>
<tr>
<td>0F FA /r</td>
<td>PSUBD mm, mm/m64</td>
<td>Subtract packed doublewords in mm/m64 from packed doublewords in mm.</td>
</tr>
</tbody>
</table>
PSUBB/PSUBW/PSUBD—Packed Subtract (Continued)

Note that like the integer SUB instruction, the PSUBB, PSUBW, and PSUBD instructions can operate on either unsigned or signed (two’s complement notation) packed integers. Unlike the integer instructions, none of the MMX instructions affect the EFLAGS register. With MMX instructions, there are no carry or overflow flags to indicate when overflow has occurred, so the software must control the range of values or else use the “with saturation” MMX instructions.

Operation

IF instruction is PSUBB
THEN
    DEST(7..0) ← DEST(7..0) – SRC(7..0);
    DEST(15..8) ← DEST(15..8) – SRC(15..8);
    DEST(23..16) ← DEST(23..16) – SRC(23..16);
    DEST(31..24) ← DEST(31..24) – SRC(31..24);
    DEST(39..32) ← DEST(39..32) – SRC(39..32);
    DEST(47..40) ← DEST(47..40) – SRC(47..40);
    DEST(55..48) ← DEST(55..48) – SRC(55..48);
    DEST(63..56) ← DEST(63..56) – SRC(63..56);
ELSEIF instruction is PSUBW
THEN
    DEST(15..0) ← DEST(15..0) – SRC(15..0);
    DEST(31..16) ← DEST(31..16) – SRC(31..16);
    DEST(47..32) ← DEST(47..32) – SRC(47..32);
    DEST(63..48) ← DEST(63..48) – SRC(63..48);
ELSE { (* instruction is PSUBD *)
    DEST(31..0) ← DEST(31..0) – SRC(31..0);
    DEST(63..32) ← DEST(63..32) – SRC(63..32);
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
PSUBB/PSUBW/PSUBD—Packed Subtract (Continued)

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
**PSUBSB/PSUBSW—Packed Subtract with Saturation**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F E8</td>
<td>PSUBSB mm, mm/m64</td>
<td>Subtract signed packed bytes in mm/m64 from signed packed bytes in mm and saturate.</td>
</tr>
<tr>
<td>0F E9</td>
<td>PSUBSW mm, mm/m64</td>
<td>Subtract signed packed words in mm/m64 from signed packed words in mm and saturate.</td>
</tr>
</tbody>
</table>

**Description**

Subtracts the individual signed data elements (bytes or words) of the source operand (second operand) from the individual signed data elements of the destination operand (first operand). (See Figure 2-20.) If the result of a subtraction exceeds the range for the specified data type, the result is saturated. The destination operand must be an MMX technology register; the source operand can be either an MMX technology register or a quadword memory location.

**Figure 2-20. Operation of the PSUBSW Instruction**

The PSUBSB instruction subtracts the signed bytes of the source operand from the signed bytes of the destination operand and stores the results to the destination operand. When an individual result is beyond the range of a signed byte (that is, greater than 7FH or less than 80H), the saturated byte value of 7FH or 80H, respectively, is written to the destination operand.

The PSUBSW instruction subtracts the signed words of the source operand from the signed words of the destination operand and stores the results to the destination operand. When an individual result is beyond the range of a signed word (that is, greater than 7FFFH or less than 8000H), the saturated word value of 7FFFH or 8000H, respectively, is written to the destination operand.
PSUBSB/PSUBSW—Packed Subtract with Saturation (Continued)

Operation

IF instruction is PSUBSB
THEN
  DEST(7..0) ← SaturateToSignedByte(DEST(7..0) – SRC(7..0));
  DEST(15..8) ← SaturateToSignedByte(DEST(15..8) – SRC(15..8));
  DEST(23..16) ← SaturateToSignedByte(DEST(23..16) – SRC(23..16));
  DEST(31..24) ← SaturateToSignedByte(DEST(31..24) – SRC(31..24));
  DEST(39..32) ← SaturateToSignedByte(DEST(39..32) – SRC(39..32));
  DEST(47..40) ← SaturateToSignedByte(DEST(47..40) – SRC(47..40));
  DEST(55..48) ← SaturateToSignedByte(DEST(55..48) – SRC(55..48));
  DEST(63..56) ← SaturateToSignedByte(DEST(63..56) – SRC(63..56))
ELSE (* instruction is PSUBSW *)
  DEST(15..0) ← SaturateToSignedWord(DEST(15..0) – SRC(15..0));
  DEST(31..16) ← SaturateToSignedWord(DEST(31..16) – SRC(31..16));
  DEST(47..32) ← SaturateToSignedWord(DEST(47..32) – SRC(47..32));
  DEST(63..48) ← SaturateToSignedWord(DEST(63..48) – SRC(63..48));
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
PSUBSB/PSUBSW—Packed Subtract with Saturation (Continued)

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PSUBUSB/PSUBUSW—Packed Subtract Unsigned with Saturation

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F D8 /r</td>
<td>PSUBUSB mm, mm/m64</td>
<td>Subtract unsigned packed bytes in mm/m64 from unsigned packed bytes in mm and saturate.</td>
</tr>
<tr>
<td>0F D9 /r</td>
<td>PSUBUSW mm, mm/m64</td>
<td>Subtract unsigned packed words in mm/m64 from unsigned packed words in mm and saturate.</td>
</tr>
</tbody>
</table>

Description

Subtracts the individual unsigned data elements (bytes or words) of the source operand (second operand) from the individual unsigned data elements of the destination operand (first operand). (See Figure 2-21.) If the result of an individual subtraction exceeds the range for the specified unsigned data type, the result is saturated. The destination operand must be an MMX technology register; the source operand can be either an MMX technology register or a quadword memory location.

Figure 2-21. Operation of the PSUBUSB Instruction

The PSUBUSB instruction subtracts the unsigned bytes of the source operand from the unsigned bytes of the destination operand and stores the results to the destination operand. When an individual result is less than zero (a negative value), the saturated unsigned byte value of 00H is written to the destination operand.

The PSUBUSW instruction subtracts the unsigned words of the source operand from the unsigned words of the destination operand and stores the results to the destination operand. When an individual result is less than zero (a negative value), the saturated unsigned word value of 0000H is written to the destination operand.
PSUBUSB/PSUBUSW—Packed Subtract Unsigned with Saturation
(Continued)

Operation

IF instruction is PSUBUSB
  THEN
    DEST(7..0) ← SaturateToUnsignedByte (DEST(7..0) – SRC (7..0) );
    DEST(15..8) ← SaturateToUnsignedByte ( DEST(15..8) – SRC(15..8) );
    DEST(23..16) ← SaturateToUnsignedByte (DEST(23..16) – SRC(23..16) );
    DEST(31..24) ← SaturateToUnsignedByte (DEST(31..24) – SRC(31..24) );
    DEST(39..32) ← SaturateToUnsignedByte (DEST(39..32) – SRC(39..32) );
    DEST(47..40) ← SaturateToUnsignedByte (DEST(47..40) – SRC(47..40) );
    DEST(55..48) ← SaturateToUnsignedByte (DEST(55..48) – SRC(55..48) );
    DEST(63..56) ← SaturateToUnsignedByte (DEST(63..56) – SRC(63..56) );
  ELSE { (* instruction is PSUBUSW *)
    DEST(15..0) ← SaturateToUnsignedWord (DEST(15..0) – SRC(15..0) );
    DEST(31..16) ← SaturateToUnsignedWord (DEST(31..16) – SRC(31..16) );
    DEST(47..32) ← SaturateToUnsignedWord (DEST(47..32) – SRC(47..32) );
    DEST(63..48) ← SaturateToUnsignedWord (DEST(63..48) – SRC(63..48) );
  FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults  VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#UD    If EM in CR0 is set.
#NM    If TS in CR0 is set.
#MF    If there is a pending FPU exception.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
PSUBUSB/PSUBUSW—Packed Subtract Unsigned with Saturation
(Continued)

Real-Address Mode Exceptions

#GP   If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD   If EM in CR0 is set.
#NM   If TS in CR0 is set.
#MF   If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP   If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD   If EM in CR0 is set.
#NM   If TS in CR0 is set.
#MF   If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PUNPCKHBW/PUNPCKHWD/PUNPCKHDQ—Unpack High Packed Data

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F 68</td>
<td>PUNPCKHBW mm, mm/m64</td>
<td>Interleave high-order bytes from mm and mm/m64 into mm.</td>
</tr>
<tr>
<td>0F 69</td>
<td>PUNPCKHWD mm, mm/m64</td>
<td>Interleave high-order words from mm and mm/m64 into mm.</td>
</tr>
<tr>
<td>0F 6A</td>
<td>PUNPCKHDQ mm, mm/m64</td>
<td>Interleave high-order doublewords from mm and mm/m64 into mm.</td>
</tr>
</tbody>
</table>

Description

Unpacks and interleaves the high-order data elements (bytes, words, or doublewords) of the destination operand (first operand) and source operand (second operand) into the destination operand (see Figure 2-22). The low-order data elements are ignored. The destination operand must be an MMX technology register; the source operand may be either an MMX technology register or a 64-bit memory location. When the source data comes from a memory operand, the full 64-bit operand is accessed from memory, but the instruction uses only the high-order 32 bits.

Figure 2-22. High-order Unpacking and Interleaving of Bytes with the PUNPCKHBW Instruction

The PUNPCKHBW instruction interleaves the four high-order bytes of the source operand and the four high-order bytes of the destination operand and writes them to the destination operand.

The PUNPCKHWD instruction interleaves the two high-order words of the source operand and the two high-order words of the destination operand and writes them to the destination operand.

The PUNPCKHDQ instruction interleaves the high-order doubleword of the source operand and the high-order doubleword of the destination operand and writes them to the destination operand.

If the source operand is all zeros, the result (stored in the destination operand) contains zero extensions of the high-order data elements from the original value in the destination operand. With the PUNPCKHBW instruction the high-order bytes are zero extended (that is, unpacked into unsigned words), and with the PUNPCKHWD instruction, the high-order words are zero extended (unpacked into unsigned doublewords).
Operation

IF instruction is PUNPCKHBW
THEN
  DEST(7..0) ← DEST(39..32);
  DEST(15..8) ← SRC(39..32);
  DEST(23..16) ← DEST(47..40);
  DEST(31..24) ← SRC(47..40);
  DEST(39..32) ← DEST(55..48);
  DEST(47..40) ← SRC(55..48);
  DEST(55..48) ← DEST(63..56);
  DEST(63..56) ← SRC(63..56);
ELSE IF instruction is PUNPCKHDW
THEN
  DEST(15..0) ← DEST(47..32);
  DEST(31..16) ← SRC(47..32);
  DEST(47..32) ← DEST(63..48);
  DEST(63..48) ← SRC(63..48);
ELSE (* instruction is PUNPCKHDQ *)
  DEST(31..0) ← DEST(63..32)
  DEST(63..32) ← SRC(63..32);
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults
- Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.

Itanium Mem Faults
- VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
PUNPCKHBW/PUNPCKHWD/PUNPCKHDQ—Unpack High Packed Data

(Continued)

Real-Address Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.

#UD If EM in CR0 is set.

#NM If TS in CR0 is set.

#MF If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP If any part of the operand lies outside of the effective address space from 0 to FFFFH.

#UD If EM in CR0 is set.

#NM If TS in CR0 is set.

#MF If there is a pending FPU exception.

#PF(fault-code) If a page fault occurs.

#AC(0) If alignment checking is enabled and an unaligned memory reference is made.
PUNPCKLBW/PUNPCKLWD/PUNPCKLDQ—Unpack Low Packed Data

### Description

Unpacks and interleaves the low-order data elements (bytes, words, or doublewords) of the destination and source operands into the destination operand (see Figure 2-23). The destination operand must be an MMX technology register; the source operand may be either an MMX technology register or a memory location. When source data comes from an MMX technology register, the upper 32 bits of the register are ignored. When the source data comes from a memory, only 32-bits are accessed from memory.

**Figure 2-23. Low-order Unpacking and Interleaving of Bytes with the PUNPCKLBW Instruction**

The PUNPCKLBW instruction interleaves the four low-order bytes of the source operand and the four low-order bytes of the destination operand and writes them to the destination operand.

The PUNPCKLWD instruction interleaves the two low-order words of the source operand and the two low-order words of the destination operand and writes them to the destination operand.

The PUNPCKLDQ instruction interleaves the low-order doubleword of the source operand and the low-order doubleword of the destination operand and writes them to the destination operand.

If the source operand is all zeros, the result (stored in the destination operand) contains zero extensions of the high-order data elements from the original value in the destination operand. With the PUNPCKLBW instruction the low-order bytes are zero extended (that is, unpacked into unsigned words), and with the PUNPCKLWD instruction, the low-order words are zero extended (unpacked into unsigned doublewords).
PUNPCKLBW/PUNPCKLWD/PUNPCKLDQ—Unpack Low Packed Data
(Continued)

Operation

IF instruction is PUNPCKLBW
THEN
  DEST(63..56) ← SRC(31..24);
  DEST(55..48) ← DEST(31..24);
  DEST(47..40) ← SRC(23..16);
  DEST(39..32) ← DEST(23..16);
  DEST(31..24) ← SRC(15..8);
  DEST(23..16) ← DEST(15..8);
  DEST(15..8) ← SRC(7..0);
  DEST(7..0) ← DEST(7..0);
ELSE IF instruction is PUNPCKLWD
THEN
  DEST(63..48) ← SRC(31..16);
  DEST(47..32) ← DEST(31..16);
  DEST(31..16) ← SRC(15..0);
  DEST(15..0) ← DEST(15..0);
ELSE (* instruction is PUNPCKLDQ *)
  DEST(63..32) ← SRC(31..0);
  DEST(31..0) ← DEST(31..0);
FI;

Flags Affected

None.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults          Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
Itanium Mem Faults          VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Protected Mode Exceptions

#GP(0) If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0) If a memory operand effective address is outside the SS segment limit.
#UD If EM in CR0 is set.
#NM If TS in CR0 is set.
#MF If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0) If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.
PUNPCKLBW/PUNPCKLWD/PUNPCKLDQ—Unpack Low Packed Data
(Continued)

Real-Address Mode Exceptions

#GP          If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD          If EM in CR0 is set.
#NM          If TS in CR0 is set.
#MF          If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP          If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD          If EM in CR0 is set.
#NM          If TS in CR0 is set.
#MF          If there is a pending FPU exception.
#PF(fault-code) If a page fault occurs.
#AC(0)       If alignment checking is enabled and an unaligned memory reference is made.
**PXOR—Logical Exclusive OR**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F EF /r</td>
<td>PXOR mm, mm/m64</td>
<td>XOR quadword from mm/m64 to quadword in mm.</td>
</tr>
</tbody>
</table>

**Description**

Performs a bitwise logical exclusive-OR (XOR) operation on the quadword source (second) and destination (first) operands and stores the result in the destination operand location (see Figure 2-24). The source operand can be an MMX technology register or a quadword memory location; the destination operand must be an MMX technology register. Each bit of the result is 1 if the corresponding bits of the two operands are different; each bit is 0 if the corresponding bits of the operands are the same.

**Figure 2-24. Operation of the PXOR Instruction**

![Figure 2-24](image)

**Operation**

DEST ← DEST XOR SRC;

**Flags Affected**

None.

**Additional Itanium® System Environment Exceptions**

- **Itanium Reg Faults**: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Abort.
- **Itanium Mem Faults**: VHPT Data Fault, Nested TLB Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
PXOR—Logical Exclusive OR (Continued)

Protected Mode Exceptions

#GP(0)  If a memory operand effective address is outside the CS, DS, ES, FS or GS segment limit.
#SS(0)  If a memory operand effective address is outside the SS segment limit.
#UD     If EM in CR0 is set.
#NM     If TS in CR0 is set.
#MF     If there is a pending FPU exception.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made while the current privilege level is 3.

Real-Address Mode Exceptions

#GP  If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD  If EM in CR0 is set.
#NM  If TS in CR0 is set.
#MF  If there is a pending FPU exception.

Virtual-8086 Mode Exceptions

#GP  If any part of the operand lies outside of the effective address space from 0 to FFFFH.
#UD  If EM in CR0 is set.
#NM  If TS in CR0 is set.
#MF  If there is a pending FPU exception.
#PF(fault-code)  If a page fault occurs.
#AC(0)  If alignment checking is enabled and an unaligned memory reference is made.
3.1 IA-32 Streaming SIMD Extension Instructions

This section lists the IA-32 Streaming SIMD Extension instructions designed to increase performance of IA-32 3D and floating-point intensive applications. For details on Streaming SIMD Extension please refer to the IA-32 Intel® Architecture Software Developer’s Manual.

3.2 About the Intel® Architecture Streaming SIMD Extensions

The Streaming SIMD Extensions for the Intel Architecture (IA) accelerates performance of 3D graphics applications over the current P6 generation of the Pentium Pro, Pentium II and Pentium III processors. The programming model is similar to the MMX technology model except that instructions now operate on new packed floating-point data types which contain four single-precision floating-point numbers.

The Streaming SIMD Extensions introduces new general purpose floating-point instructions, which operate on a new set of eight 128-bit Streaming SIMD Extension registers. This gives the programmer the ability to develop algorithms that can finely mix packed single-precision floating-point and integer using both Streaming SIMD Extension and MMX instructions respectively. In addition to these instructions, Streaming SIMD Extensions also provides new instructions to control cacheability of all MMX technology data types. These include ability to stream data into and from the processor while minimizing pollution of the caches and the ability to prefetch data before it is actually used. The main focus of packed floating-point instructions is the acceleration of 3D geometry. The new definition also contains additional SIMD Integer instructions to accelerate 3D rendering and video encoding and decoding. Together with the cacheability control instruction, this combination enables the development of new algorithms that can significantly accelerate 3D graphics.

The new Streaming SIMD Extension state requires OS support for saving and restoring the new state during a context switch. A new set of extended FSAVE/FRSTOR instructions will permit saving/restoring new and existing state for applications and OS. To make use of these new instructions, an application must verify that the processor supports Streaming SIMD Extensions extensions and the operating system supports this new extension. If both the extension and support is enabled, then the software application can use the new features.

The Streaming SIMD Extension instruction set is fully compatible with all software written for Intel architecture microprocessors. All existing software continues to run correctly, without modification, on microprocessors that incorporate the Streaming SIMD Extensions, as well as in the presence of existing and new applications that incorporate this technology.
3.3 Single Instruction Multiple Data

The Streaming SIMD Extensions uses the Single Instruction Multiple Data (SIMD) technique. This technique speeds up software performance by processing multiple data elements in parallel, using a single instruction. The Streaming SIMD Extensions supports operations on packed single-precision floating-point data types, and the additional SIMD Integer instructions support operations on packed quadrate data types (byte, word, or double-word). This approach was chosen because most 3D graphics and DSP applications have the following characteristics:

- Inherently parallel
- Wide dynamic range, hence floating-point based
- Regular and re-occurring memory access patterns
- Localized re-occurring operations performed on the data
- Data independent control flow

Streaming SIMD Extensions is 100% compatible with the IEEE Standard 754 for Binary Floating-point Arithmetic. The Streaming SIMD Extension instructions are accessible from all IA execution modes: Protected mode, Real address mode, and Virtual 8086 mode. New Features

Streaming SIMD Extensions provides the following new features, while maintaining backward compatibility with all existing Intel architecture microprocessors, IA applications and operating systems.

- New data type
- Eight Streaming SIMD Extension registers
- Enhanced instruction set

Streaming SIMD Extensions can enhance the performance of applications that use these features.

3.4 New Data Types

The principal data type of the Streaming SIMD Extensions is a packed single-precision floating-point operand, specifically:

- Four 32-bit single-precision (SP) floating-point numbers (Figure 3-1).

The SIMD Integer instructions will operate on the packed byte, word or doubleword data types. The prefetch instruction works on typeless data of size 32 bytes or greater.

Figure 3-1. Packed Single-FP Data Type

```
127  96  95  65  63   32  31   0

Packed Single-FP
```
3.5 Streaming SIMD Extension Registers

The Streaming SIMD Extensions provides eight 128-bit general purpose registers, each of which can be directly addressed. These registers are new state, and require support from the operating system to use them.

The Streaming SIMD Extension registers can hold packed 128-bit data. The Streaming SIMD Extension instructions access the Streaming SIMD Extension registers directly using the registers names XMM0 to XMM7 (Figure 3-2).

![Figure 3-2. Streaming SIMD Extension Register Set]

Streaming SIMD Extension registers can be used to perform calculation on data. They cannot be used to address memory; addressing is accomplished by using the integer registers and existing IA addressing modes.

The contents of Streaming SIMD Extension registers are cleared upon reset.

There is a new control/status register MXCSR which is used to mask/unmask numerical exception handling, to set rounding modes, to set flush-to-zero mode, and to view status flags.

3.6 Extended Instruction Set

The Streaming SIMD Extensions supplies a rich set of instructions that operate on either all or the least significant pairs of packed data operands, in parallel. The packed instructions operate on a pair of operands as shown in Figure 3-3 while scalar instructions always operate on the least significant pair of the two operands as shown in Figure 3-4; for scalar operations, the three upper components from the first operand are passed through to the destination. In general, the address of a memory operand has to be aligned on a 16-byte boundary for all instructions, except for unaligned loads and stores.
3.6.1 Instruction Group Review

3.6.1.1 Arithmetic Instructions

Packed/Scalar Addition and Subtraction
The ADDPS (Add packed single-precision floating-point) and SUBPS (Subtract packed single-precision floating-point) instructions add or subtract four pairs of packed single-precision floating-point operands.

The ADDSS (Add scalar single-precision floating-point) and SUBSS (Subtract scalar single-precision floating-point) instructions add or subtract the least significant pair of packed single-precision floating-point operands; the upper three fields are passed through from the source operand.

Packed/Scalar Multiplication and Division
The MULPS (Multiply packed single-precision floating-point) instruction multiplies four pairs of packed single-precision floating-point operands.
The MULSS (Multiply scalar single-precision floating-point) instruction multiplies the least significant pair of packed single-precision floating-point operands; the upper three fields are passed through from the source operand.

The DIVPS (Divide packed single-precision floating-point) instruction divides four pairs of packed single-precision floating-point operands.

The DIVSS (Divide scalar single-precision floating-point) instruction divides the least significant pair of packed single-precision floating-point operands; the upper three fields are passed through from the source operand.

**Packed/Scalar Square Root**

The SQRTPS (Square root packed single-precision floating-point) instruction returns the square root of the packed four single-precision floating-point numbers from the source to a destination register.

The SQRTSS (Square root scalar single-precision floating-point) instruction returns the square root of the least significant component of the packed single-precision floating-point numbers from source to a destination register; the upper three fields are passed through from the source operand.

**Packed Maximum/Minimum**

The MAXPS (Maximum packed single-precision floating-point) instruction returns the maximum of each pair of packed single-precision floating-point numbers into the destination register.

The MAXSS (Maximum scalar single-precision floating-point) instruction returns the maximum of the least significant pair of packed single-precision floating-point numbers into the destination register; the upper three fields are passed through from the source operand, to the destination register.

The MINPS (Minimum packed single-precision floating-point) instruction returns the minimum of each pair of packed single-precision floating-point numbers into the destination register.

The MINSS (Minimum scalar single-precision floating-point) instruction returns the minimum of the least significant pair of packed single-precision floating-point numbers into the destination register; the upper three fields are passed through from the source operand, to the destination register.

3.6.1.2 **Logical Instructions**

The ANDPS (Bit-wise packed logical AND for single-precision floating-point) instruction returns a bitwise AND between the two operands.

The ANDNPS (Bit-wise packed logical AND NOT for single-precision floating-point) instruction returns a bitwise AND NOT between the two operands.

The ORPS (Bit-wise packed logical OR for single-precision floating-point) instruction returns a bitwise OR between the two operands.

The XORPS (Bit-wise packed logical XOR for single-precision floating-point) instruction returns a bitwise XOR between the two operands.
### 3.6.1.3 Compare Instructions

The **CMPPS** (Compare packed single-precision floating-point) instruction compares four pairs of packed single-precision floating-point numbers using the immediate operand as a predicate, returning per SP field an all “1” 32-bit mask or an all “0” 32-bit mask as a result. The instruction supports a full set of 12 conditions: equal, less than, less than equal, greater than, greater than or equal, unordered, not equal, not less than, not less than or equal, not greater than, not greater than or equal, ordered.

The **CMPSS** (Compare scalar single-precision floating-point) instruction compares the least significant pairs of packed single-precision floating-point numbers using the immediate operand as a predicate (same as CMPPS), returning per SP field an all “1” 32-bit mask or an all “0” 32-bit mask as a result.

The **COMISS** (Compare scalar single-precision floating-point ordered and set EFLAGS) instruction compares the least significant pairs of packed single-precision floating-point numbers and sets the ZF,PF,CF bits in the EFLAGS register (the OF, SF and AF bits are cleared).

The **UCOMISS** (Unordered compare scalar single-precision floating-point ordered and set EFLAGS) instruction compares the least significant pairs of packed single-precision floating-point numbers and sets the ZF,PF,CF bits in the EFLAGS register as described above (the OF, SF and AF bits are cleared).

### 3.6.1.4 Shuffle Instructions

The **SHUFPS** (Shuffle packed single-precision floating-point) instruction is able to shuffle any of the packed four single-precision floating-point numbers from one source operand to the lower two destination fields; the upper two destination fields are generated from a shuffle of any of the four SP FP numbers from the second source operand (Figure 3-5). By using the same register for both sources, SHUFPS can return any combination of the four SP FP numbers from this register.

**Figure 3-5. Packed Shuffle Operation**

![Figure 3-5. Packed Shuffle Operation](image)

The **UNPCKHPS** (Unpacked high packed single-precision floating-point) instruction performs an interleaved unpack of the high-order data elements of first and second packed single-precision floating-point operands. It ignores the lower half part of the sources (Figure 3-6). When unpacking from a memory operand, the full 128-bit operand is accessed from memory but only the high order 64 bits are utilized by the instruction.
The UNPCKLPS (Unpacked low packed single-precision floating-point) instruction performs an interleaved unpack of the low-order data elements of first and second packed single-precision floating-point operands. It ignores the higher half part of the sources (Figure 3-7). When unpacking from a memory operand, the full 128-bit operand is accessed from memory but only the low order 64 bits are utilized by the instruction.

3.6.1.5 Conversion Instructions

These instructions support packed and scalar conversions between 128-bit Streaming SIMD Extension registers and either 64-bit integer MMX technology registers or 32-bit integer IA-32 registers. The packed versions behave identically to original MMX instructions, in the presence of x87-FP instructions, including:

- Transition from x87-FP to MMX technology (TOS=0, FP valid bits set to all valid).
- MMX instructions write ones (1’s) to the exponent part of the corresponding x87-FP register.
- Use of EMMS for transition from MMX technology to x87-FP.

The CVTP12PS (Convert packed 32-bit integer to packed single-precision floating-point) instruction converts two 32-bit signed integers in a MMX technology register to the two least significant single-precision floating-point numbers; when the conversion is inexact, the rounded value according to the rounding mode in MXCSR is returned. The upper two significant numbers in the destination register are retained.
The CVTSI2SS (Convert scalar 32-bit integer to scalar single-precision floating-point) instruction converts a 32-bit signed integer in a MMX technology register to the least significant single-precision floating-point number; when the conversion is inexact, the rounded value according to the rounding mode in MXCSR is returned. The upper three significant numbers in the destination register are retained.

The CVTPS2PI (Convert packed single-precision floating-point to packed 32-bit integer) instruction converts the two least significant single-precision floating-point numbers to two 32-bit signed integers in a MMX technology register; when the conversion is inexact, the rounded value according to the rounding mode in MXCSR is returned. The CVTTPS2PI (Convert truncate packed single-precision floating-point to packed 32-bit integer) instruction is similar to CVTPS2PI except if the conversion is inexact, in which case the truncated result is returned.

The CVTSS2SI (Convert scalar single-precision floating-point to a 32-bit integer) instruction converts the least significant single-precision floating-point number to a 32-bit signed integer in an Intel architecture 32-bit integer register; when the conversion is inexact, the rounded value according to the rounding mode in MXCSR is returned. The CVTTSS2SI (Convert truncate scalar single-precision floating-point to scalar 32-bit integer) instruction is similar to CVTSS2SI except if the conversion is inexact, the truncated result is returned.

### 3.6.1.6 Data Movement Instructions

The MOVAPS (Move aligned packed single-precision floating-point) instruction transfers 128-bits of packed data from memory to Streaming SIMD Extension registers and vice versa, or between Streaming SIMD Extension registers. The memory address is aligned to 16-byte boundary; if not then a general protection exception will occur.

The MOVUPS (Move unaligned packed single-precision floating-point) instruction transfers 128-bits of packed data from memory to Streaming SIMD Extension registers and vice versa, or between Streaming SIMD Extension registers. No assumption is made for alignment.

The MOVHPS (Move aligned high packed single-precision floating-point) instruction transfers 64-bits of packed data from memory to the upper two fields of a Streaming SIMD Extension register and vice versa. The lower field is left unchanged.

The MOVLPS (Move aligned low packed single-precision floating-point) instruction transfers 64-bits of packed data from memory to the lower two fields of a Streaming SIMD Extension register and vice versa. The upper field is left unchanged.

The MOVMSKPS (Move mask packed single-precision floating-point) instruction transfers the most significant bit of each of the four packed single-precision floating-point number to an IA integer register. This 4-bit value can then be used as a condition to perform branching.

The MOVSS (Move scalar single-precision floating-point) instruction transfers a single 32-bit floating-point number from memory to a Streaming SIMD Extension register or vice versa, and between registers.
3.6.1.7 State Management Instructions

The LDMXCSR (Load Streaming SIMD Extension Control and Status Register) instruction loads the Streaming SIMD Extension control and status register from memory. STMXCSR (Store Streaming SIMD Extension Control and Status Register) instruction stores the Streaming SIMD Extension control and status word to memory.

The FXSAVE instruction saves FP and MMX technology state and Streaming SIMD Extension state to memory. Unlike FSAVE, FXSAVE does not clear the x87-FP state. FXRSTOR loads FP and MMX technology state and Streaming SIMD Extension state from memory.

3.6.1.8 Additional SIMD Integer Instructions

Similar to the conversions instructions discussed in Section 3.6.1.5, these SIMD Integer instructions also behave identically to original MMX instructions, in the presence of x87-FP instructions.

The PAVGB/PAVGW (Average unsigned source sub-operands, without incurring a loss in precision) instructions add the unsigned data elements of the source operand to the unsigned data elements of the destination register. The results of the add are then each independently right shifted right by one bit position. The high order bits of each element are filled with the carry bits of the sums. To prevent cumulative round-off errors, an averaging is performed. The low order bit of each final shifted result is set to 1 if at least one of the two least significant bits of the intermediate unshifted shifted sum is 1.

The PEXTRW (Extract 16-bit word from MMX technology register) instruction moves the word in a MMX technology register selected by the two least significant bits of the immediate operand to the lower half of a 32-bit integer register; the upper word in the integer register is cleared.

The PINSRW (Insert 16-bit word into MMX technology register) instruction moves the lower word in a 32-bit integer register or 16-bit word from memory into one of the four word locations in a MMX technology register, selected by the two least significant bits of the immediate operand.

The PMAXUB/PMAXSW (Maximum of packed unsigned integer bytes or signed integer words) instruction returns the maximum of each pair of packed elements into the destination register.

The PMINUB/PMINSW (Minimum of packed unsigned integer bytes or signed integer words) instructions returns the minimum of each pair of packed data elements into the destination register.

The PMOVMSKB (Move Byte Mask from MMX technology register) instruction returns an 8-bit mask formed of the most significant bits of each byte of its source operand in a MMX technology register to an IA integer register.

The PMULHUW (Unsigned high packed integer word multiply in MMX technology register) instruction performs an unsigned multiply on each word field of the two source MMX technology registers, returning the high word of each result to a MMX technology register.

The PSADBW (Sum of absolute differences) instruction computes the absolute difference for each pair of sub-operand byte sources and then accumulates the 8 differences into a single 16-bit result.

The PSHUFW (Shuffle packed integer word in MMX technology register) instruction performs a full shuffle of any source word field to any result word field, using an 8-bit immediate operand.
3.6.1.9 Cacheability Control Instructions

Data referenced by a programmer can have temporal (data will be used again) or spatial (data will be in adjacent locations, e.g. same cache line) locality. Some multimedia data types, such as the display list in a 3D graphics application, are referenced once and not reused in the immediate future. We will refer to this data type as non-temporal data. Thus the programmer does not want the application’s cached code and data to be overwritten by this non-temporal data. The cacheability control instructions enable the programmer to control caching so that non-temporal accesses will minimize cache pollution.

In addition, the execution engine needs to be fed such that it does not become stalled waiting for data. Streaming SIMD Extension instructions allow the programmer to prefetch data long before it’s final use. These instructions are not architectural since they do not update any architectural state, and are specific to each implementation. The programmer may have to tune his application for each implementation to take advantage of these instructions. These instructions merely provide a hint to the hardware, and they will not generate exceptions or faults. Excessive use of prefetch instructions may be throttled by the processor.

The following four instructions provide hints to the cache hierarchy which enables the data to be prefetched to different levels of the cache hierarchy and avoid polluting cache with non-temporal data.

The MASKMOVQ (Non-temporal byte mask store of packed integer in a MMX technology register) instruction stores data from a MMX technology register to the location specified by the EDI register. The most significant bit in each byte of the second MMX technology mask register is used to selectively write the data of the first register on a per-byte basis. The instruction is implicitly weakly-ordered, with all of the characteristics of the WC memory type; successive non-temporal stores may not write memory in program-order, do not write-allocate (i.e. the processor will not fetch the corresponding cache line into the cache hierarchy, prior to performing the store), write combine/collapse, and minimize cache pollution.

The MOVNTQ (Non-temporal store of packed integer in a MMX technology register) instruction stores data from a MMX technology register to memory. The instruction is implicitly weakly-ordered, does not write-allocate and minimizes cache pollution.

The MOVNTPS (Non-temporal store of packed single-precision floating-point) instruction stores data from a Streaming SIMD Extension register to memory. The memory address must be aligned to a 16-byte boundary; if it is not aligned, a general protection exception will occur. The instruction is implicitly weakly-ordered, does not write-allocate and minimizes cache pollution.

The main difference between a non-temporal store and a regular cacheable store is in the write-allocation policy. The memory type of the region being written to can override the non-temporal hint, leading to the following considerations:

- If the programmer specifies a non-temporal store to uncacheable memory, then the store behaves like an uncacheable store; the non-temporal hint is ignored and the memory type for the region is retained. Uncacheable as referred to here means that the region being written to has been mapped with either a UC or WP memory type. If the memory region has been mapped as WB, WT or WC, the non-temporal store will implement weakly-ordered (WC) semantic behavior.
• If the programmer specifies a non-temporal store to cacheable memory, two cases may result:
  • If the data is present in the cache hierarchy, the instruction will ensure consistency. A given processor may choose different ways to implement this; some examples include: updating data in-place in the cache hierarchy while preserving the memory type semantics assigned to that region, or evicting the data from the caches and writing the new non-temporal data to memory (with WC semantics).
  • If the data is not present in the cache hierarchy, and the destination region is mapped as WB, WT or WC, the transaction will be weakly ordered, and is subject to all WC memory semantics. The non-temporal store will not write allocate. Different implementations may choose to collapse and combine these stores.
• In general, WC semantics require software to ensure coherence, with respect to other processors and other system agents (such as graphics cards). Appropriate use of synchronization and a fencing operation (see SFENCE, below) must be performed for producer-consumer usage models. Fencing ensures that all system agents have global visibility of the stored data; for instance, failure to fence may result in a written cache line staying within a processor, and the line would not be visible to other agents. For processors which implement non-temporal stores by updating data in-place that already resides in the cache hierarchy, the destination region should also be mapped as WC. Otherwise if mapped as WB or WT, there is the potential for speculative processor reads to bring the data into the caches; in this case, non-temporal stores would then update in place, and data would not be flushed from the processor by a subsequent fencing operation.
• The memory type visible on the bus in the presence of memory type aliasing is implementation specific. As one possible example, the memory type written to the bus may reflect the memory type for the first store to this line, as seen in program order; other alternatives are possible. This behavior should be considered reserved, and dependency on the behavior of any particular implementation risks future incompatibility.

The PREFETCH (Load 32 or greater number of bytes) instructions load either non-temporal data or temporal data in the specified cache level. This access and the cache level are specified as a hint. The prefetch instructions do not affect functional behavior of the program and will be implementation specific.

The SFENCE (Store Fence) instruction guarantees that every store instruction that precedes the store fence instruction in program order is globally visible before any store instruction which follows the fence. The SFENCE instruction provides an efficient way of ensuring ordering between routines that produce weakly-ordered results and routines that consume this data.

### IEEE Compliance

A Streaming SIMD Extension floating-point computation is IEEE-754 compliant except when the control word is set to flush to zero mode. IEEE-754 compliance includes support for single-precision signed infinities, QNaNs, SNaNs, integer indefinite, signed zeros, denormals, masked and unmasked exceptions. Single-precision floating-point values are represented identically both internally and in memory, and are of the following form:

<table>
<thead>
<tr>
<th>Sign</th>
<th>Exponent</th>
<th>Significand</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30...23</td>
<td>22...0</td>
</tr>
</tbody>
</table>
This is a change from x87 floating-point which internally represents all numbers in 80-bit extended format. This change implies that x87-FP libraries re-written to use Streaming SIMD Extension instructions may not produce results that are identical to those of the x87-FP implementation.

Real Numbers and Floating-point Formats.

This section describes how real numbers are represented in floating-point format in the processor. It also introduces terms such as normalized numbers, denormalized numbers, biased exponents, signed zeros, and NaNs. Readers who are already familiar with floating-point processing techniques and the IEEE standards may wish to skip this section.

3.7.1 Real Number System

As shown in Figure 3-8, the real-number system comprises the continuum of real numbers from minus infinity (−∞) to plus infinity (+∞).

Figure 3-8. Binary Real Number System

Because the size and number of registers that any computer can have is limited, only a subset of the real-number continuum can be used in real-number calculations. As shown at the bottom of Figure 3-1, the subset of real numbers that a particular processor supports represents an approximation of the real number system. The range and precision of this real-number subset is determined by the format that the processor uses to represent real numbers.
3.7.1.1 Floating-point Format

To increase the speed and efficiency of real-number computations, computers typically represent real numbers in a binary floating-point format. In this format, a real number has three parts: a sign, a significand, and an exponent. Figure 3-9 shows the binary floating-point format that Streaming SIMD Extension data uses. This format conforms to the IEEE standard.

**Figure 3-9. Binary Floating-point Format**

The sign is a binary value that indicates whether the number is positive (0) or negative (1). The significand has two parts: a 1-bit binary integer (also referred to as the J-bit) and a binary fraction. The J-bit is often not represented, but instead is an implied value. The exponent is a binary integer that represents the base-2 power that the significand is raised to.

Table 3-1 shows how the real number 178.125 (in ordinary decimal format) is stored in floating-point format. The table lists a progression of real number notations that leads to the format that the processor uses. In this format, the binary real number is normalized and the exponent is biased.

**Table 3-1. Real Number Notation**

<table>
<thead>
<tr>
<th>Notation</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ordinary Decimal</td>
<td>178.125</td>
</tr>
<tr>
<td>Scientific Decimal</td>
<td>1.78125E102</td>
</tr>
<tr>
<td>Scientific Binary (Biased Exponent)</td>
<td>1.0110010001EZ111</td>
</tr>
<tr>
<td>Scientific Binary (Biased Exponent)</td>
<td>1.0110010001Z10000110</td>
</tr>
<tr>
<td>Single Format (Normalized)</td>
<td></td>
</tr>
<tr>
<td>Sign</td>
<td>Biased Exponent</td>
</tr>
<tr>
<td>0</td>
<td>10000110</td>
</tr>
<tr>
<td>1 (Implied)</td>
<td>011001000100000000000000</td>
</tr>
</tbody>
</table>

3.7.1.2 Normalized Numbers

In most cases, the processor represents real numbers in normalized form. This means that except for zero, the significand is always made up of an integer of 1 and the following fraction:

1.fff...ff

For values less than 1, leading zeros are eliminated. (For each leading zero eliminated, the exponent is decremented by one.)
Representing numbers in normalized form maximizes the number of significant digits that can be accommodated in a significand of a given width. To summarize, a normalized real number consists of a normalized significand that represents a real number between 1 and 2 and an exponent that specifies the number’s binary point.

### 3.7.1.3 Biased Exponent

The processor represents exponents in a biased form. This means that a constant is added to the actual exponent so that the biased exponent is always a positive number. The value of the biasing constant depends on the number of bits available for representing exponents in the floating-point format being used. The biasing constant is chosen so that the smallest normalized number can be reciprocated without overflow.

### 3.7.1.4 Real Number and Non-Number Encodings

A variety of real numbers and special values can be encoded in the processor’s floating-point format. These numbers and values are generally divided into the following classes:

- Signed zeros
- Denormalized finite numbers
- Normalized finite numbers
- Signed infinities
- NaNs
- Indefinite numbers

(The term NaN stands for “Not a Number.”)

Figure 3-10 shows how the encodings for these numbers and non-numbers fit into the real number continuum. The encodings shown here are for the IEEE single-precision (32-bit) format, where the term “S” indicates the sign bit, “E” the biased exponent, and “F” the fraction. (The exponent values are given in decimal.)

The processor can operate on and/or return any of these values, depending on the type of computation being performed. The following sections describe these number and non-number classes.

### 3.7.1.5 Signed Zeros

Zero can be represented as a +0 or a −0 depending on the sign bit. Both encodings are equal in value. The sign of a zero result depends on the operation being performed and the rounding mode being used. Signed zeros have been provided to aid in implementing interval arithmetic. The sign of a zero may indicate the direction from which underflow occurred, or it may indicate the sign of an ∞ that has been reciprocated.
3.7.1.6 Normalized and Denormalized Finite Numbers

Non-zero, finite numbers are divided into two classes: normalized and denormalized. The normalized finite numbers comprise all the non-zero finite values that can be encoded in a normalized real number format between zero and $\infty$. In the format shown in Figure 3-10, this group of numbers includes all the numbers with biased exponents ranging from 1 to 254\(_{10}\) (unbiased, the exponent range is from \(-126\) to \(+127\)\(_{10}\)).

**Figure 3-10. Real Numbers and NaNs**

<table>
<thead>
<tr>
<th>S</th>
<th>E</th>
<th>F</th>
</tr>
</thead>
</table>
| 1 | 0 | 0 | -0
| 1 | 0 | 0.XXX\(2\) | Denormalized Finite
| 1 | ...254 | Any Value | Normalized Finite
| 1 | 255 | 0 | -\(\infty\)
| X\(1\) | 255 | 1.XXX\(2\) | SNaN
| X\(1\) | 255 | 1.1XX | QNaN

When real numbers become very close to zero, the normalized-number format can no longer be used to represent the numbers. This is because the range of the exponent is not large enough to compensate for shifting the binary point to the right to eliminate leading zeros.

When the biased exponent is zero, smaller numbers can only be represented by making the integer bit (and perhaps other leading bits) of the significand zero. The numbers in this range are called denormalized (or tiny) numbers. The use of leading zeros with denormalized numbers allows smaller numbers to be represented. However, this denormalization causes a loss of precision (the number of significant bits in the fraction is reduced by the leading zeros).

When performing normalized floating-point computations, a processor normally operates on normalized numbers and produces normalized numbers as results. Denormalized numbers represent an underflow condition.

A denormalized number is computed through a technique called gradual underflow. Table 3-2 gives an example of gradual underflow in the denormalization process. Here the single-real format is being used, so the minimum exponent (unbiased) is \(-126\)\(_{10}\). The true result in this example requires an exponent of \(-129\)\(_{10}\) in order to have a normalized number. Since \(-129\)\(_{10}\) is beyond the allowable exponent range, the result is denormalized by inserting leading zeros until the minimum exponent of \(-126\)\(_{10}\) is reached.
In the extreme case, all the significant bits are shifted out to the right by leading zeros, creating a zero result.

The processor deals with denormal values in the following ways:
- It avoids creating denormals by normalizing numbers whenever possible.
- It provides the floating-point underflow exception to permit programmers to detect cases when denormals are created.
- It provides the floating-point denormal-operand exception to permit procedures or programs to detect when denormals are being used as source operands for computations.

### 3.7.1.7 Signed Infinities

The two infinities, $+\infty$ and $-\infty$, represent the maximum positive and negative real numbers, respectively, that can be represented in the floating-point format. Infinity is always represented by a zero significand (fraction and integer bit) and the maximum biased exponent allowed in the specified format (for example, 255 for the single-real format).

The signs of infinities are observed, and comparisons are possible. Infinities are always interpreted in the affine sense; that is, $-\infty$ is less than any finite number and $+\infty$ is greater than any finite number. Arithmetic on infinities is always exact. Exceptions are generated only when the use of an infinity as a source operand constitutes an invalid operation.

Whereas denormalized numbers represent an underflow condition, the two infinity numbers represent the result of an overflow condition. Here, the normalized result of a computation has a biased exponent greater than the largest allowable exponent for the selected result format.

### 3.7.1.8 NaNs

Since NaNs are non-numbers, they are not part of the real number line. In Figure 3-10, the encoding space for NaNs in the processor floating-point formats is shown above the ends of the real number line. This space includes any value with the maximum allowable biased exponent and a non-zero fraction. (The sign bit is ignored for NaNs.)

The IEEE standard defines two classes of NaN: quiet NaNs (QNaNs) and signaling NaNs (SNaNs). A QNaN is a NaN with the most significant fraction bit set; an SNaN is a NaN with the most significant fraction bit clear. QNaNs are allowed to propagate through most arithmetic operations without signaling an exception. SNaNs generally signal an invalid-operation exception whenever they appear as operands in arithmetic operations. Exceptions, as well as detailed information on how the processor handles NaNs, are discussed in Section 3.7.2.
3.7.1.9 Indefinite

In response to a masked invalid-operation floating-point exceptions, the indefinite value QNAN is produced. The integer indefinite, which can be produced during conversion from single-precision floating-point to 32-bit integer, is defined to be 80000000H.

3.7.2 Operating on NaNs

As was described in Section 3.7.1.8, Streaming SIMD Extension supports two types of NaNs: SNaNs and QNaNs. An SNaN is any NaN value with its most-significant fraction bit set to 0 and at least one other fraction bit set to 1. (If all the fraction bits are set to 0, the value is an \(\infty\).) A QNaN is any NaN value with the most-significant fraction bit set to 1. The sign bit of a NaN is not interpreted.

As a general rule, when a QNaN is used in one or more arithmetic floating-point instructions, it is allowed to propagate through a computation. An SNaN on the other hand causes a floating-point invalid-operation exception to be signaled. SNaNs are typically used to trap or invoke an exception handler.

The invalid operation exception has a flag and a mask bit associated with it in MXCSR. The mask bit determines how the an SNaN value is handled. If the invalid operation mask bit is set, the SNaN is converted to a QNaN by setting the most-significant fraction bit of the value to 1. The result is then stored in the destination operand and the invalid operation flag is set. If the invalid operation mask is clear, an invalid operation fault is signaled and no result is stored in the destination operand.

When a real operation or exception delivers a QNaN result, the value of the result depends on the source operands, as shown in Table 3-3. The exceptions to the behavior described in Table 3-3 are the MINPS and MAXPS instructions. If only one source is a NaN for these instructions, the Src2 operand (either NaN or real value) is written to the result; this differs from the behavior for other instructions as defined in Table 3-3, which is to always write the NaN to the result, regardless of which source operand contains the NaN. This approach for MINPS/MAXPS allows NaN data to be screened out of the bounds-checking portion of an algorithm. If instead of this behavior, it is required that the NaN source operand be returned, the min/max functionality can be emulated using a sequence of instructions: comparison followed by AND, ANDN and OR.

In general Src1 and Src2 relate to a Streaming SIMD Extension instruction as follows:

\[
\text{ADDPS Src1, Src2/m128}
\]

Except for the rules given at the beginning of this section for encoding SNaNs and QNaNs, software is free to use the bits in the significand of a NaN for any purpose. Both SNaNs and QNaNs can be encoded to carry and store data, such as diagnostic information.
3.8 Data Formats

3.8.1 Memory Data Formats

The Intel architecture Streaming SIMD Extension introduces a new packed 128-bit data type which consists of 4 single-precision floating-point numbers. The 128 bits are numbered 0 through 127. Bit 0 is the least significant bit (LSB), and bit 127 is the most significant bit (MSB).

Bytes in the new data type format have consecutive memory addresses. The ordering is always little endian, that is, the bytes with the lower addresses are less significant than the bytes with the higher addresses.

3.8.2 Streaming SIMD Extension Register Data Formats

Values in Streaming SIMD Extension registers have the same format as a 128-bit quantity in memory. They have two data access modes: 128-bit access mode and 32-bit access mode. The data type corresponds directly to the single-precision format in the IEEE standard. Table 3-4 gives the precision and range of this data type. Only the fraction part of the significand is encoded. The integer is assumed to be 1 for all numbers except 0 and denormalized finite numbers. The exponent of the single-precision data type is encoded in biased format. The biasing constant is 127 for the single-precision format.

Table 3-3. Results of Operations with NAN Operands

<table>
<thead>
<tr>
<th>Source Operands</th>
<th>NaN Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>An SNaN and a QNaN.</td>
<td>Src1 NaN (converted to QNaN if Src1 is an SNaN).</td>
</tr>
<tr>
<td>Two SNaNs.</td>
<td>Src1 NaN (converted to QNaN).</td>
</tr>
<tr>
<td>Two QNaNs.</td>
<td>Src1 QNaN</td>
</tr>
<tr>
<td>An SNaN and a real value.</td>
<td>The SNaN converted into a QNaN.</td>
</tr>
<tr>
<td>A QNaN and a real value.</td>
<td>The QNaN source operand.</td>
</tr>
<tr>
<td>An SNaN/QNaN value (for instructions which take only one operand i.e. RCPFS, RCPSS, RSQRTPS, RSQRTSS)</td>
<td>The SNaN converted into a QNaN/the source QNaN.</td>
</tr>
<tr>
<td>Neither source operand is a NaN and a floating-point invalid-operation exception is signaled.</td>
<td>The default QNaN real indefinite.</td>
</tr>
</tbody>
</table>

Figure 3-11. Four Packed FP Data in Memory (at address 1000H)
Table 3-4. Precision and Range of Streaming SIMD Extension Datatype

<table>
<thead>
<tr>
<th>Data Type</th>
<th>Length</th>
<th>Precision (Bits)</th>
<th>Approximate Normalized Range</th>
<th>Binary</th>
<th>Decimal</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-precision</td>
<td>32</td>
<td>24</td>
<td>$2^{-128}$ to $2^{127}$</td>
<td>$1.18 \times 10^{-38}$ to $3.40 \times 10^{38}$</td>
<td></td>
</tr>
</tbody>
</table>

Table 3-5 shows the encodings for all the classes of real numbers (that is, zero, denormalized-finite, normalized-finite, and $\infty$) and NaNs for the single-real data-type. It also gives the format for the real indefinite value, which is a QNaN encoding that is generated by several Streaming SIMD Extension instructions in response to a masked floating-point invalid-operation exception.

Table 3-5. Real Number and NaN Encodings

<table>
<thead>
<tr>
<th>Class</th>
<th>Sign</th>
<th>Biased Exponent</th>
<th>Significand</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>Integer $^1$</td>
</tr>
<tr>
<td>Positive</td>
<td>$+\infty$</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$+\text{Normals}$</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>$+\text{Denormals}$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$+\text{Zero}$</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Negative</td>
<td>$-\text{Zero}$</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$-\text{Denormals}$</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$-\text{Normals}$</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>$-\infty$</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>NaNs</td>
<td>SNaN</td>
<td>$X$</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>QNaN</td>
<td>$X$</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Real Indefinite (QNaN)</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

When storing real values in memory, single-real values are stored in 4 consecutive bytes in memory. The 128-bit access mode is used for 128-bit memory accesses, 128-bit transfers between Streaming SIMD Extension registers, and all logical, unpack and arithmetic instructions. The 32-bit access mode is used for 32-bit memory access, 32-bit transfers between Streaming SIMD Extension registers, and all arithmetic instructions.

There are sixty-eight new instructions in a Streaming SIMD Extension instruction set. This chapter describes the packed and scalar floating-point instructions in alphabetical order, with a full description of each instruction. The last two sections of this chapter describe the SIMD Integer instructions and the cacheability control instructions.
3.9 Instruction Formats

The nature of Streaming SIMD Extension allows the use of existing instruction formats. Instructions use the ModR/M format and are preceded by the 0F prefix byte. In general, operations are not duplicated to provide two directions (i.e. separate load and store variants).

3.10 Instruction Prefixes

The Streaming SIMD Extension instruction uses prefixes as specified in Table 3-6, Table 3-7, and Table 3-8. The effect of multiple prefixes (more than one prefix from a group) is unpredictable and may vary from processor to processor.

Applying a prefix, in a manner not defined in this document, is considered reserved behavior. For example, Table 3-6 shows general behavior for most Streaming SIMD Extension instructions; however, the application of a prefix (Repeat, Repeat NE, Operand Size) is reserved for the following instructions:

ANDPS, ANDNPS, COMISS, FXRSTOR, FXSAVE, ORPS, LDMXCSR, MOVAPS, MOVHPS, MOVLPS, MOVMSKPS, MOVNTPS, MOVUPS, SHUFPS, STMXCSR, UCOMISS, UNPCKHPS, UNPCKLPS, XORPS.

Table 3-6. Streaming SIMD Extension Instruction Behavior with Prefixes

<table>
<thead>
<tr>
<th>Prefix Type</th>
<th>Effect on Streaming SIMD Extension Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Size Prefix (67H)</td>
<td>Affects Streaming SIMD Extension instructions with memory operand Ignored by Streaming SIMD Extension instructions without memory operand.</td>
</tr>
<tr>
<td>Operand Size (66H)</td>
<td>Reserved and may result in unpredictable behavior.</td>
</tr>
<tr>
<td>Segment Override</td>
<td>Affects Streaming SIMD Extension instructions with mem. operand Ignored by Streaming SIMD Extension instructions without mem operand</td>
</tr>
<tr>
<td>Repeat Prefix (F3H)</td>
<td>Affects Streaming SIMD Extension instructions</td>
</tr>
<tr>
<td>Repeat NE Prefix (F2H)</td>
<td>Reserved and may result in unpredictable behavior.</td>
</tr>
<tr>
<td>Lock Prefix (0F0H)</td>
<td>Generates invalid opcode exception.</td>
</tr>
</tbody>
</table>

Table 3-7. SIMD Integer Instructions – Behavior with Prefixes

<table>
<thead>
<tr>
<th>Prefix Type</th>
<th>Effect on Intel® MMX™ Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Size Prefix (67H)</td>
<td>Affects Intel® MMX™ instructions with mem. operand Ignored by Intel® MMX™ instructions without mem. operand.</td>
</tr>
<tr>
<td>Operand Size (66H)</td>
<td>Reserved and may result in unpredictable behavior.</td>
</tr>
<tr>
<td>Segment Override</td>
<td>Affects Intel® MMX™ instructions with mem. operand Ignored by Intel® MMX™ instructions without mem operand</td>
</tr>
<tr>
<td>Repeat Prefix (F3H)</td>
<td>Reserved and may result in unpredictable behavior.</td>
</tr>
<tr>
<td>Repeat NE Prefix (F2H)</td>
<td>Reserved and may result in unpredictable behavior.</td>
</tr>
<tr>
<td>Lock Prefix (0F0H)</td>
<td>Generates invalid opcode exception.</td>
</tr>
</tbody>
</table>
### 3.11 Reserved Behavior and Software Compatibility

In many register and memory layout descriptions, certain bits are marked as *reserved*. When bits are marked as reserved, it is essential for compatibility with future processors that software treat these bits as having a future, though unknown, effect. The behavior of reserved bits should be regarded as not only reserved, but unpredictable. In general, reserved behavior may also be applied in other areas. Software should follow these guidelines in dealing with reserved behavior:

- Do not depend on the states of any reserved fields when testing the values of registers which contain such bits. Mask out the reserved fields before testing.
- Do not depend on the states of any reserved fields when storing to memory or to a register.
- Do not depend on the ability to retain information written into any reserved fields.
- When loading a register, always load the reserved fields with the values indicated in the documentation, if any, or reload them with values previously read from the same register.

**Note:** Avoid any software dependency upon the reserved state/behavior. Depending upon reserved behavior will make the software dependent upon the unspecified manner in which the processor handles this behavior and risks incompatibility with future processors.

### 3.12 Notations

Besides opcodes, two kinds of notations are found which both describe information found in the ModR/M byte:

1. `/digit:` (digit between 0 and 7) indicates that the instruction uses only the r/m (register and memory) operand. The reg field contains the digit that provides an extension to the instruction's opcode.
2. `/r:` indicates that the ModR/M byte of an instruction contains both a register operand and an r/m operand.

In addition, the following abbreviations are used:

- `r32:` Intel architecture 32-bit integer register.
- `xmm/m128:` Indicates a 128-bit multimedia register or a 128-bit memory location.
- `xmm/m64:` Indicates a 128-bit multimedia register or a 64-bit memory location.

---

**Table 3-8. Cacheability Control Instruction Behavior with Prefixes**

<table>
<thead>
<tr>
<th>Prefix Type</th>
<th>Effect on Streaming SIMD Extension Instructions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address Size Prefix (67H)</td>
<td>Affects cacheability control instruction with a mem. operand</td>
</tr>
<tr>
<td>Operand Size (66H)</td>
<td>Ignored by cacheability control instruction w/o a mem. operand.</td>
</tr>
<tr>
<td>Segment Override (2EH,36H,3EH,26H,64H,65H)</td>
<td>Reserved and may result in unpredictable behavior.</td>
</tr>
<tr>
<td>Repeat Prefix(F3H)</td>
<td>Affects cacheability control instructions with mem. operand</td>
</tr>
<tr>
<td>Repeat NE Prefix(F2H)</td>
<td>Ignored by cacheability control instruction without mem operand</td>
</tr>
<tr>
<td>Lock Prefix (0F0H)</td>
<td>Reserved and may result in unpredictable behavior.</td>
</tr>
<tr>
<td></td>
<td>Generates an invalid opcode exception for all cacheability instructions.</td>
</tr>
</tbody>
</table>
• **xmm/m32**: Indicates a 128-bit multimedia register or a 32-bit memory location.

• **mm/m64**: Indicates a 64-bit multimedia register or a 64-bit memory location.

• **imm8**: Indicates an immediate 8-bit operand.

• **ib**: Indicates that an immediate byte operand follows the opcode, ModR/M byte or scaled-indexing byte.

When there is ambiguity, xmm1 indicates the first source operand and xmm2 the second source operand.

Table 3-9 describes the naming conventions used in the Streaming SIMD Extension instruction mnemonics.

**Table 3-9. Key to Streaming SIMD Extension Naming Convention**

<table>
<thead>
<tr>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PI</td>
<td>Packed integer qword (e.g. mm0)</td>
</tr>
<tr>
<td>PS</td>
<td>Packed single FP (e.g. xmm0)</td>
</tr>
<tr>
<td>SI</td>
<td>Scalar integer (e.g. eax)</td>
</tr>
<tr>
<td>SS</td>
<td>Scalar single-FP (e.g. low 32 bits of xmm0)</td>
</tr>
</tbody>
</table>
ADDPS: Packed Single-FP Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,58,/r</td>
<td>ADDPS xmm1, xmm2/m128</td>
<td>Add packed SP FP numbers from XMM2/Mem to XMM1.</td>
</tr>
</tbody>
</table>

Operation:

- \( \text{xmm1}[31-0] = \text{xmm1}[31-0] + \text{xmm2/m128}[31-0]; \)
- \( \text{xmm1}[63-32] = \text{xmm1}[63-32] + \text{xmm2/m128}[63-32]; \)
- \( \text{xmm1}[95-64] = \text{xmm1}[95-64] + \text{xmm2/m128}[95-64]; \)
- \( \text{xmm1}[127-96] = \text{xmm1}[127-96] + \text{xmm2/m128}[127-96]; \)

Description: The ADDPS instruction adds the packed SP FP numbers of both their operands.

Exceptions: General protection exception if not aligned on 16-byte boundary, regardless of segment.

Numeric Exceptions: Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; 
- #NM if TS bit in CR0 is set. #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0);
- #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0).

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
ADDSS: Scalar Single-FP Add

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3.0F.58. /r</td>
<td>ADDSS xmm1, xmm2/m32</td>
<td>Add the lower SP FP number from XMM2/Mem to XMM1.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\begin{align*}
\text{xmm1}[31-0] &= \text{xmm1}[31-0] + \text{xmm2/m32}[31-0]; \\
\text{xmm1}[63-32] &= \text{xmm1}[63-32]; \\
\text{xmm1}[95-64] &= \text{xmm1}[95-64]; \\
\text{xmm1}[127-96] &= \text{xmm1}[127-96];
\end{align*}
\]

**Description:** The ADDSS instruction adds the lower SP FP numbers of both their operands; the upper 3 fields are passed through from xmm1.

**FP Exceptions:** None.

**Numeric Exceptions:** Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3);
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0);
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0);
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

- Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
ANDNPS: Bit-wise Logical And Not for Single-FP

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,55,/r</td>
<td>ANDNPS xmm1, xmm2/m128</td>
<td>Invert the 128 bits in XMM1 and then AND the result with 128 bits from XMM2/Mem.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\text{xmm1}[127-0] = \neg (\text{xmm1}[127-0]) \& \text{xmm2/m128}[127-0];
\]

**Description:**
The ANDNPS instructions returns a bit-wise logical AND between the complement of XMM1 and XMM2/Mem.

**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** None

**Protected Mode Exceptions:**
- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**
- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set.

**Virtual 8086 Mode Exceptions:**
- Same exceptions as in Real Address Mode;
- #PF(fault-code) for a page fault;
- #UD if CR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Additional Itanium® System Environment Exceptions**
- Itanium Reg Faults
- Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults
- VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

**Comments:** The usage of Repeat Prefixes (F2H, F3H) with ANDNPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with ANDNPS risks incompatibility with future processors.
ANDPS: Bit-wise Logical And for Single-FP

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,54,1/r</td>
<td>ANDPS xmm1, xmm2/m128</td>
<td>Logical AND of 128 bits from XMM2/Mem to XMM1 register.</td>
</tr>
</tbody>
</table>

**Operation:**
\[ \text{xmm1}[127:0] \&= \text{xmm2/m128}[127:0]; \]

**Description:** The ANDPS instruction returns a bit-wise logical AND between XMM1 and XMM2/Mem.

**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** None

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CRCR4.OSFxSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CRCR4.OSFxSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

- Same exceptions as in Real Address Mode;
- #PF(fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults Disabled FP Register Fault if PSR.df is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

**Comments:** The usage of Repeat Prefixes (F2H, F3H) with ANDPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with ANDPS risks incompatibility with future processors.
CMPPS: Packed Single-FP Compare

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,C2,/r,ib</td>
<td>CMPPS xmm1, xmm2/m128, imm8</td>
<td>Compare packed SP FP numbers from XMM2/Mem to packed SP FP numbers in XMM1 register using imm8 as predicate.</td>
</tr>
</tbody>
</table>

**Operation:**
```
switch (imm8) {
    case eq:  op = eq;
    case lt:  op = lt;
    case le:  op = le;
    case unord:  op = unord;
    case neq:  op = neq;
    case nlt:  op = nlt;
    case nle:  op = nle;
    case ord:  op = ord;
    default:  Reserved;
}
```

```c
cmp0 = op(xmm1[31-0],xmm2/m128[31-0]);
cmp1 = op(xmm1[63-32],xmm2/m128[63-32]);
cmp2 = op(xmm1[95-64],xmm2/m128[95-64]);
cmp3 = op(xmm1[127-96],xmm2/m128[127-96]);
```

```c
xmm1[31-0]   = (cmp0) ? 0xffffffff : 0x00000000;
xmm1[63-32]  = (cmp1) ? 0xffffffff : 0x00000000;
xmm1[95-64]  = (cmp2) ? 0xffffffff : 0x00000000;
xmm1[127-96] = (cmp3) ? 0xffffffff : 0x00000000;
```

**Description:**
For each individual pairs of SP FP numbers, the CMPPS instruction returns an all “1” 32-bit mask or an all “0” 32-bit mask, using the comparison predicate specified by imm8; note that a subsequent computational instruction which uses this mask as an input operand will not generate a fault, since a mask of all “0”s corresponds to a FP value of +0.0 and a mask of all “1”s corresponds to a FP value of -qNaN. Some of the comparisons can be achieved only through software emulation. For these comparisons the programmer must swap the operands, copying registers when necessary to protect the data that will now be in the destination, and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in under the heading “Emulation”. The following table shows the different comparison types:
**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** Invalid if sNaN operand, invalid if qNaN and predicate as listed in above table, denormal.

**Protected Mode Exceptions:**

#GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments; #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults | Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
Itanium Mem Faults | VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

---

<table>
<thead>
<tr>
<th>Predicate</th>
<th>Description&lt;sup&gt;a&lt;/sup&gt;</th>
<th>Relation</th>
<th>Emulation</th>
<th>imm8 Encoding</th>
<th>Result if NaN Operand</th>
<th>QNaN Operand Signals</th>
<th>Invalid</th>
</tr>
</thead>
<tbody>
<tr>
<td>eq</td>
<td>equal</td>
<td>xmm1 == xmm2</td>
<td></td>
<td>000B</td>
<td>False</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>lt</td>
<td>less-than</td>
<td>xmm1 &lt; xmm2</td>
<td></td>
<td>001B</td>
<td>False</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>le</td>
<td>less-than-or-equal</td>
<td>xmm1 ≤ xmm2</td>
<td></td>
<td>010B</td>
<td>False</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td></td>
<td>greater-than</td>
<td>xmm1 &gt; xmm2</td>
<td>swap, protect, It</td>
<td>011B</td>
<td>True</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td></td>
<td>greater-than-or-equal</td>
<td>xmm1 ≥ xmm2</td>
<td>swap protect, le</td>
<td>100B</td>
<td>True</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td></td>
<td>unordered</td>
<td>xmm1 ≠ xmm2</td>
<td></td>
<td>101B</td>
<td>True</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>neq</td>
<td>not-equal</td>
<td>!(xmm1 == xmm2)</td>
<td></td>
<td>110B</td>
<td>True</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>nlt</td>
<td>not-less-than</td>
<td>!(xmm1 &lt; xmm2)</td>
<td></td>
<td>111B</td>
<td>True</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>nle</td>
<td>not-less-than-or-equal</td>
<td>!(xmm1 ≤ xmm2)</td>
<td></td>
<td>False</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>greater-than</td>
<td>!(xmm1 &gt; xmm2)</td>
<td>swap, protect, nlt</td>
<td>False</td>
<td>No</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ngt</td>
<td>not-greater-than</td>
<td>!(xmm1 ≥ xmm2)</td>
<td>swap, protect, nle</td>
<td>True</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ord</td>
<td>ordered</td>
<td>!(xmm1 ≠ xmm2)</td>
<td></td>
<td>True</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<sup>a</sup> The greater-than, greater-than-or-equal, not-greater-than, and not-greater-than-or-equal relations are not directly implemented in hardware.
Comments: Compilers and assemblers should implement the following 2-operand pseudo-ops in addition to the 3-operand CMPPS instruction:

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPEQPS xmm1, xmm2</td>
<td>CMPPS xmm1,xmm2, 0</td>
</tr>
<tr>
<td>CMPLTPS xmm1, xmm2</td>
<td>CMPPS xmm1,xmm2, 1</td>
</tr>
<tr>
<td>CMPLEPS xmm1, xmm2</td>
<td>CMPPS xmm1,xmm2, 2</td>
</tr>
<tr>
<td>CMPUNORDPS xmm1, xmm2</td>
<td>CMPPS xmm1,xmm2, 3</td>
</tr>
<tr>
<td>CMPNEQPS xmm1, xmm2</td>
<td>CMPPS xmm1,xmm2, 4</td>
</tr>
<tr>
<td>CMPNLTPS xmm1, xmm2</td>
<td>CMPPS xmm1,xmm2, 5</td>
</tr>
<tr>
<td>CMPNLEPS xmm1, xmm2</td>
<td>CMPPS xmm1,xmm2, 6</td>
</tr>
<tr>
<td>CMPORDPS xmm1, xmm2</td>
<td>CMPPS xmm1,xmm2, 7</td>
</tr>
</tbody>
</table>

The greater-than relations not implemented in hardware require more than one instruction to emulate in software and therefore should not be implemented as pseudo-ops. (For these, the programmer should reverse the operands of the corresponding less than relations and use move instructions to ensure that the mask is moved to the correct destination register and that the source operand is left intact.)

Bits 7-4 of the immediate field are reserved. Different processors may handle them differently. Usage of these bits risks incompatibility with future processors.
CMPSS: Scalar Single-FP Compare

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3.0F,C2,/r,ib</td>
<td>CMPSS xmm1, xmm2/m32, imm8</td>
<td>Compare lowest SP FP number from XMM2/Mem to lowest SP FP number in XMM1 register using imm8 as predicate.</td>
</tr>
</tbody>
</table>

Operation:

```
switch (imm8) {
    case eq:    op = eq;
    case lt:    op = lt;
    case le:    op = le;
    case unord: op = unord;
    case neq:   op = neq;
    case nlt:   op = nlt;
    case nle:   op = nle;
    case ord:   op = ord;
    default:    Reserved;
}
```

cmp0 = op(xmm1[31-0],xmm2/m32[31-0]);

```
xmm1[31-0]    = (cmp0) ? 0xffffffff : 0x00000000;
xmm1[63-32]   = xmm1[63-32];
xmm1[95-64]   = xmm1[95-64];
xmm1[127-96]  = xmm1[127-96];
```

Description: For the lowest pair of SP FP numbers, the CMPSS instruction returns an all “1” 32-bit mask or an all “0” 32-bit mask, using the comparison predicate specified by imm8; the values for the upper three pairs of SP FP numbers are not compared. Note that a subsequent computational instruction which uses this mask as an input operand will not generate a fault, since a mask of all “0’s” corresponds to a FP value of +0.0 and a mask of all “1’s” corresponds to a FP value of -qNaN. Some of the comparisons can be achieved only through software emulation. For these comparisons the programmer must swap the operands, copying registers when necessary to protect the data that will now be in the destination, and then perform the compare using a different predicate. The predicate to be used for these emulations is listed in under the heading “Emulation”. The following table shows the different comparison types:
### FP Exceptions
None.

### Numeric Exceptions
Invalid if sNaN operand, invalid if qNaN and predicate as listed in above table, denormal.

### Protected Mode Exceptions

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

### Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

### Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

### Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault

### Table: Predicate Description and Encoding

<table>
<thead>
<tr>
<th>Predicate</th>
<th>Description</th>
<th>Relation</th>
<th>Emulation</th>
<th>imm8 Encoding</th>
<th>Result if NaN Operand</th>
<th>qNaN Operand Signals</th>
<th>Invalid</th>
</tr>
</thead>
<tbody>
<tr>
<td>eq</td>
<td>equal</td>
<td>xmm1 == xmm2</td>
<td></td>
<td>000B</td>
<td>False</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>lt</td>
<td>less-than</td>
<td>xmm1 &lt; xmm2</td>
<td>swap, protect, lt</td>
<td>001B</td>
<td>False</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>le</td>
<td>less-than-or-equal</td>
<td>xmm1 &lt;= xmm2</td>
<td>swap, protect, le</td>
<td>010B</td>
<td>False</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>gt</td>
<td>greater</td>
<td>xmm1 &gt; xmm2</td>
<td></td>
<td>011B</td>
<td>True</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>ge</td>
<td>greater-or-equal</td>
<td>xmm1 &gt;= xmm2</td>
<td></td>
<td>100B</td>
<td>True</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>unordered</td>
<td>unordered</td>
<td>xmm1 ? xmm2</td>
<td></td>
<td>101B</td>
<td>True</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>neq</td>
<td>not-equal</td>
<td>!(xmm1 == xmm2)</td>
<td></td>
<td>110B</td>
<td>True</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>nlt</td>
<td>not-less-than</td>
<td>!(xmm1 &lt; xmm2)</td>
<td></td>
<td>111B</td>
<td>False</td>
<td>No</td>
<td></td>
</tr>
<tr>
<td>nle</td>
<td>not-less-than-or-equal</td>
<td>!(xmm1 &lt;= xmm2)</td>
<td></td>
<td></td>
<td>True</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>not-gt</td>
<td>not-greater</td>
<td>!(xmm1 &gt; xmm2)</td>
<td></td>
<td></td>
<td>True</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>nge</td>
<td>not-greater-or-equal</td>
<td>!(xmm1 &gt;= xmm2)</td>
<td></td>
<td></td>
<td>True</td>
<td>Yes</td>
<td></td>
</tr>
<tr>
<td>ord</td>
<td>ordered</td>
<td>!(xmm1 ? xmm2)</td>
<td></td>
<td></td>
<td>False</td>
<td>No</td>
<td></td>
</tr>
</tbody>
</table>

a. The greater-than, greater-than-or-equal, not-greater-than, and not-greater-than-or-equal relations are not directly implemented in hardware.
Itanium Mem Faults

VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments: Compilers and assemblers should implement the following 2-operand pseudo-ops in addition to the 3-operand CMPSS instruction:

<table>
<thead>
<tr>
<th>Pseudo-Op</th>
<th>Implementation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMPEQSS xmm1, xmm2</td>
<td>CMPSS xmm1,xmm2, 0</td>
</tr>
<tr>
<td>CMPLTSS xmm1, xmm2</td>
<td>CMPSS xmm1,xmm2, 1</td>
</tr>
<tr>
<td>CMPLESS xmm1, xmm2</td>
<td>CMPSS xmm1,xmm2, 2</td>
</tr>
<tr>
<td>CMPUNORDSS xmm1, xmm2</td>
<td>CMPSS xmm1,xmm2, 3</td>
</tr>
<tr>
<td>CMPNEQSS xmm1, xmm2</td>
<td>CMPSS xmm1,xmm2, 4</td>
</tr>
<tr>
<td>CMPNLSSS xmm1, xmm2</td>
<td>CMPSS xmm1,xmm2, 5</td>
</tr>
<tr>
<td>CMPNLESSS xmm1, xmm2</td>
<td>CMPSS xmm1,xmm2, 6</td>
</tr>
<tr>
<td>CMPORDSS xmm1, xmm2</td>
<td>CMPSS xmm1,xmm2, 7</td>
</tr>
</tbody>
</table>

The greater-than relations not implemented in hardware require more than one instruction to emulate in software and therefore should not be implemented as pseudo-ops. (For these, the programmer should reverse the operands of the corresponding less than relations and use move instructions to ensure that the mask is moved to the correct destination register and that the source operand is left intact.)

Bits 7-4 of the immediate field are reserved. Different processors may handle them differently. Usage of these bits risks incompatibility with future processors.
COMISS: Scalar Ordered Single-FP Compare and set EFLAGS

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,2F,lr</td>
<td>COMISS xmm1, xmm2/m32</td>
<td>Compare lower SP FP number in XMM1 register with lower SP FP number in XMM2/Mem and set the status flags accordingly</td>
</tr>
</tbody>
</table>

Operation:

```
switch (xmm1[31-0] <> xmm2/m32[31-0]) {
    OF, SF, AF = 000;
    case UNORDERED:     ZF, PF, CF = 111;
    case GREATER_THAN:  ZF, PF, CF = 000;
    case LESS_THAN:     ZF, PF, CF = 001;
    case EQUAL:         ZF, PF, CF = 100;
}
```

Description: The COMISS instructions compare two SP FP numbers and sets the ZF,PF,CF bits in the EFLAGS register as described above. Although the data type is packed single-FP, only the lower SP numbers are compared. In addition, the OF, SF and AF bits in the EFLAGS register are zeroed out. The unordered predicate is returned if either source operand is a NaN (qNaN or sNaN).

FP Exceptions: None.

Numeric Exceptions: Invalid (if SNaN or QNaN operands), Denormal. Integer EFLAGS values will not be updated in the presence of unmasked numeric exceptions.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EF = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFFH; #UD if CR0.EF = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.
COMISS: Scalar Ordered Single-FP Compare and set EFLAGS (Continued)

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments: COMISS differs from UCOMISS in that it signals an invalid numeric exception when a source operand is either a qNaN or sNaN; UCOMISS signals invalid only if a source operand is an sNaN.

The usage of Repeat (F2H, F3H) and Operand-Size (66H) prefixes with COMISS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with COMISS risks incompatibility with future processors.
CVTPI2PS: Packed Signed INT32 to Packed Single-FP Conversion

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,2A/r</td>
<td>CVTPI2PS xmm, mm/m64</td>
<td>Convert two 32-bit signed integers from MM/Mem to two SP FP.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\begin{align*}
\text{xmm}[31-0] &= (\text{float}) (\text{mm/m64}[31-0]); \\
\text{xmm}[63-32] &= (\text{float}) (\text{mm/m64}[63-32]); \\
\text{xmm}[95-64] &= \text{xmm}[95-64]; \\
\text{xmm}[127-96] &= \text{xmm}[127-96];
\end{align*}
\]

**Description:** The CVTPI2PS instruction converts signed 32-bit integers to SP FP numbers; when the conversion is inexact, rounding is done according to MXCSR.

**FP Exceptions:** None.

**Numeric Exceptions:** Precision.

**Protected Mode Exceptions:**

#GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments; #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception; #AC for unaligned memory reference; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception; #AC for unaligned memory reference; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults Disabled FP Register Fault if PSR.df1 is 1, NaT Register Consumption Fault.

Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault.
CVTPI2PS: Packed Signed INT32 to Packed Single-FP Conversion
(Continued)

Comments: This instruction behaves identically to original MMX instructions, in the presence of x87-FP instructions:

- Transition from x87-FP to MMX technology (TOS=0, FP valid bits set to all valid).
- MMX instructions write ones (1’s) to the exponent part of the corresponding x87-FP register.

However, the use of a memory source operand with this instruction will not result in the above transition from x87-FP to MMX technology.

Prioritization for fault and assist behavior for CVTPI2PS is as follows:

Memory source
1. Invalid opcode (CR0.EM=1)
2. DNA (CR0.TS=1)
3. #SS or #GP, for limit violation
4. #PF, page fault
5. Streaming SIMD Extension numeric fault (i.e. precision)

Register source
1. Invalid opcode (CR0.EM=1)
2. DNA (CR0.TS=1)
3. #MF, pending x87-FP fault signalled
4. After returning from #MF, x87-FP->MMX technology transition
5. Streaming SIMD Extension numeric fault (i.e. precision)
CVTPS2PI: Packed Single-FP to Packed INT32 Conversion

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,2D,/r</td>
<td>CVTPS2PI mm, xmm/m64</td>
<td>Convert lower 2 SP FP from XMM/Mem to 2 32-bit signed integers in MM using rounding specified by MXCSR.</td>
</tr>
</tbody>
</table>

Operation:  
mm[31-0] = (int) (xmm/m64[31-0]);  
mm[63-32] = (int) (xmm/m64[63-32]);

Description:  
The CVTPS2PI instruction converts the lower 2 SP FP numbers in xmm/m64 to signed 32-bit integers in mm; when the conversion is inexact, the value rounded according to the MXCSR is returned. If the converted result(s) is/are larger than the maximum signed 32 bit value, the Integer Indefinite value (0x80000000) will be returned.

FP Exceptions: None.

Numeric Exceptions: Invalid, Precision.

Protected Mode Exceptions:
- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #MF if there is a pending FPU exception;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3);
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0);
- #UD if CR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:
- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #MF if there is a pending FPU exception;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0);
- #UD if CR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:
- Same exceptions as in Real Address Mode;
- #AC for unaligned memory reference if the current privilege level is 3;
- #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions
- Itanium Reg Faults:
  - Disabled FP Register Fault if PSR.dfl is 1;
  - NaT Register Consumption Fault
- Itanium Mem Faults:
  - VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments: This instruction behaves identically to original MMX instructions, in the presence of x87-FP instructions, including:
**CVTPS2PI: Packed Single-FP to Packed INT32 Conversion** (Continued)

- Transition from x87-FP to MMX technology (TOS=0, FP valid bits set to all valid).
- MMX instructions write ones (1’s) to the exponent part of the corresponding x87-FP register.

Prioritization for fault and assist behavior for CVTPS2PI is as follows:

**Memory source**
1. Invalid opcode (CR0.EM=1)
2. DNA (CR0.TS=1)
3. #MF, pending x87-FP fault signalled
4. After returning from #MF, x87-FP->MMX technology transition
5. #SS or #GP, for limit violation
6. #PF, page fault
7. Streaming SIMD Extension numeric fault (i.e. invalid, precision)

**Register source**
1. Invalid opcode (CR0.EM=1)
2. DNA (CR0.TS=1)
3. #MF, pending x87-FP fault signalled
4. After returning from #MF, x87-FP->MMX technology transition
5. Streaming SIMD Extension numeric fault (i.e. precision)
CVTSI2SS: Scalar signed INT32 to Single-FP Conversion

Opcode | Instruction | Description
--- | --- | ---
F3.0F,2A,/r | CVTSI2SS xmm, r/m32 | Convert one 32-bit signed integer from Integer Reg/Mem to one SP FP.

Operation:

\[
\begin{align*}
\text{xmm}[31-0] &= (\text{float}) (r/m32); \\
\text{xmm}[63-32] &= \text{xmm}[63-32]; \\
\text{xmm}[95-64] &= \text{xmm}[95-64]; \\
\text{xmm}[127-96] &= \text{xmm}[127-96]; \\
\end{align*}
\]

Description: The CVTSI2SS instruction converts a signed 32-bit integer from memory or from a 32-bit integer register to a SP FP number; when the conversion is inexact, rounding is done according to the MXCSR.

FP Exceptions: None.

Numeric Exceptions: Precision.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Volume 3: IA-32 Streaming SIMD Extension Instruction Reference 3:849
CVTSS2SI: Scalar Single-FP to Signed INT32 Conversion

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3,0F,2D,/r</td>
<td>CVTSS2SI r32, xmm/m32</td>
<td>Convert one SP FP from XMM/Mem to one 32 bit signed integer using rounding mode specified by MXCSR, and move the result to an integer register.</td>
</tr>
</tbody>
</table>

**Operation:**

\[ r32 = (\text{int}) (\text{xmm/m32}[31-0]) \]

**Description:**
The CVTSS2SI instruction converts a SP FP number to a signed 32-bit integer and returns it in the 32-bit integer register; when the conversion is inexact, the rounded value according to the MXCSR is returned. If the converted result is larger than the maximum signed 32 bit integer, the Integer Indefinite value (0x80000000) will be returned.

**FP Exceptions:** None.

**Numeric Exceptions:** Invalid, Precision.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3);
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0);
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0);
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
**CVTTPS2PI: Packed Single-FP to Packed INT32 Conversion (truncate)**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,2C,/r</td>
<td>CVTTPS2PI mm, xmm/m64</td>
<td>Convert lower 2 SP FP from XMM/Mem to 2 32-bit signed integers in MM using truncate.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\begin{align*}
\text{mm}[31-0] &= \text{(int)} \left( \text{xmm/m64}[31-0] \right); \\
\text{mm}[63-32] &= \text{(int)} \left( \text{xmm/m64}[63-32] \right);
\end{align*}
\]

**Description:**

The CVTTPS2PI instruction converts the lower 2 SP FP numbers in xmm/m64 to 2 32-bit signed integers in mm; if the conversion is inexact, the truncated result is returned. If the converted result(s) is/are larger than the maximum signed 32 bit value, the Integer Indefinite value (0x80000000) will be returned.

**FP Exceptions:** None.

**Numeric Exceptions:** Invalid, Precision.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.E[1] = 1;
- #NM if TS bit in CR0 is set;
- #MF if there is a pending FPU exception;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3);
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0);
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.E[1] = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception;

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
CVTTPS2PI: Packed Single-FP to Packed INT32 Conversion (truncate)
(Continued)

Comments: This instruction behaves identically to original MMX instructions, in the presence of x87-FP instructions, including:

- Transition from x87-FP to MMX technology (TOS=0, FP valid bits set to all valid).
- MMX instructions write ones (1’s) to the exponent part of the corresponding x87-FP register.

Prioritization for fault and assist behavior for CVTTPS2PI is as follows:

Memory source
1. Invalid opcode (CR0.EM=1)
2. DNA (CR0.TS=1)
3. #MF, pending x87-FP fault signalled
4. After returning from #MF, x87-FP->MMX technology transition
5. #SS or #GP, for limit violation
6. #PF, page fault
7. Streaming SIMD Extension numeric fault (i.e. invalid, precision)

Register source
1. Invalid opcode (CR0.EM=1)
2. DNA (CR0.TS=1)
3. #MF, pending x87-FP fault signalled
4. After returning from #MF, x87-FP->MMX technology transition
5. Streaming SIMD Extension numeric fault (i.e. precision)
**CVTSS2SI: Scalar Single-FP to signed INT32 Conversion (truncate)**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3.0F.2C./r</td>
<td>CVTSS2SI r32, xmm/m32</td>
<td>Convert lowest SP FP from XMM/Mem to one 32 bit signed integer using truncate, and move the result to an integer register.</td>
</tr>
</tbody>
</table>

**Operation:**  
\[
\text{r32} = (\text{int}) \ (\text{xmm/m32}[31\text{--}0])
\]

**Description:** The CVTSS2SI instruction converts a SP FP number to a signed 32-bit integer and returns it in the 32-bit integer register; if the conversion is inexact, the truncated result is returned. If the converted result is larger than the maximum signed 32 bit value, the Integer Indefinite value (0x80000000) will be returned.

**FP Exceptions:** None.

**Numeric Exceptions:** Invalid, Precision.

**Protected Mode Exceptions:**
- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**
- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**
- Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**
- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
DIVPS: Packed Single-FP Divide

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,5E,/r</td>
<td>DIVPS xmm1, xmm2/m128 Divide packed SP FP numbers in XMM1 by XMM2/Mem</td>
</tr>
</tbody>
</table>

**Operation:**

\[
xmm1[31-0] = \frac{xmm1[31-0]}{(xmm2/m128[31-0])};
\]

\[
xmm1[63-32] = \frac{xmm1[63-32]}{(xmm2/m128[63-32])};
\]

\[
xmm1[95-64] = \frac{xmm1[95-64]}{(xmm2/m128[95-64])};
\]

\[
xmm1[127-96] = \frac{xmm1[127-96]}{(xmm2/m128[127-96])};
\]

**Description:**
The DIVPS instruction divides the packed SP FP numbers of both their operands.

**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** Overflow, Underflow, Invalid, Divide by Zero, Precision, Denormal.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EF = 1;
- #NM if TS bit in CR0 is set;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0);
- #UD if CR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;
- #UD if CR0.EF = 1;
- #NM if TS bit in CR0 is set;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0);
- #UD if CR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
DIVSS: Scalar Single-FP Divide

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3,0F,5E,/r</td>
<td>DIVSS xmm1, xmm2/m32</td>
<td>Divide lower SP FP numbers in XMM1 by XMM2/Mem</td>
</tr>
</tbody>
</table>

**Operation:**

- \( \text{xmm1}[31-0] = \text{xmm1}[31-0] / (\text{xmm2/m32}[31-0]) \);  
- \( \text{xmm1}[63-32] = \text{xmm1}[63-32] \);  
- \( \text{xmm1}[95-64] = \text{xmm1}[95-64] \);  
- \( \text{xmm1}[127-96] = \text{xmm1}[127-96] \);  

**Description:** The DIVSS instructions divide the lowest SP FP numbers of both operands; the upper 3 fields are passed through from xmm1.

**FP Exceptions:** None.

**Numeric Exceptions:** Overflow, Underflow, Invalid, Divide by Zero, Precision, Denormal.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;  
- #SS(0) for an illegal address in the SS segment;  
- #PF (fault-code) for a page fault;  
- #UD if CR0.EM = 1;  
- #NM if TS bit in CR0 is set;  
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3);  
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1);  
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0);  
- #UD if CRCR4.OSFXSR(bit 9) = 0;  
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;  
- #UD if CR0.EM = 1;  
- #NM if TS bit in CR0 is set;  
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1);  
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0);  
- #UD if CRCR4.OSFXSR(bit 9) = 0;  
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

- Same exceptions as in Real Address Mode;  
- #AC for unaligned memory reference if the current privilege level is 3;  
- #PF (fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults  
- Disabled FP Register Fault if PSR.df is 1, NaT Register Consumption Fault  
- Itanium Mem Faults  
- VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
FXRSTOR: Restore FP and Intel® MMX™ State and Streaming SIMD Extension State

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,AE,/1</td>
<td>FXRSTOR m512byte</td>
<td>Load FP/Intel® MMX™ and Streaming SIMD Extension state from m512byte.</td>
</tr>
</tbody>
</table>

**Operation:** FP and MMX state and Streaming SIMD Extension state = m512byte;

**Description:** The FXRSTOR instruction reloads the FP and MMX technology state and Streaming SIMD Extension state (environment and registers) from the memory area defined by m512byte. This data should have been written by a previous FXSAVE.

The FP and MMX technology and Streaming SIMD Extension environment and registers consist of the following data structure (little-endian byte order as arranged in memory, with byte offset into row described by right column):

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
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<tbody>
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<tr>
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Three fields in the floating-point save area contain reserved bits that are not indicated in the table:

- **FOP**: The lower 11-bits contain the opcode, upper 5-bits are reserved.
- **IP & DP**: 32-bit mode: 32-bit IP-offset.
- **16-bit mode**: lower 16-bits are IP-offset and upper 16-bits are reserved.

If the MXCSR state contains an unmasked exception with corresponding status flag also set, loading it will not result in a floating-point error condition being asserted; only the next occurrence of this unmasked exception will result in the error condition being asserted.

Some bits of MXCSR (bits 31-16 and bit 6) are defined as reserved and cleared; attempting to write a non-zero value to these bits will result in a general protection exception.

FXRSTOR does not flush pending x87-FP exceptions, unlike FRSTOR. To check and raise exceptions when loading a new operating environment, use FWAIT after FXRSTOR.

The Streaming SIMD Extension fields in the save image (XMM0-XMM7 and MXCSR) may not be loaded into the processor if the CR4.OSFXSR bit is not set. This CR4 bit must be set in order to enable execution of Streaming SIMD Extension instructions.

**FP Exceptions**: If #AC exception detection is disabled, a general protection exception is signalled if the address is not aligned on 16-byte boundary. Note that if #AC is enabled (and CPL is 3), signalling of #AC is not guaranteed and may vary with implementation; in all implementations where #AC is not signalled, a general protection fault will instead be signalled. In addition, the width of the alignment check when #AC is enabled may also vary with implementation; for instance, for a given implementation #AC might be signalled for a 2-byte misalignment, whereas #GP might be signalled for all other misalignments (4/8/16-byte). Invalid opcode exception if instruction is preceded by a LOCK override prefix. General protection fault if reserved bits of MXCSR are loaded with non-zero values.

**Numeric Exceptions**: None

**Protected Mode Exceptions**:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #NM if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

**Real Address Mode Exceptions**:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #NM if CR0.EM = 1; #NM if TS bit in CR0 is set.
FXRSTOR: Restore FP and Intel® MMX™ State and Streaming SIMD Extension State (Continued)

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Notes:

State saved with FXSAVE and restored with FRSTOR (and vice versa) will result in incorrect restoration of state in the processor. The address size prefix will have the usual effect on address calculation but will have no effect on the format of the FXRSTOR image.

The use of Repeat (F2H, F3H) and Operand Size (66H) prefixes with FXRSTOR is reserved. Different processor implementations may handle this prefix differently. Use of this prefix with FXRSTOR risks incompatibility with future processors.
FXSAVE: Store FP and Intel® MMX™ State and Streaming SIMD Extension State

**Operation:** m512byte = FP and MMX state and Streaming SIMD Extension state;

**Description:** The FXSAVE instruction writes the current FP and MMX technology state and Streaming SIMD Extension state (environment and registers) to the specified destination defined by m512byte. It does this without checking for pending unmasked floating-point exceptions, similar to the operation of FNSAVE. Unlike the FSAVE/FNSAVE instructions, the processor retains the contents of the FP and MMX technology state and Streaming SIMD Extension state in the processor after the state has been saved. This instruction has been optimized to maximize floating-point save performance. The save data structure is as follows (little-endian byte order as arranged in memory, with byte offset into row described by right column):

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,AE,0</td>
<td>FXSAVE m512byte</td>
<td>Store FP and Intel® MMX™ state and Streaming SIMD Extension state to m512byte.</td>
</tr>
</tbody>
</table>

<table>
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<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
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- **IP & DP**: 32-bit mode: 32-bit IP-offset.
- **16-bit mode**: lower 16-bits are IP-offset and upper 16-bits are reserved.

The **FXSAVE** instruction is used when an operating system needs to perform a context switch or when an exception handler needs to use the FP and MMX technology and Streaming SIMD Extension units. It cannot be used by an application program to pass a “clean” FP state to a procedure, since it retains the current state. An application must explicitly execute an **FINIT** instruction after **FXSAVE** to provide for this functionality.

All of the x87-FP fields retain the same internal format as in **FSAVE** except for **FTW**.

Unlike **FSAVE**, **FXSAVE** saves only the FTW valid bits rather than the entire x87-FP FTW field. The FTW bits are saved in a non-TOS relative order, which means that FR0 is always saved first, followed by FR1, FR2 and so forth. As an example, if TOS=4 and only ST0, ST1 and ST2 are valid, FSAVE saves the FTW field in the following format:

```
ST3  ST2  ST1  ST0  ST7  ST6  ST5  ST4 (TOS=4)
FR7  FR6  FR5  FR4  FR3  FR2  FR1  FR0
11  xx  xx  xx  11  11  11  11
```

where xx is one of (00, 01, 10). (11) indicates an empty stack elements, and the 00, 01, and 10 indicate Valid, Zero, and Special, respectively. In this example, **FXSAVE** would save the following vector:

```
FR7  FR6  FR5  FR4  FR3  FR2  FR1  FR0
0  1  1  1  0  0  0  0
```

The FSAVE format for FTW can be recreated from the FTW valid bits and the stored 80-bit FP data (assuming the stored data was not the contents of MMX technology registers) using the following table:

<table>
<thead>
<tr>
<th>Exponent all 1's</th>
<th>Exponent all 0's</th>
<th>Fraction all 0's</th>
<th>J and M bits</th>
<th>FTW valid bit</th>
<th>x87 FTW</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0x</td>
<td>1</td>
<td>Special 10</td>
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<td>1x</td>
<td>1</td>
<td>Special 10</td>
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</tbody>
</table>
The J-bit is defined to be the 1-bit binary integer to the left of the decimal place in the significand. The M-bit is defined to be the most significant bit of the fractional portion of the significand (i.e. the bit immediately to the right of the decimal place).

When the M-bit is the most significant bit of the fractional portion of the significand, it must be 0 if the fraction is all 0’s.

If the FXSAVE instruction is immediately preceded by an FP instruction which does not use a memory operand, then the FXSAVE instruction does not write/update the DP field, in the FXSAVE image.

MXCSR holds the contents of the Streaming SIMD Extension Control/Status Register. See the LDMXCSR instruction for a full description of this field.

The fields XMM0-XMM7 contain the content of registers XMM0-XMM7 in exactly the same format as they exist in the registers.

The Streaming SIMD Extension fields in the save image (XMM0-XMM7 and MXCSR) may not be loaded into the processor if the CR4.OSFXSR bit is not set. This CR4 bit must be set in order to enable execution of Streaming SIMD Extension instructions.

The destination m512byte is assumed to be aligned on a 16-byte boundary. If m512byte is not aligned on a 16-byte boundary, FXSAVE generates a general protection exception.

**FP Exceptions:** If #AC exception detection is disabled, a general protection exception is signalled if the address is not aligned on 16-byte boundary. Note that if #AC is enabled (and CPL is 3), signalling of #AC is not guaranteed and may vary with implementation; in all implementations where #AC is not signalled, a general protection fault will instead be signalled. In addition, the width of the alignment check when #AC is enabled may also vary with implementation; for instance, for a given implementation #AC might be signalled for a 2-byte misalignment, whereas #GP might be signalled for all other misalignments (4/8/16-byte). Invalid opcode exception if instruction is preceded by a LOCK override prefix.

**Numeric Exceptions:** None

**Protected Mode Exceptions:**

#GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments; #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #NM if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3).
FXSAVE: Store FP and Intel® MMX™ State and Streaming SIMD Extension State (Continued)

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #NM if CR0.EM = 1; #NM if TS bit in CR0 is set.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
Itanium Mem Faults  VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Notes:

State saved with FXSAVE and restored with FRSTOR (and vice versa) will result in incorrect restoration of state in the processor. The address size prefix will have the usual effect on address calculation but will have no effect on the format of the FXSAVE image.

If there is a pending unmasked FP exception at the time FXSAVE is executed, the sequence of FXSAVE-FWAIT-FXRSTOR will result in incorrect state in the processor. The FWAIT instruction causes the processor to check and handle pending unmasked FP exceptions. Since the processor does not clear the FP state with FXSAVE (unlike FSAVE), the exception is handled but that fact is not reflected in the saved image. When the image is reloaded using FXRSTOR, the exception bits in FSW will be incorrectly reloaded.

The use of Repeat (F2H, F3H) and Operand Size (66H) prefixes with FXSAVE is reserved. Different processor implementations may handle this prefix differently. Use of these prefixes with FXSAVE risks incompatibility with future processors.
LDMXCSR: Load Streaming SIMD Extension Control/Status

### Operation

MXCSR = m32;

### Description

The MXCSR control/status register is used to enable masked/unmasked exception handling, to set rounding modes, to set flush-to-zero mode, and to view exception status flags. The following figure shows the format and encoding of the fields in MXCSR.

<table>
<thead>
<tr>
<th>31-16</th>
<th>15</th>
<th>10</th>
<th>5</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td>FZ</td>
<td>RC</td>
<td>RC</td>
<td>PM</td>
</tr>
</tbody>
</table>

Bits 5-0 indicate whether a Streaming SIMD Extension numerical exception has been detected. They are “sticky” flags, and can be cleared by using the LDMXCSR instruction to write zeroes to these fields. If a LDMXCSR instruction clears a mask bit and sets the corresponding exception flag bit, an exception will not be immediately generated. The exception will occur only upon the next Streaming SIMD Extension to cause this type of exception. A Streaming SIMD Extension uses only one exception flag for each exception. There is no provision for individual exception reporting within a packed data type. In situations where multiple identical exceptions occur within the same instruction, the associated exception flag is updated and indicates that at least one of these conditions happened. These flags are cleared upon reset.

Bits 12-7 configure numerical exception masking; an exception type is masked if the corresponding bit is set and it is unmasked if the bit is clear. These enables are set upon reset, meaning that all numerical exceptions are masked.

Bits 14-13 encode the rounding-control, which provides for the common round-to-nearest mode, as well as directed rounding and true chop. Rounding control affects the arithmetic instructions and certain conversion instructions. The encoding for RC is as follows:

<table>
<thead>
<tr>
<th>Rounding Mode</th>
<th>RC Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Round to nearest (even)</td>
<td>00B</td>
<td>Rounded result is the closest to the infinitely precise result. If two values are equally close, the result is the even value (that is, the one with the least-significant bit of zero).</td>
</tr>
<tr>
<td>Round down (to minus infinity)</td>
<td>01B</td>
<td>Rounded result is close to but no greater than the infinitely precise result</td>
</tr>
<tr>
<td>Round up (toward positive infinity)</td>
<td>10B</td>
<td>Rounded result is close to but no less than the infinitely precise result.</td>
</tr>
<tr>
<td>Round toward zero (truncate)</td>
<td>11B</td>
<td>Rounded result is close to but no greater in absolute value than the infinitely precise result.</td>
</tr>
</tbody>
</table>

The rounding-control is set to round to nearest upon reset.

Bit 15 (FZ) is used to turn on the Flush To Zero mode (bit is set). Turning on the Flush To Zero mode has the following effects during underflow situations:

- Zero results are returned with the sign of the true result.
- Precision and underflow exception flags are set.
LDMXCSR: Load Streaming SIMD Extension Control/Status (Continued)

The IEEE mandated masked response to underflow is to deliver the denormalized result (i.e. gradual underflow); consequently, the flush to zero mode is not compatible with IEEE Std. 754. It is provided primarily for performance reasons. At the cost of a slight precision loss, faster execution can be achieved for applications where underflows are common. Unmasking the underflow exception takes precedence over Flush To Zero mode; this means that an exception handler will be invoked for a Streaming SIMD Extension instruction that generates an underflow condition while this exception is unmasked, regardless of whether flush to zero is enabled.

The other bits of MXCSR (bits 31-16 and bit 6) are defined as reserved and cleared; attempting to write a non-zero value to these bits, using either the FXRSTOR or LDMXCSR instructions, will result in a general protection exception.

The linear address corresponds to the address of the least-significant byte of the referenced memory data.

FP Exceptions: General protection fault if reserved bits are loaded with non-zero values.

Numeric Exceptions: None

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault. #AC for unaligned memory reference.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments: The usage of Repeat (F2H, F3H) and Operand Size (66H) prefixes with LDMXCSR is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with LDMXCSR risks incompatibility with future processors.
MAXPS: Packed Single-FP Maximum

<table>
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<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,5F,ir</td>
<td>MAXPS xmm1, xmm2/m128</td>
<td>Return the maximum SP FP numbers between XMM2/Mem and XMM1.</td>
</tr>
</tbody>
</table>

Operation:

\[
\text{xmm1[31-0]} = \begin{cases} 
\text{NAN} & \text{if } \text{xmm1[31-0]} == \text{NAN} \\
\text{xmm2[31-0]} & \text{otherwise}
\end{cases} \\
\text{m128[31-0];}
\]

\[
\text{xmm1[63-32]} = \begin{cases} 
\text{NAN} & \text{if } \text{xmm1[63-32]} == \text{NAN} \\
\text{xmm2[63-32]} & \text{otherwise}
\end{cases} \\
\text{m128[63-32];}
\]

\[
\text{xmm1[95-64]} = \begin{cases} 
\text{NAN} & \text{if } \text{xmm1[95-64]} == \text{NAN} \\
\text{xmm2[95-64]} & \text{otherwise}
\end{cases} \\
\text{m128[95-64];}
\]

\[
\text{xmm1[127-96]} = \begin{cases} 
\text{NAN} & \text{if } \text{xmm1[127-96]} == \text{NAN} \\
\text{xmm2[127-96]} & \text{otherwise}
\end{cases} \\
\text{m128[127-96];}
\]

\[
\text{xmm2/m128[127-96];}
\]

Description: The MAXPS instruction returns the maximum SP FP numbers from XMM1 and XMM2/Mem. If the values being compared are both zeros, source2 (xmm2/m128) would be returned. If source2 (xmm2/m128) is an sNaN, this sNaN is forwarded unchanged to the destination (i.e. a quieted version of the sNaN is not returned).

FP Exceptions: General protection exception if not aligned on 16-byte boundary, regardless of segment.

Numeric Exceptions: Invalid (including qNaN source operand), Denormal.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.
MAXPS: Packed Single-FP Maximum (Continued)

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments:  Note that if only one source is a NaN for these instructions, the Src2 operand (either NaN or real value) is written to the result; this differs from the behavior for other instructions as defined in Table 3-3, which is to always write the NaN to the result, regardless of which source operand contains the NaN. This approach for MAXPS allows compilers to use the MAXPS instruction for common C conditional constructs. If instead of this behavior, it is required that the NaN source operand be returned, the min/max functionality can be emulated using a sequence of instructions: comparison followed by AND, ANDN and OR.
MAXSS: Scalar Single-FP Maximum

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<td>F3,0F,5F,/r</td>
<td>MAXSS xmm1, xmm2/m32</td>
<td>Return the maximum SP FP number between the lower SP FP numbers from XMM2/Mem and XMM1.</td>
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</table>

**Operation:**

\[
\begin{align*}
\text{xmm1}[31-0] & = (\text{xmm1}[31-0] == \text{NAN}) \ ? \ \text{xmm2}[31-0] : \\
& \quad (\text{xmm2}[31-0] == \text{NAN}) \ ? \ \text{xmm2}[31-0] : \\
& \quad (\text{xmm1}[31-0] > \text{xmm2}/m32[31-0]) \ ? \ \text{xmm1}[31-0] : \ \text{xmm2}/m32[31-0]; \\
\text{xmm1}[63-32] & = \text{xmm1}[63-32]; \\
\text{xmm1}[95-64] & = \text{xmm1}[95-64]; \\
\text{xmm1}[127-96] & = \text{xmm1}[127-96];
\end{align*}
\]

**Description:**
The MAXSS instruction returns the maximum SP FP number from the lower SP FP numbers of XMM1 and XMM2/Mem; the upper 3 fields are passed through from xmm1. If the values being compared are both zeros, source2 (xmm2/m128) would be returned. If source2 (xmm2/m128) is an sNaN, this sNaN is forwarded unchanged to the destination (i.e. a quieted version of the sNaN is not returned).

**FP Exceptions:** None

**Numeric Exceptions:** Invalid (including qNaN source operand), Denormal.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.
MAXSS: Scalar Single-FP Maximum (Continued)

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults  VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments:  Note that if only one source is a NaN for these instructions, the Src2 operand (either NaN or real value) is written to the result; this differs from the behavior for other instructions as defined in Table 3-3, which is to always write the NaN to the result, regardless of which source operand contains the NaN. The upper three operands are still bypassed from the src1 operand, as in all other scalar operations. This approach for MAXSS allows compilers to use the MAXSS instruction for common C conditional constructs. If instead of this behavior, it is required that the NaN source operand be returned, the min/max functionality can be emulated using a sequence of instructions: comparison followed by AND, ANDN and OR.
MINPS: Packed Single-FP Minimum

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<tr>
<td>0F,5D,/r</td>
<td>MINPS xmm1, xmm2/m128</td>
<td>Return the minimum SP numbers between XMM2/Mem and XMM1.</td>
</tr>
</tbody>
</table>

**Operation:**

- `xmm1[31-0] = (xmm1[31-0] == NAN) ? xmm2[31-0] : (xmm2[31-0] == NAN) ? xmm2[31-0] : (xmm1[31-0] < xmm2/m128[31-0]) ? xmm1[31-0] : xmm2/m128[31-0];`
- `xmm1[95-64] = (xmm1[95-64] == NAN) ? xmm2[95-64] : (xmm2[95-64] == NAN) ? xmm2[95-64] : (xmm1[95-64] < xmm2/m128[95-64]) ? xmm1[95-64] : xmm2/m128[95-64];`

**Description:**
The MINPS instruction returns the minimum SP FP numbers from XMM1 and XMM2/Mem. If the values being compared are both zeros, source2 (xmm2/m128) would be returned. If source2 (xmm2/m128) is an sNaN, this sNaN is forwarded unchanged to the destination (i.e. a quieted version of the sNaN is not returned).

**FP Exceptions:**
General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:**
Invalid (including qNaN source operand), Denormal.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.
MINPS: Packed Single-FP Minimum (Continued)

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments:  Note that if only one source is a NaN for these instructions, the Src2 operand (either NaN or real value) is written to the result; this differs from the behavior for other instructions as defined in Table 3-3, which is to always write the NaN to the result, regardless of which source operand contains the NaN. This approach for MINPS allows compilers to use the MINPS instruction for common C conditional constructs. If instead of this behavior, it is required that the NaN source operand be returned, the min/max functionality can be emulated using a sequence of instructions: comparison followed by AND, ANDN and OR.
**MINSS: Scalar Single-FP Minimum**

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<td>F3,0F,5D,ir</td>
<td>MINSS xmm1, xmm2/m32</td>
<td>Return the minimum SP FP number between the lowest SP FP numbers from XMM2/Mem and XMM1.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\text{xmm1}_{[31-0]} = \begin{cases} 
(xmm1_{[31-0]} == \text{NAN}) & \text{?} \ xmm2_{[31-0]} \\
(xmm2_{[31-0]} == \text{NAN}) & \text{?} \ xmm2_{[31-0]} \\
(xmm1_{[31-0]} < xmm2/m32_{[31-0]}) & \text{?} \ xmm1_{[31-0]} \\
\end{cases}
\]

\[
xmm1_{[63-32]} = xmm1_{[63-32]};
\]

\[
xmm1_{[95-64]} = xmm1_{[95-64]};
\]

\[
xmm1_{[127-96]} = xmm1_{[127-96]};
\]

**Description:** The MINSS instruction returns the minimum SP FP number from the lower SP FP numbers from XMM1 and XMM2/Mem; the upper 3 fields are passed through from xmm1. If the values being compared are both zeros, source2 (xmm2/m128) would be returned. If source2 (xmm2/m128) is an sNaN, this sNaN is forwarded unchanged to the destination (i.e. a quieted version of the sNaN is not returned).

**FP Exceptions:** None

**Numeric Exceptions:** Invalid (including qNaN source operand), Denormal.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

- Same exceptions as in Real Address Mode; #PF (fault-code) for a page fault; #AC for unaligned memory references.
MINSS: Scalar Single-FP Minimum (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments: Note that if only one source is a NaN for these instructions, the Src2 operand (either NaN or real value) is written to the result; this differs from the behavior for other instructions as defined in Table 3-3, which is to always write the NaN to the result, regardless of which source operand contains the NaN. The upper three operands are still bypassed from the src1 operand, as in all other scalar operations. This approach for MINSS allows compilers to use the MINSS instruction for common C conditional constructs. If instead of this behavior, it is required that the NaN source operand be returned, the min/max functionality can be emulated using a sequence of instructions: comparison followed by AND, ANDN and OR.
MOVAPS: Move Aligned Four Packed Single-FP

### Operation

```cpp
if (destination == xmm1) {
    if (source == m128) {
        // load instruction
        xmm1[127-0] = m128;
    }
    else {
        // move instruction
        xmm1[127-0] = xmm2[127-0];
    }
}
else {
    if (destination == m128) {
        // store instruction
        m128 = xmm1[127-0];
    }
    else {
        // move instruction
        xmm2[127-0] = xmm1[127-0];
    }
}
```

### Description:
The linear address corresponds to the address of the least-significant byte of the referenced memory data. When a memory address is indicated, the 16 bytes of data at memory location m128 are loaded or stored. When the register-register form of this operation is used, the content of the 128-bit source register is copied into 128-bit destination register.

### FP Exceptions:
General protection exception if not aligned on 16-byte boundary, regardless of segment.

### Numeric Exceptions:
None
MOVAPS: Move Aligned Four Packed Single-FP (Continued)

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments:

MOVAPS should be used when dealing with 16-byte aligned SP FP numbers. If the data is not known to be aligned, MOVUPS should be used instead of MOVAPS. The usage of this instruction should be limited to the cases where the aligned restriction is easy to meet. Processors that support Streaming SIMD Extension will provide optimal aligned performance for the MOVAPS instruction.

The usage of Repeat Prefixes (F2H, F3H) with MOVAPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with MOVAPS risks incompatibility with future processors.
MOVHLPS: Move High to Low Packed Single-FP

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,12,./r</td>
<td>MOVHLPS xmm1, xmm2</td>
<td>Move 64 bits representing higher two SP operands from XMM2 to lower two fields of XMM1 register.</td>
</tr>
</tbody>
</table>

Operation:  
// move instruction

xmm1[127–64] = xmm1[127–64];
xmm1[63–0] = xmm2[127–64];

Description: The upper 64-bits of the source register xmm2 are loaded into the lower 64-bits of the 128-bit register xmm1 and the upper 64-bits of xmm1 are left unchanged.

FP Exceptions: None

Numeric Exceptions: None

Protected Mode Exceptions:

#UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

#UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1

Comments: The usage of Repeat (F2H, F3H) and Operand Size (66H) prefixes with MOVHLPS is reserved. Different processor implementations may handle these prefixes differently. Usage of these prefixes with MOVHLPS risks incompatibility with future processors.
## MOVHPS: Move High Packed Single-FP

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,16/r</td>
<td>MOVHPS xmm, m64</td>
<td>Move 64 bits representing two SP operands from Mem to upper two fields of XMM register.</td>
</tr>
<tr>
<td>0F,17/r</td>
<td>MOVHPS m64, xmm</td>
<td>Move 64 bits representing two SP operands from upper two fields of XMM register to Mem.</td>
</tr>
</tbody>
</table>

### Operation:

```c
if (destination == xmm) {
    // load instruction
    xmm[127-64] = m64;
    xmm[31-0] = xmm[31-0];
    xmm[63-32] = xmm[63-32];
}
else {
    // store instruction
    m64 = xmm[127-64];
}
```

### Description:
The linear address corresponds to the address of the least-significant byte of the referenced memory data. When the load form of this operation is used, m64 is loaded into the upper 64-bits of the 128-bit register xmm and the lower 64-bits are left unchanged.

### FP Exceptions:
None

### Numeric Exceptions:
None

### Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3);
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

### Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFF; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

### Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #PF (fault-code) for a page fault; #AC for unaligned memory reference if the current privilege level is 3.
MOVHPS: Move High Packed Single-FP (Continued)

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Comments: The usage of Repeat Prefixes (F2H, F3H) with MOVHPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with MOVHPS risks incompatibility with future processors.
MOVLHPS: Move Low to High Packed Single-FP

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,16/r</td>
<td>MOVLHPS xmm1, xmm2</td>
<td>Move 64 bits representing lower two SP operands from XMM2 to upper two fields of XMM1 register.</td>
</tr>
</tbody>
</table>

**Operation:** // move instruction

\[
xmm1[127-64] = xmm2[63-0]; \\
xmm1[63-0] = xmm1[63-0]; 
\]

**Description:** The lower 64-bits of the source register xmm2 are loaded into the upper 64-bits of the 128-bit register xmm1 and the lower 64-bits of xmm1 are left unchanged.

**FP Exceptions:** None

**Numeric Exceptions:** None

**Protected Mode Exceptions:**

- #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1

**Comments:**

The usage of Repeat (F2H, F3H) and Operand Size (66H) prefixes with MOVLHPS is reserved. Different processor implementations may handle these prefixes differently. Usage of these prefixes with MOVLHPS risks incompatibility with future processors.

Example: The usage of Repeat (F2H, F3H) and Operand Size (66H) prefixes with MOVLHPS is reserved. Different processor implementations may handle these prefixes differently. Usage of these prefixes with MOVLHPS risks incompatibility with future processors.
MOVLPS: Move Low Packed Single-FP

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,12,/r</td>
<td>MOVLPS xmm, m64</td>
<td>Move 64 bits representing two SP operands from Mem to lower two fields of XMM register.</td>
</tr>
<tr>
<td>0F,13,/r</td>
<td>MOVLPS m64, xmm</td>
<td>Move 64 bits representing two SP operands from lower two fields of XMM register to Mem.</td>
</tr>
</tbody>
</table>

Operation:
if (destination == xmm) {
    // load instruction
    xmm[63-0]   = m64;
    xmm[95-64]  = xmm[95-64];
    xmm[127-96] = xmm[127-96];
}
else {
    // store instruction
    m64 = xmm[63-0];
}

Description: The linear address corresponds to the address of the least-significant byte of the referenced memory data. When the load form of this operation is used, m64 is loaded into the lower 64-bits of the 128-bit register xmm and the upper 64-bits are left unchanged.

FP Exceptions: None

Numeric Exceptions: None

Protected Mode Exceptions:

#GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments; #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set.; #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #PF (fault-code) for a page fault; #AC for unaligned memory reference if the current privilege level is 3.
MOVLPS: Move Low Packed Single-FP (Continued)

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Comments: The usage of Repeat Prefixes (F2H, F3H) with MOVLPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with MOVLPS risks incompatibility with future processors.
MOVMSKPS: Move Mask to Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,50,/r</td>
<td>MOVMSKPS r32, xmm</td>
<td>Move the single mask to r32.</td>
</tr>
</tbody>
</table>

**Operation:**

```
r32[1] = xmm[63]; r32[0] = xmm[31];
r32[7-4] = 0x0; r32[15-8] = 0x00;
r32[31-16] = 0x0000;
```

**Description:** The MOVMSKPS instruction returns to the integer register r32 a 4-bit mask formed of the most significant bits of each SP FP number of its operand.

**FP Exceptions:** None

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**

- #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception.
- #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- #UD if CR0.EM = 1; #NM if TS bit in CR0 is set.; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault

**Comments:** The usage of Repeat Prefixes (F2H, F3H) with MOVMSKPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with MOVMSKPS risks incompatibility with future processors.
### MOVSS: Move Scalar Single-FP

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3,0F,10,/r</td>
<td>MOVSS xmm1, xmm2/m32</td>
<td>Move 32 bits representing one scalar SP operand from XMM2/Mem to XMM1 register.</td>
</tr>
<tr>
<td>F3,0F,11,/r</td>
<td>MOVSS xmm2/m32, xmm1</td>
<td>Move 32 bits representing one scalar SP operand from XMM1 register to XMM2/Mem.</td>
</tr>
</tbody>
</table>

**Operation:**

```c
if (destination == xmm1) {
    if (source == m32) {
        // load instruction
        xmm1[31-0] = m32;
        xmm1[63-32] = 0x00000000;
        xmm1[95-64] = 0x00000000;
        xmm1[127-96] = 0x00000000;
    } else {
        // move instruction
        xmm1[31-0] = xmm2[31-0];
        xmm1[63-32] = xmm1[63-32];
        xmm1[95-64] = xmm1[95-64];
        xmm1[127-96] = xmm1[127-96];
    }
} else {
    if (destination == m32) {
        // store instruction
        m32 = xmm1[31-0];
    } else {
        // move instruction
        xmm2[31-0] = xmm1[31-0];
        xmm2[63-32] = xmm2[63-32];
        xmm2[95-64] = xmm2[95-64];
    }
}
```
MOVSS: Move Scalar Single-FP (Continued)

\[
\text{xmm2}[127-96] = \text{xmm2}[127-96];
\]

\}
\}

**Description:** The linear address corresponds to the address of the least-significant byte of the referenced memory data. When a memory address is indicated, the 4 bytes of data at memory location m32 are loaded or stored. When the load form of this operation is used, the 32-bits from memory are copied into the lower 32 bits of the 128-bit register xmm, the 96 most significant bits being cleared.

**FP Exceptions:** None

**Numeric Exceptions:** None

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault
MOVUPS: Move Unaligned Four Packed Single-FP

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,10,/r</td>
<td>MOVUPS xmm1, xmm2/m128</td>
<td>Move 128 bits representing four SP data from XMM2/Mem to XMM1 register.</td>
</tr>
<tr>
<td>0F,11,/r</td>
<td>MOVUPS xmm2/m128, xmm1</td>
<td>Move 128 bits representing four SP data from XMM1 register to XMM2/Mem.</td>
</tr>
</tbody>
</table>

**Operation:**

```c
if (destination == xmm1) {
    if (source == m128) {
        // load instruction
        xmm1[127-0] = m128;
    } else {
        // move instruction
        xmm1[127-0] = xmm2[127-0];
    }
} else {
    if (destination == m128) {
        // store instruction
        m128 = xmm1[127-0];
    } else {
        // move instruction
        xmm2[127-0] = xmm1[127-0];
    }
}
```

**Description:** The linear address corresponds to the address of the least-significant byte of the referenced memory data. When a memory address is indicated, the 16 bytes of data at memory location m128 are loaded to the 128-bit multimedia register xmm or stored from the 128-bit multimedia register xmm. When the register-register form of this operation is used, the content of the 128-bit source register is copied into 128-bit register xmm. No assumption is made about alignment.

**FP Exceptions:** None

**Numeric Exceptions:** None
MOVUPS: Move Unaligned Four Packed Single-FP (Continued)

Protected Mode Exceptions:

#GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
#SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #AC for unaligned memory reference if the current privilege level is 3; #NM if TS bit in CR0 is set.

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Comments: MOVUPS should be used with SP FP numbers when that data is known to be unaligned. The usage of this instruction should be limited to the cases where the aligned restriction is hard or impossible to meet. Streaming SIMD Extension implementations guarantee optimum unaligned support for MOVUPS. Efficient Streaming SIMD Extension applications should mainly rely on MOVAPS, not MOVUPS, when dealing with aligned data.

The usage of Repeat-NE Prefix (F2H) and Operand Size Prefix (66H) with MOVUPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with MOVUPS risks incompatibility with future processors.

A linear address of the 128 bit data access, while executing in 16-bit mode, that overlaps the end of a 16-bit segment is not allowed and is defined as reserved behavior. Different processor implementations may/may not raise a GP fault in this case if the segment limit has been exceeded; additionally, the address that spans the end of the segment may/may not wrap around to the beginning of the segment.
MULPS: Packed Single-FP Multiply

<table>
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<tr>
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<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,59,/r</td>
<td>MULPS xmm1, xmm2/m128</td>
<td>Multiply packed SP FP numbers in XMM2/Mem to XMM1.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\begin{align*}
\text{xmm1}[31-0] & = \text{xmm1}[31-0] \times \text{xmm2/m128}[31-0]; \\
\text{xmm1}[63-32] & = \text{xmm1}[63-32] \times \text{xmm2/m128}[63-32]; \\
\text{xmm1}[95-64] & = \text{xmm1}[95-64] \times \text{xmm2/m128}[95-64]; \\
\text{xmm1}[127-96] & = \text{xmm1}[127-96] \times \text{xmm2/m128}[127-96];
\end{align*}
\]

**Description:** The MULPS instructions multiply the packed SP FP numbers of both their operands.

**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0).

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT = 0).

**Virtual 8086 Mode Exceptions:**

- Same exceptions as in Real Address Mode;
- #PF(fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
MULSS: Scalar Single-FP Multiply

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3,0F,59,/r</td>
<td>MULSS xmm1 xmm2/m32</td>
<td>Multiply the lowest SP FP number in XMM2/Mem to XMM1.</td>
</tr>
</tbody>
</table>

```plaintext
xmm1[31-0] = xmm1[31-0] * xmm2/m32[31-0];
xmm1[63-32] = xmm1[63-32];
xmm1[95-64] = xmm1[95-64];
xmm1[127-96] = xmm1[127-96];
```

Description: The MULSS instructions multiply the lowest SP FP numbers of both their operands; the upper 3 fields are passed through from xmm1.

FP Exceptions: None

Numeric Exceptions: Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0).

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0).

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
ORPS: Bit-wise Logical OR for Single-FP Data

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,56,/r</td>
<td>ORPS xmm1, xmm2/m128</td>
<td>OR 128 bits from XMM2/Mem to XMM1 register.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\text{xmm1}[127-0] \mid= \text{xmm2/m128}[127-0];
\]

**Description:**
The ORPS instructions return a bit-wise logical OR between xmm1 and xmm2/mem.

**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** None

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set.

**Real Address Mode Exceptions:**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

**Comments:**
The usage of Repeat Prefixes (F2H, F3H) with ORPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with ORPS risks incompatibility with future processors.
RCPPS: Packed Single-FP Reciprocal

**Opcode** | **Instruction** | **Description**
--- | --- | ---
0F,53,/r | RCPPS xmm1, xmm2/m128 | Return a packed approximation of the reciprocal of XMM2/Mem.

**Operation:**
- \( \text{xmm1}[31-0] = \text{approx} \left( \frac{1}{\text{xmm2}/\text{m128}[31-0]} \right) \)
- \( \text{xmm1}[63-32] = \text{approx} \left( \frac{1}{\text{xmm2}/\text{m128}[63-32]} \right) \)
- \( \text{xmm1}[95-64] = \text{approx} \left( \frac{1}{\text{xmm2}/\text{m128}[95-64]} \right) \)
- \( \text{xmm1}[127-96] = \text{approx} \left( \frac{1}{\text{xmm2}/\text{m128}[127-96]} \right) \)

**Description:**
RCPPS returns an approximation of the reciprocal of the SP FP numbers from xmm2/m128. The relative error for this approximation is Error, which satisfies:

\[ |\text{Error}| \leq 1.5 \times 2^{-12} \]

**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**
- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set.

**Real Address Mode Exceptions:**
- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set.

**Virtual 8086 Mode Exceptions:**
- Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**
- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Presence Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

**Comments:**
RCPPS is not affected by the rounding control in MXCSR. Denormal inputs are treated as zeros (of the same sign) and tiny results are always flushed to zero, with the sign of the operand.

Results are guaranteed not to be tiny, and therefore not flushed to zero, for input values \( x \) which satisfy

\[ |x| \leq 1.111111111010000000000B \times 2^{125} \]

For input values \( x \) which satisfy
flush-to-zero might or might not occur, depending on the implementation (this interval contains 6144 + 3072 = 9216 single precision floating-point numbers).

Results are guaranteed to be tiny, and therefore flushed to zero, for input values x which satisfy

\[ |x| \leq 1.00000000000110000000000B \times 2^{126} \]

The decimal approximations of the single precision numbers that delimit the three intervals specified above, are as follows:

1.11111111110100000000000B \times 2^{125} \approx 8.5039437 \times 10^{37}

1.11111111110100000000001B \times 2^{125} \approx 8.5039443 \times 10^{37}

1.00000000000110000000000B \times 2^{126} \approx 4.2550872 \times 10^{37}

1.00000000000110000000001B \times 2^{126} \approx 4.2550877 \times 10^{37}

The hexadecimal representations of the single precision numbers that delimit the three intervals specified above, are as follows:

1.11111111110100000000000B \times 2^{125} = 0x7e7fe800

1.11111111110100000000001B \times 2^{125} = 0x7e7fe801

1.00000000000110000000000B \times 2^{126} = 0x7e800c00

1.00000000000110000000001B \times 2^{126} = 0x7e800c01
RCPSS: Scalar Single-FP Reciprocal

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3,0F.53,/r</td>
<td>RCPSS xmm1, xmm2/m32</td>
<td>Return an approximation of the reciprocal of the lower SP FP number in XMM2/Mem.</td>
</tr>
</tbody>
</table>

Operation:

\[ \text{xmm1}[31-0] = \text{approx } (1.0/(\text{xmm2/m32}[31-0])); \]

\[ \text{xmm1}[63-32] = \text{xmm1}[63-32]; \]

\[ \text{xmm1}[95-64] = \text{xmm1}[95-64]; \]

\[ \text{xmm1}[127-96] = \text{xmm1}[127-96]; \]

Description: RCPSS returns an approximation of the reciprocal of the lower SP FP number from xmm2/m32; the upper 3 fields are passed through from xmm1. The relative error for this approximation is Error, which satisfies:

\[ |\text{Error}| \leq 1.5 \times 2^{-12} \]

Numeric Exceptions: None.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EF = 1; #AC for unaligned memory reference if the current privilege level is 3; #NM if TS bit in CR0 is set.

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EF = 1; #NM if TS bit in CR0 is set.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults
- Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault

Comments: RCPSS is not affected by the rounding control in MXCSR. Denormal inputs are treated as zeros (of the same sign) and tiny results are always flushed to zero, with the sign of the operand.

Results are guaranteed not to be tiny, and therefore not flushed to zero, for input values \( x \) which satisfy

\[ |x| \leq 1.1111111111010000000000B \times 2^{125} \]

For input values \( x \) which satisfy
flush-to-zero might or might not occur, depending on the implementation (this interval contains 6144 + 3072 = 9216 single precision floating-point numbers).

Results are guaranteed to be tiny, and therefore flushed to zero, for input values \( x \) which satisfy

\[
| x | <= 1.00000000000110000000000B \times 2^{126}
\]

The decimal approximations of the single precision numbers that delimit the three intervals specified above, are as follows:

\[
1.11111111110100000000000B \times 2^{125} \approx 8.5039437 \times 10^{37}
\]
\[
1.11111111110100000000001B \times 2^{125} \approx 8.5039443 \times 10^{37}
\]
\[
1.00000000000110000000000B \times 2^{126} \approx 4.2550872 \times 10^{37}
\]
\[
1.00000000000110000000001B \times 2^{126} \approx 4.2550877 \times 10^{37}
\]

The hexadecimal representations of the single precision numbers that delimit the three intervals specified above, are as follows:

\[
1.11111111110100000000000B \times 2^{125} = 0x7e7fe800
\]
\[
1.11111111110100000000001B \times 2^{125} = 0x7e7fe801
\]
\[
1.00000000000110000000000B \times 2^{126} = 0x7e8000c0
\]
\[
1.00000000000110000000001B \times 2^{126} = 0x7e8000c1
\]
RSQRTPS: Packed Single-FP Square Root Reciprocal

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,52,/=</td>
<td>RSQRTPS xmm1, xmm2/m128</td>
<td>Return a packed approximation of the square root of the reciprocal of XMM2/Mem.</td>
</tr>
</tbody>
</table>

**Operation:**
- xmm1[31-0] = approx (1.0/sqrt(xmm2/m128[31-0]));
- xmm1[63-32] = approx (1.0/sqrt(xmm2/m128[63-32]));
- xmm1[95-64] = approx (1.0/sqrt(xmm2/m128[95-64]));
- xmm1[127-96] = approx (1.0/sqrt(xmm2/m128[127-96]));

**Description:**
RSQRTPS returns an approximation of the reciprocal of the square root of the SP FP numbers from xmm2/m128. The relative error for this approximation is Error, which satisfies:

\[ |\text{Error}| \leq 1.5 \times 2^{-12} \]

**FP Exceptions:**
General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**
- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0;

**Real Address Mode Exceptions:**
Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**
Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**
- Itanium Reg Faults
- Disabled FP Register Fault if PSR.dfl is 1
- NaN Register Consumption Fault
- Itanium Mem Faults
- VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaN Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

**Comments:**
RSQRTPS is not affected by the rounding control in MXCSR. Denormal inputs are treated as zeros (of the same sign).
RSQRTSS: Scalar Single-FP Square Root Reciprocal

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3,0F,52,/r</td>
<td>RSQRTSS xmm1, xmm2/m32</td>
<td>Return an approximation of the square root of the reciprocal of the lowest SP FP number in XMM2/Mem.</td>
</tr>
</tbody>
</table>

Operation:

\[
\begin{align*}
\text{xmm1}[31-0] & = \text{approx } (1.0/\sqrt{\text{xmm2/m32}[31-0]}); \\
\text{xmm1}[63-32] & = \text{xmm1}[63-32]; \\
\text{xmm1}[95-64] & = \text{xmm1}[95-64]; \\
\text{xmm1}[127-96] & = \text{xmm1}[127-96];
\end{align*}
\]

Description: RSQRTSS returns an approximation of the reciprocal of the square root of the lowest SP FP number from xmm2/m32; the upper 3 fields are passed through from xmm1. The relative error for this approximation is Error, which satisfies:

\[|\text{Error}| \leq 1.5\times2^{-12}\]

Numeric Exceptions: None.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments:

Example: RSQRTSS is not affected by the rounding control in MXCSR. Denormal inputs are treated as zeros (of the same sign).
**SHUFPS: Shuffle Single-FP**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,C6,/r, ib</td>
<td>SHUFPS xmm1, xmm2/m128, imm8</td>
<td>Shuffle Single.</td>
</tr>
</tbody>
</table>

**Operation:**

```c
fp_select  = (imm8 >> 0) & 0x3;
xmm1[31-0]   = (fp_select == 0) ? xmm1[31-0]   :
                              (fp_select == 1) ? xmm1[63-32]  :
                              (fp_select == 2) ? xmm1[95-64]  :
                              xmm1[127-96];

fp_select  = (imm8 >> 2) & 0x3;
xmm1[63-32]  = (fp_select == 0) ? xmm1[31-0]   :
                         (fp_select == 1) ? xmm1[63-32]  :
                         (fp_select == 2) ? xmm1[95-64]  :
                         xmm1[127-96];

fp_select  = (imm8 >> 4) & 0x3;
xmm1[95-64]  = (fp_select == 0) ? xmm2/m128[31-0]   :
                     (fp_select == 1) ? xmm2/m128[63-32]  :
                     (fp_select == 2) ? xmm2/m128[95-64]  :
                     xmm2/m128[127-96];

fp_select  = (imm8 >> 6) & 0x3;
xmm1[127-96] = (fp_select == 0) ? xmm2/m128[31-0]   :
                     (fp_select == 1) ? xmm2/m128[63-32]  :
                     (fp_select == 2) ? xmm2/m128[95-64]  :
                     xmm2/m128[127-96];
```

**Description:**

The SHUFPS instruction is able to shuffle any of the four SP FP numbers from xmm1 to the lower 2 destination fields; the upper 2 destination fields are generated from a shuffle of any of the four SP FP numbers from xmm2/m128. By using the same register for both sources, SHUFPS can return any combination of the four SP FP numbers from this register. Bits 0 and 1 of the immediate field are used to select which of the four input SP FP numbers will be put in the first SP FP number of the result; bits 3 and 2 of the immediate field are used to select which of the four input SP FP will be put in the second SP FP number of the result; etc.
SHUFPS: Shuffle Single-FP (Continued)

Example:

```
X4  X3  X2  X1
 xmm1

Y4  Y3  Y2  Y1
 xmm2/m128

{x4 ... x1}  {x4 ... x1}  {x4 ... x1}  {x4 ... x1}
 xmm1
```

**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** None

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults
- Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults
- VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

**Comments:** The usage of Repeat Prefixes (F2H, F3H) with SHUFPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with SHUFPS risks incompatibility with future processors.
SQRTPS: Packed Single-FP Square Root

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,51,/r</td>
<td>SQRTPS xmm1, xmm2/m128</td>
<td>Square Root of the packed SP FP numbers in XMM2/Mem.</td>
</tr>
</tbody>
</table>

Operation:  
\[
\begin{align*}
xmm1[31-0] &= \sqrt{xmm2/m128[31-0]}; \\
xmm1[63-32] &= \sqrt{xmm2/m128[63-32]}; \\
xmm1[95-64] &= \sqrt{xmm2/m128[95-64]}; \\
xmm1[127-96] &= \sqrt{xmm2/m128[127-96]}; \\
\end{align*}
\]

Description: The SQRTPS instruction returns the square root of the packed SP FP numbers from xmm2/m128.

FP Exceptions: General protection exception if not aligned on 16-byte boundary, regardless of segment.

Numeric Exceptions: Invalid, Precision, Denormal.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaN Page ConsumptionAbort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
**SQRTSS: Scalar Single-FP Square Root**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3.0F.51./r</td>
<td>SQRTSS xmm1, xmm2/m32</td>
<td>Square Root of the lower SP FP number in XMM2/Mem.</td>
</tr>
</tbody>
</table>

**Operation:**

- \( \text{xmm1}[31-0] = \sqrt{\text{xmm2/m32}[31-0]}; \)
- \( \text{xmm1}[63-32] = \text{xmm1}[63-32]; \)
- \( \text{xmm1}[95-64] = \text{xmm1}[95-64]; \)
- \( \text{xmm1}[127-96] = \text{xmm1}[127-96]; \)

**Description:** The SQRTSS instructions return the square root of the lowest SP FP numbers of their operand.

**FP Exceptions:** None

**Numeric Exceptions:** Invalid, Precision, Denormal.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

- Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
STMXCSR: Store Streaming SIMD Extension Control/Status

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F, AE,/3</td>
<td>STMXCSR m32</td>
<td>Store Streaming SIMD Extension control/status word to m32.</td>
</tr>
</tbody>
</table>

**Operation:**

\[ m32 = MXCSR; \]

**Description:**

The MXCSR control/status register is used to enable masked/unmasked exception handling, to set rounding modes, to set flush-to-zero mode, and to view exception status flags. Refer to LDMXCSR for a description of the format of MXCSR. The linear address corresponds to the address of the least-significant byte of the referenced memory data. The reserved bits in the MXCSR are stored as zeroes.

**FP Exceptions:** None.

**Numeric Exceptions:** None

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #UD if CRCR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault. #AC for unaligned memory reference.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults  NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

**Comments:**

The usage of Repeat (F2H, F3H) and Operand Size (66H) prefixes with STMXCSR is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with STMXCSR risks incompatibility with future processors.
SUBPS: Packed Single-FP Subtract

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,5C,/r</td>
<td>SUBPS xmm1 xmm2/m128</td>
<td>Subtract packed SP FP numbers in XMM2/Mem from XMM1.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\begin{align*}
\text{xmm1}[31-0] &= \text{xmm1}[31-0] - \text{xmm2/m128}[31-0]; \\
\text{xmm1}[63-32] &= \text{xmm1}[63-32] - \text{xmm2/m128}[63-32]; \\
\text{xmm1}[95-64] &= \text{xmm1}[95-64] - \text{xmm2/m128}[95-64]; \\
\text{xmm1}[127-96] &= \text{xmm1}[127-96] - \text{xmm2/m128}[127-96];
\end{align*}
\]

**Description:** The SUBPS instruction subtracts the packed SP FP numbers of both their operands.

**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** Overflow, Underflow, Invalid, Precision, Denormal.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault; #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault;

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
SUBSS: Scalar Single-FP Subtract

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F3,0F,5C, /r</td>
<td>SUBSS xmm1, xmm2/m32</td>
<td>Subtract the lower SP FP numbers in XMM2/Mem from XMM1.</td>
</tr>
</tbody>
</table>

Operation:

\[
\begin{align*}
\text{xmm1}[31-0] &= \text{xmm1}[31-0] - \text{xmm2/m32}[31-0]; \\
\text{xmm1}[63-32] &= \text{xmm1}[63-32]; \\
\text{xmm1}[95-64] &= \text{xmm1}[95-64]; \\
\text{xmm1}[127-96] &= \text{xmm1}[127-96];
\end{align*}
\]

Description: The SUBSS instruction subtracts the lower SP FP numbers of both their operands.

FP Exceptions: None.

Numeric Exceptions: Overflow, Underflow, Invalid, Precision, Denormal.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3); #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1); #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0); #UD if CR4.OSFXSR(bit 9) = 0; #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF(fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults  VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
UCOMISS: Unordered Scalar Single-FP Compare and Set EFLAGS

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,2E,/r</td>
<td>UCOMISS xmm1, xmm2/m32</td>
<td>Compare lower SP FP number in XMM1 register with lower SP FP number in XMM2/Mem and set the status flags accordingly.</td>
</tr>
</tbody>
</table>

**Operation:**

```
switch (xmm1[31-0] <> xmm2/m32[31-0]) {
    OF, SF, AF = 000;
    case UNORDERED:     ZF, PF, CF = 111;
    case GREATER_THAN:  ZF, PF, CF = 000;
    case LESS_THAN:     ZF, PF, CF = 001;
    case EQUAL:         ZF, PF, CF = 100;
}
```

**Description:**
The UCOMISS instructions compare the two lowest scalar SP FP numbers and sets the ZF,PF,CF bits in the EFLAGS register as described above. In addition, the OF, SF and AF bits in the EFLAGS register are zeroed out. The unordered predicate is returned if either source operand is a NaN (qNaN or sNaN).

**FP Exceptions:** None.

**Numeric Exceptions:** Invalid (if SNaN operands), Denormal. Integer EFLAGS values will not be updated in the presence of unmasked numeric exceptions.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3);
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0);
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #XM for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =1);
- #UD for an unmasked Streaming SIMD Extension numeric exception (CR4.OSXMMEXCPT =0);
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.
UCOMISS: Unordered Scalar Single-FP Compare and Set EFLAGS
(Continued)

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments:
UCOMISS differs from COMISS in that it signals an invalid numeric exception when a source operand is an sNaN; COMISS signals invalid if a source operand is either a qNaN or an sNaN.

The usage of Repeat (F2H, F3H) and Operand-Size prefixes with UCOMISS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with UCOMISS risks incompatibility with future processors.
UNPCKHPS: Unpack High Packed Single-FP Data

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,15/</td>
<td>UNPCKHPS xmm1, xmm2/m128</td>
<td>Interleaves SP FP numbers from the high halves of XMM1 and XMM2/Mem into XMM1 register.</td>
</tr>
</tbody>
</table>

Operation:

\[
\begin{align*}
\text{xmm1}[31-0] &= \text{xmm1}[95-64]; \\
\text{xmm1}[63-32] &= \text{xmm2/m128}[95-64]; \\
\text{xmm1}[95-64] &= \text{xmm1}[127-96]; \\
\text{xmm1}[127-96] &= \text{xmm2/m128}[127-96];
\end{align*}
\]

Description: The UNPCKHPS instruction performs an interleaved unpack of the high-order data elements of XMM1 and XMM2/Mem. It ignores the lower half of the sources.

Example:

![Diagram of UNPCKHPS operation]

FP Exceptions: General protection exception if not aligned on 16-byte boundary, regardless of segment.

Numeric Exceptions: None

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode;
- #PF(fault-code) for a page fault.
UNPCKHPS: Unpack High Packed Single-FP Data (Continued)

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments:

When unpacking from a memory operand, an implementation may decide to fetch only the appropriate 64 bits. Alignment to 16-byte boundary and normal segment checking will still be enforced.

The usage of Repeat Prefixes (F2H, F3H) with UNPCKHPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with UNPCKHPS risks incompatibility with future processors.
UNPCKLPS: Unpack Low Packed Single-FP Data

**Operation:**

\[
\begin{align*}
\text{xmm1}[31-0] &= \text{xmm1}[31-0]; \\
\text{xmm1}[63-32] &= \text{xmm2/m128}[31-0]; \\
\text{xmm1}[95-64] &= \text{xmm1}[63-32]; \\
\text{xmm1}[127-96] &= \text{xmm2/m128}[63-32];
\end{align*}
\]

**Description:**

The UNPCKLPS instruction performs an interleaved unpack of the low-order data elements of XMM1 and XMM2/Mem. It ignores the upper half part of the sources.

**Example:**

```
X4 X3 X2 X1
\hline
\text{xmm1} \\
\text{xmm2/m128} \\
\text{xmm1}
```

**FP Exceptions:**

General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**

 Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;
#UD if CR0.EM = 1;
#NM if TS bit in CR0 is set;
#UD if CRCR4.OSFXSR(bit 9) = 0;
#UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.
UNPCKLPS: Unpack Low Packed Single-FP Data (Continued)

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults  VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

Comments:

When unpacking from a memory operand, an implementation may decide to fetch only the appropriate 64 bits. Alignment to 16-byte boundary and normal segment checking will still be enforced.

The usage of Repeat Prefixes (F2H, F3H) with UNPCKLPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with UNPCKLPS risks incompatibility with future processors.
**XORPS: Bit-wise Logical Xor for Single-FP Data**

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,57,/r</td>
<td>XORPS xmm1, xmm2/m128</td>
<td>XOR 128 bits from XMM2/Mem to XMM1 register.</td>
</tr>
</tbody>
</table>

**Operation:**
\[
\text{xmm}[127-0] ^= \text{xmm/m128}[127-0];
\]

**Description:**
The XORPS instruction returns a bit-wise logical XOR between XMM1 and XMM2/Mem.

**FP Exceptions:** General protection exception if not aligned on 16-byte boundary, regardless of segment.

**Numeric Exceptions:** None

**Protected Mode Exceptions:**
- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

**Real Address Mode Exceptions:**
Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH;  
#UD if CR0.EM = 1;  
#NM if TS bit in CR0 is set;  
#UD if CRCR4.OSFXSR(bit 9) = 0;  
#UD if CPUID.XMM(EDX bit 25) = 0.

**Virtual 8086 Mode Exceptions:**
Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**
- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

**Comments:**
The usage of Repeat Prefixes (F2H, F3H) with XORPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with XORPS risks incompatibility with future processors.

### 3.13 SIMD Integer Instruction Set Extensions

Additional new SIMD Integer instructions have been added to accelerate the performance of 3D graphics, video decoding and encoding and other applications. These instructions operate on the MMX technology registers and on 64-bit memory operands.
PAVGB/PAVGW: Packed Average

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,E0, /r</td>
<td>PAVGB mm1,mm2/m64</td>
<td>Average with rounding packed unsigned bytes from MM2/Mem to packed bytes in MM1 register.</td>
</tr>
<tr>
<td>0F,E3, /r</td>
<td>PAVGW mm1, mm2/m64</td>
<td>Average with rounding packed unsigned words from MM2/Mem to packed words in MM1 register.</td>
</tr>
</tbody>
</table>

Operation:

```c
if (instruction == PAVGB) {
    x[0] = mm1[7-0] y[0] = mm2/m64[7-0];
    x[1] = mm1[15-8] y[1] = mm2/m64[15-8];
    x[5] = mm1[47-40] y[5] = mm2/m64[47-40];
    x[7] = mm1[63-56] y[7] = mm2/m64[63-56];

    for (i = 0; i < 8; i++) {
        temp[i] = zero_ext(x[i], 8) + zero_ext(y[i], 8);
        res[i] = (temp[i] +1) >> 1;
    }
    mm1[7-0] = res[0];
    ...
    mm1[63-56] = res[7];
}
else if (instruction == PAVGW){
    x[0] = mm1[15-0] y[0] = mm2/m64[15-0];
    x[1] = mm1[31-16] y[1] = mm2/m64[31-16];

    for (i = 0; i < 4; i++) {
```
PAVGB/PAVGW: Packed Average (Continued)

\[
\text{temp}[i] = \text{zero\_ext}(x[i], 16) + \text{zero\_ext}(y[i], 16);
\]
\[
\text{res}[i] = (\text{temp}[i] + 1) >> 1;
\]
}

\[
\text{mm1}[15-0] = \text{res}[0];
\]
...

\[
\text{mm1}[63-48] = \text{res}[3];
\]

Description: The PAVG instructions add the unsigned data elements of the source operand to the unsigned data elements of the destination register, along with a carry-in. The results of the add are then each independently right shifted by one bit position. The high order bits of each element are filled with the carry bits of the corresponding sum.

The destination operand is a MMX technology register. The source operand can either be a MMX technology register or a 64-bit memory operand.

The PAVGB instruction operates on packed unsigned bytes and the PAVGW instruction operates on packed unsigned words.

Numeric Exceptions: None.

Protected Mode Exceptions:

\#GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
\#SS(0) for an illegal address in the SS segment; \#PF(fault-code) for a page fault; \#UD if CR0.EM = 1; \#NM if TS bit in CR0 is set. \#MF if there is a pending FPU exception; \#AC for unaligned memory reference. To enable \#AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFH; \#UD if CR0.EM = 1; \#NM if TS bit in CR0 is set; \#MF if there is a pending FPU exception.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; \#PF(fault-code) for a page fault; \#AC for unaligned memory references (if the current privilege level is 3).

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.df is 1, NaT Register Consumption Fault
Itanium Mem Faults  VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
PEXTRW: Extract Word

Opcode | Instruction | Description
------|-------------|-------------
0F.C5, /r, ib | PEXTRW r32, mm, imm8 | Extract the word pointed to by imm8 from MM and move it to a 32-bit integer register.

Operation:  
\[
\text{sel} = \text{imm8} \& 0x3;
\]
\[
\text{mm\_temp} = (\text{mm} >> (\text{sel} \times 16)) \& 0xffff;
\]
\[
\text{r}[15-0] = \text{mm\_temp}[15-0];
\]
\[
\text{r}[31-16] = 0x0000;
\]

Description: The PEXTRW instruction moves the word in MM selected by the two least significant bits of imm8 to the lower half of a 32-bit integer register.

Numeric Exceptions: None.

Protected Mode Exceptions:

  * #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
  * #SS(0) for an illegal address in the SS segment; #PF(fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #MF if there is a pending FPU exception.

Real Address Mode Exceptions:

  * Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #MF if there is a pending FPU exception.

Virtual 8086 Mode Exceptions:

  * Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

  * Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1
### PINSRW: Insert Word

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,C4,/r,ib</td>
<td>PINSRW mm, r32/m16, imm8</td>
<td>Insert the word from the lower half of r32 or from Mem16 into the position in MM pointed to by imm8 without touching the other words.</td>
</tr>
</tbody>
</table>

**Operation:**

```plaintext
sel = imm8 & 0x3;

mask = (sel == 0)? 0x000000000000ffff :
        (sel == 1)? 0x00000000ffff0000 :
        (sel == 2)? 0x0000ffff00000000 :
            0xffff000000000000;

mm = (mm & ~mask) | ((m16/r32[15-0] << (sel * 16)) & mask);
```

**Description:** The PINSRW instruction loads a word from the lower half of a 32-bit integer register (or from memory) and inserts it in the MM destination register at a position defined by the two least significant bits of the imm8 constant. The insertion is done in such a way that the three other words from the destination register are left untouched.

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #MF if there is a pending FPU exception;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

**Real Address Mode Exceptions:**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #MF if there is a pending FPU exception.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults
- Disabled FP Register Fault if PSR.dfl is 1, NaN Register Consumption Fault
- Itanium Mem Faults
- VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaN Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
PMAXSW: Packed Signed Integer Word Maximum

**Opcode** | **Instruction** | **Description**
---|---|---
0F,EE,/r | PMAXSW mm1, mm2/m64 | Return the maximum words between MM2/Mem and MM1.

**Operation:**

\[
\begin{align*}
\text{mm1}[15-0] &= (\text{mm1}[15-0] > \text{mm2/m64}[15-0]) \ ? \ 
\text{mm1}[15-0] : \text{mm2/m64}[15-0]; \\
\text{mm1}[31-16] &= (\text{mm1}[31-16] > \text{mm2/m64}[31-16]) \ ? \ 
\text{mm1}[31-16] : \text{mm2/m64}[31-16]; \\
\text{mm1}[47-32] &= (\text{mm1}[47-32] > \text{mm2/m64}[47-32]) \ ? \ 
\text{mm1}[47-32] : \text{mm2/m64}[47-32]; \\
\text{mm1}[63-48] &= (\text{mm1}[63-48] > \text{mm2/m64}[63-48]) \ ? \ 
\text{mm1}[63-48] : \text{mm2/m64}[63-48];
\end{align*}
\]

**Description:** The PMAXSW instruction returns the maximum between the four signed words in MM1 and MM2/Mem.

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

**Real Address Mode Exceptions:**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #MF if there is a pending FPU exception.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault; #AC for unaligned memory reference if the current privilege level is 3.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
P MAXUB: Packed Unsigned Integer Byte Maximum

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,DE, /r</td>
<td>P MAXUB mm1, mm2/m64</td>
<td>Return the maximum bytes between MM2/Mem and MM1.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\begin{align*}
    mm1[7-0] &= (mm1[7-0] > mm2/m64[7-0]) \ ? \ mm1[7-0] : mm2/m64[7-0]; \\
    mm1[15-8] &= (mm1[15-8] > mm2/m64[15-8]) \ ? \ mm1[15-8] : mm2/m64[15-8]; \\
    mm1[23-16] &= (mm1[23-16] > mm2/m64[23-16]) \ ? \ mm1[23-16] : mm2/m64[23-16]; \\
    mm1[31-24] &= (mm1[31-24] > mm2/m64[31-24]) \ ? \ mm1[31-24] : mm2/m64[31-24]; \\
    mm1[39-32] &= (mm1[39-32] > mm2/m64[39-32]) \ ? \ mm1[39-32] : mm2/m64[39-32]; \\
    mm1[47-40] &= (mm1[47-40] > mm2/m64[47-40]) \ ? \ mm1[47-40] : mm2/m64[47-40]; \\
    mm1[55-48] &= (mm1[55-48] > mm2/m64[55-48]) \ ? \ mm1[55-48] : mm2/m64[55-48]; \\
    mm1[63-56] &= (mm1[63-56] > mm2/m64[63-56]) \ ? \ mm1[63-56] : mm2/m64[63-56];
\end{align*}
\]

**Description:** The P MAXUB instruction returns the maximum between the eight unsigned words in MM1 and MM2/Mem.

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set. #MF if there is a pending FPU exception.

**Virtual 8086 Mode Exceptions:**

- Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault; #AC for unaligned memory reference if the current privilege level is 3.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults  VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
PMINSW: Packed Signed Integer Word Minimum

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F, EA, /r</td>
<td>PMINSW mm1, mm2/m64</td>
<td>Return the minimum words between MM2/Mem and MM1.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\begin{align*}
\text{mm1}[15-0] & = (\text{mm1}[15-0] < \text{mm2/m64}[15-0]) \ ? \ \text{mm1}[15-0] : \ \text{mm2/m64}[15-0]; \\
\text{mm1}[31-16] & = (\text{mm1}[31-16] < \text{mm2/m64}[31-16]) \ ? \ \text{mm1}[31-16] : \ \text{mm2/m64}[31-16]; \\
\text{mm1}[47-32] & = (\text{mm1}[47-32] < \text{mm2/m64}[47-32]) \ ? \ \text{mm1}[47-32] : \ \text{mm2/m64}[47-32]; \\
\text{mm1}[63-48] & = (\text{mm1}[63-48] < \text{mm2/m64}[63-48]) \ ? \ \text{mm1}[63-48] : \ \text{mm2/m64}[63-48]; \\
\end{align*}
\]

**Description:** The PMINSW instruction returns the minimum between the four signed words in MM1 and MM2/Mem.

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #MF if there is a pending FPU exception

For unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

**Real Address Mode Exceptions:**

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set.
- #MF if there is a pending FPU exception.

**Virtual 8086 Mode Exceptions:**

- Same exceptions as in Real Address Mode;
- #PF(fault-code) for a page fault;
- #AC for unaligned memory reference if the current privilege level is 3.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults
  - Disabled FP Register Fault if PSR.dfl is 1,
  - NaT Register Consumption Fault
- Itanium Mem Faults
  - VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
PMINUB: Packed Unsigned Integer Byte Minimum

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,DA, /r</td>
<td>PMINUB mm1, mm2/m64</td>
<td>Return the minimum bytes between MM2/Mem and MM1.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
\begin{align*}
\text{mm1}[7-0] &= (\text{mm1}[7-0] < \text{mm2/m64}[7-0]) \ ? \ \text{mm1}[7-0] : \ \text{mm2/m64}[7-0]; \\
\text{mm1}[15-8] &= (\text{mm1}[15-8] < \text{mm2/m64}[15-8]) \ ? \ \text{mm1}[15-8] : \ \text{mm2/m64}[15-8]; \\
\text{mm1}[23-16] &= (\text{mm1}[23-16] < \text{mm2/m64}[23-16]) \ ? \ \text{mm1}[23-16] : \ \text{mm2/m64}[23-16]; \\
\text{mm1}[31-24] &= (\text{mm1}[31-24] < \text{mm2/m64}[31-24]) \ ? \ \text{mm1}[31-24] : \ \text{mm2/m64}[31-24]; \\
\text{mm1}[39-32] &= (\text{mm1}[39-32] < \text{mm2/m64}[39-32]) \ ? \ \text{mm1}[39-32] : \ \text{mm2/m64}[39-32]; \\
\text{mm1}[47-40] &= (\text{mm1}[47-40] < \text{mm2/m64}[47-40]) \ ? \ \text{mm1}[47-40] : \ \text{mm2/m64}[47-40]; \\
\text{mm1}[55-48] &= (\text{mm1}[55-48] < \text{mm2/m64}[55-48]) \ ? \ \text{mm1}[55-48] : \ \text{mm2/m64}[55-48]; \\
\text{mm1}[63-56] &= (\text{mm1}[63-56] < \text{mm2/m64}[63-56]) \ ? \ \text{mm1}[63-56] : \ \text{mm2/m64}[63-56];
\end{align*}
\]

**Description:**
The PMINUB instruction returns the minimum between the eight unsigned words in MM1 and MM2/Mem.

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #MF if there is a pending FPU exception;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

**Real Address Mode Exceptions:**

Interruption 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault; #AC for unaligned memory reference if the current privilege level is 3.

**Additional Itanium® System Environment Exceptions**

- Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults  VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault

---

Volume 3: IA-32 Streaming SIMD Extension Instruction Reference
PMOVMSKB: Move Byte Mask To Integer

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,D7,/r</td>
<td>PMOVMSKB r32, mm</td>
<td>Move the byte mask of MM to r32.</td>
</tr>
</tbody>
</table>

**Operation:**

r32[7] = mm[63];  r32[6] = mm[55];
r32[5] = mm[47];  r32[4] = mm[39];
r32[3] = mm[31];  r32[2] = mm[23];
r32[1] = mm[15];  r32[0] = mm[7];
r32[31–8] = 0x000000;

**Description:** The PMOVMSKB instruction returns a 8-bit mask formed of the most significant bits of each byte of its source operand.

**Numeric Exceptions:** None.

**Protected Mode Exceptions:**

#GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
#SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

**Real Address Mode Exceptions:**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception.

**Virtual 8086 Mode Exceptions:**

Same exceptions as in Real Address Mode; #PF (fault-code) for a page fault; #AC for unaligned memory reference if the current privilege level is 3.

**Additional Itanium® System Environment Exceptions**

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1
PMULHUW: Packed Multiply High Unsigned

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,E4,/r</td>
<td>PMULHUW mm1, mm2/m64</td>
<td>Multiply the packed unsigned words in MM1 register with the packed unsigned words in MM2/Mem, then store the high-order 16 bits of the results in MM1.</td>
</tr>
</tbody>
</table>

Operation:

\[
\begin{align*}
  \text{mm1}[15-0] &= (\text{mm1}[15-0] \times \text{mm2/m64}[15-0])_{31-16}; \\
  \text{mm1}[31-16] &= (\text{mm1}[31-16] \times \text{mm2/m64}[31-16])_{31-16}; \\
  \text{mm1}[47-32] &= (\text{mm1}[47-32] \times \text{mm2/m64}[47-32])_{31-16}; \\
  \text{mm1}[63-48] &= (\text{mm1}[63-48] \times \text{mm2/m64}[63-48])_{31-16};
\end{align*}
\]

Description: The PMULHUW instruction multiplies the four unsigned words in the destination operand with the four unsigned words in the source operand. The high-order 16 bits of the 32-bit intermediate results are written to the destination operand.

Numeric Exceptions: None.

Protected Mode Exceptions

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #MF if there is a pending FPU exception;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

Real Address Mode Exceptions

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception.

Virtual 8086 Mode Exceptions

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault; #AC for unaligned memory reference if the current privilege level is 3.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
PSADBW: Packed Sum of Absolute Differences

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F, F6, /r</td>
<td>PSADBW mm1,mm2/m64</td>
<td>Absolute difference of packed unsigned bytes from MM2/Mem and MM1; these differences are then summed to produce a word result.</td>
</tr>
</tbody>
</table>

**Operation:**

\[
temp1 = \text{ABS}(\text{mm1}[7-0] - \text{mm2/m64}[7-0]); \\
temp2 = \text{ABS}(\text{mm1}[15-8] - \text{mm2/m64}[15-8]); \\
temp3 = \text{ABS}(\text{mm1}[23-16] - \text{mm2/m64}[23-16]); \\
temp4 = \text{ABS}(\text{mm1}[31-24] - \text{mm2/m64}[31-24]); \\
temp5 = \text{ABS}(\text{mm1}[39-32] - \text{mm2/m64}[39-32]); \\
temp6 = \text{ABS}(\text{mm1}[47-40] - \text{mm2/m64}[47-40]); \\
temp7 = \text{ABS}(\text{mm1}[55-48] - \text{mm2/m64}[55-48]); \\
temp8 = \text{ABS}(\text{mm1}[63-56] - \text{mm2/m64}[63-56]); \\
\]

\[
\text{mm1}[15:0] = temp1 + temp2 + temp3 + temp4 + temp5 + temp6 + temp7 + temp8; \\
\text{mm1}[31:16] = 0x00000000; \\
\text{mm1}[47:32] = 0x00000000; \\
\text{mm1}[63:48] = 0x00000000; \\
\]

**Description:**
The PSADBW instruction computes the absolute value of the difference of unsigned bytes for mm1 and mm2/m64. These differences are then summed to produce a word result in the lower 16-bit field; the upper 3 words are cleared.

The destination operand is a MMX technology register. The source operand can either be a MMX technology register or a 64-bit memory operand.

**Numeric Exceptions:** None

**Protected Mode Exceptions**

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

**Real Address Mode Exceptions**

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception.
PSADBW: Packed Sum of Absolute Differences (Continued)

Virtual 8086 Mode Exceptions

Same exceptions as in Real Address Mode; #PF(fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not
Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data
Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
PSHUFW: Packed Shuffle Word

Opcode: 0F,70,/r,ib

Instruction: PSHUFW mm1, mm2/m64, imm8

Description: Shuffle the words in MM2/Mem based on the encoding in imm8 and store in MM1.

Operation:

\[ mm1[15-0] = (mm2/m64 >> (imm8[1-0] * 16)) [15-0] \]
\[ mm1[31-16] = (mm2/m64 >> (imm8[3-2] * 16)) [15-0] \]
\[ mm1[47-32] = (mm2/m64 >> (imm8[5-4] * 16)) [15-0] \]
\[ mm1[63-48] = (mm2/m64 >> (imm8[7-6] * 16)) [15-0] \]

Description: The PSHUF instruction uses the imm8 operand to select which of the four words in MM2/Mem will be placed in each of the words in MM1. Bits 1 and 0 of imm8 encode the source for destination word 0 (MM1[15-0]), bits 3 and 2 encode for word 1, bits 5 and 4 encode for word 2, and bits 7 and 6 encode for word 3 (MM1[63-48]). Similarly, the two bit encoding represents which source word is to be used, e.g. an binary encoding of 10 indicates that source word 2 (MM2/Mem[47-32]) will be used.

Numeric Exceptions: None.

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF (fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #MF if there is a pending FPU exception;
- #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true (CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #MF if there is a pending FPU exception.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode;
- #PF(fault-code) for a page fault;
- #AC for unaligned memory reference if the current privilege level is 3.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults: Disabled FP Register Fault if PSR.df1 is 1, NaT Register Consumption Fault
- Itanium Mem Faults: VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault
This section describes the cacheability control instructions which enable an application writer to minimize data access latency and cache pollution.
MASKMOVQ: Byte Mask Write

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,F7,r</td>
<td>MASKMOVQ mm1, mm2</td>
<td>Move 64-bits representing integer data from MM1 register to memory location specified by the edi register, using the byte mask in MM2 register.</td>
</tr>
</tbody>
</table>

Operation: if (mm2[7])  m64[edi]    = mm1[7-0];
           if (mm2[15]) m64[edi+1]  = mm1[15-8];
           if (mm2[23]) m64[edi+2]  = mm1[23-16];
           if (mm2[31]) m64[edi+3]  = mm1[31-24];
           if (mm2[39]) m64[edi+4]  = mm1[39-32];
           if (mm2[47]) m64[edi+5]  = mm1[47-40];
           if (mm2[55]) m64[edi+6]  = mm1[55-48];
           if (mm2[63]) m64[edi+7]  = mm1[63-56];

Description: Data is stored from the mm1 register to the location specified by the di/edi register (using DS segment). The size of the store address depends on the address-size attribute. The most significant bit in each byte of the mask register mm2 is used to selectively write the data (0 = no write, 1 = write), on a per-byte basis. Behavior with a mask of all zeroes is as follows:

- No data will be written to memory. However, transition from FP to MMX technology state (if necessary) will occur, irrespective of the value of the mask.
- For memory references, a zero byte mask does not prevent addressing faults (i.e. #GP, #SS) from being signalled.
- Signalling of page faults (#PF) is implementation-specific.
- #UD, #NM, #MF, and #AC faults are signalled irrespective of the value of the mask.
- Signalling of breakpoints (code or data) is not guaranteed; different processor implementations may signal or not signal these breakpoints.
- If the destination memory region is mapped as UC or WP, enforcement of associated semantics for these memory types is not guaranteed (i.e. is reserved) and is implementation-specific. Dependency on the behavior of a specific implementation in this case is not recommended, and may lead to future incompatibility.

The Mod field of the ModR/M byte must be 11, or an Invalid Opcode Exception will result.

Numeric Exceptions: None

Protected Mode Exceptions:

#GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
#SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EF
= 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception; #AC for unaligned
memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set;
EFLAGS.AC is set; current CPL is 3).
MASKMOVQ: Byte Mask Write (Continued)

Real Address Mode Exceptions:

Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception.

Virtual 8086 Mode Exceptions:

Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

Itanium Reg Faults  Disabled FP Register Fault if PSR.dfl is 1

Comments: MASKMOVQ can be used to improve performance for algorithms which need to merge data on a byte granularity. MASKMOVQ should not cause a read for ownership; doing so generates unnecessary bandwidth since data is to be written directly using the byte-mask without allocating old data prior to the store. Similar to the Streaming SIMD Extension non-temporal store instructions, MASKMOVQ minimizes pollution of the cache hierarchy. MASKMOVQ implicitly uses weakly-ordered, write-combining stores (WC). See Section 3.6.1.9 for further information about non-temporal stores.

As a consequence of the resulting weakly-ordered memory consistency model, a fencing operation such as SFENCE should be used if multiple processors may use different memory types to read/write the same memory location specified by edi.

This instruction behaves identically to MMX instructions, in the presence of x87-FP instructions: transition from x87-FP to MMX technology (TOS=0, FP valid bits set to all valid).

MASKMOVQ ignores the value of CR4.OSFXSR. Since it does not affect the new Streaming SIMD Extension state, they will not generate an invalid exception if CR4.OSFXSR = 0.
MOVNTPS: Move Aligned Four Packed Single-FP Non-temporal

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,2B, /r</td>
<td>MOVNTPS m128, xmm</td>
<td>Move 128 bits representing four packed SP FP data from XMM register to Mem, minimizing pollution in the cache hierarchy.</td>
</tr>
</tbody>
</table>

Operation: \( m_{128} = \text{xmm}; \)

Description: The linear address corresponds to the address of the least-significant byte of the referenced memory data. This store instruction minimizes cache pollution.

FP Exceptions: General protection exception if not aligned on 16-byte boundary, regardless of segment.

Numeric Exceptions: None

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment;
- #PF(fault-code) for a page fault;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFFH;
- #UD if CR0.EM = 1;
- #NM if TS bit in CR0 is set;
- #UD if CRCR4.OSFXSR(bit 9) = 0;
- #UD if CPUID.XMM(EDX bit 25) = 0.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode;
- #PF(fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults
  - Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults
  - VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Comments: MOVNTPS should be used when dealing with 16-byte aligned single-precision FP numbers. MOVNTPS minimizes pollution in the cache hierarchy. As a consequence of the resulting weakly-ordered memory consistency model, a fencing operation should be used if multiple processors may use different memory types to read/write the memory location. See Section 3.6.1.9 for further information about non-temporal stores.

The usage of Repeat Prefixes(F2H, F3H) with MOVNTPS is reserved. Different processor implementations may handle this prefix differently. Usage of this prefix with MOVNTPS risks incompatibility with future processors.
MOVNTQ: Move 64 Bits Non-temporal

<table>
<thead>
<tr>
<th>Opcode</th>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0F,E7,\r</td>
<td>MOVNTQ m64, mm</td>
<td>Move 64 bits representing integer operands (8b, 16b, 32b) from MM register to memory, minimizing pollution within cache hierarchy.</td>
</tr>
</tbody>
</table>

Operation: \m64 = mm;

Description: The linear address corresponds to the address of the least-significant byte of the referenced memory data. This store instruction minimizes cache pollution.

Numeric Exceptions: None

Protected Mode Exceptions:

- #GP(0) for an illegal memory operand effective address in the CS, DS, ES, FS or GS segments;
- #SS(0) for an illegal address in the SS segment; #PF (fault-code) for a page fault; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception; #AC for unaligned memory reference. To enable #AC exceptions, three conditions must be true(CR0.AM is set; EFLAGS.AC is set; current CPL is 3).

Real Address Mode Exceptions:

- Interrupt 13 if any part of the operand would lie outside of the effective address space from 0 to 0FFFFH; #UD if CR0.EM = 1; #NM if TS bit in CR0 is set; #MF if there is a pending FPU exception.

Virtual 8086 Mode Exceptions:

- Same exceptions as in Real Address Mode; #AC for unaligned memory reference if the current privilege level is 3; #PF (fault-code) for a page fault.

Additional Itanium® System Environment Exceptions

- Itanium Reg Faults Disabled FP Register Fault if PSR.dfl is 1, NaT Register Consumption Fault
- Itanium Mem Faults VHPT Data Fault, Data TLB Fault, Alternate Data TLB Fault, Data Page Not Present Fault, Data NaT Page Consumption Abort, Data Key Miss Fault, Data Key Permission Fault, Data Access Rights Fault, Data Access Bit Fault, Data Dirty Bit Fault

Comments: MOVNTQ minimizes pollution in the cache hierarchy. As a consequence of the resulting weakly-ordered memory consistency model, a fencing operation should be used if multiple processors may use different memory types to read/write the memory location. See Section 3.6.1.9 for further information about non-temporal stores.

MOVNTQ ignores the value of CR4.OSFXSR. Since it does not affect the new Streaming SIMD Extension state, they will not generate an invalid exception if CR4.OSFXSR = 0.
PREFETCH: Prefetch

If there are no excepting conditions, the prefetch instruction fetches the line containing the addresses byte to a location in the cache hierarchy specified by a locality hint. If the line is already present in the cache hierarchy at a level closer to the processor, no data movement occurs. The bits 5:3 of the ModR/M byte specify locality hints as follows:

- Temporal data (t0) - prefetch data into all cache levels.
- Temporal with respect to first level cache (t1) – prefetch data in all cache levels except 0th cache level.
- Temporal with respect to second level cache (t2) – prefetch data in all cache levels, except 0th and 1st cache levels.
- Non-temporal with respect to all cache levels (nta) – prefetch data into non-temporal cache structure.

Locality hints do not affect the functional behavior of the program. They are implementation dependent, and can be overloaded or ignored by an implementation. The prefetch instruction does not cause any exceptions (except for code breakpoints), does not affect program behavior and may be ignored by the implementation. The amount of data prefetched is implementation dependent. It will however be a minimum of 32 bytes. Prefetches to uncacheable memory (UC or WC memory types) will be ignored. Additional ModRM encodings, besides those specified above, are defined to be reserved and the use of reserved encodings risks future incompatibility.

Numeric Exceptions: None

Protected Mode Exceptions: None

Real Address Mode Exceptions: None

Virtual 8086 Mode Exceptions: None

Additional Itanium® System Environment Exceptions: None

Comments: This instruction is merely a hint. If executed, this instruction moves data closer to the processor in anticipation of future use. The performance of these instructions in application code can be implementation specific. To achieve maximum speedup, code tuning might be necessary for each implementation. The non-temporal hint also minimizes pollution of useful cache data.

PREFETCH instructions ignore the value of CR4.OSFXSR. Since they do not affect the new Streaming SIMD Extension state, they will not generate an invalid exception if CR4.OSFXSR = 0.
SFENCE: Store Fence

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<td>0F AE /7</td>
<td>SFENCE</td>
<td>Guarantees that every store instruction that precedes in program order the store fence instruction is globally visible before any store instruction which follows the fence is globally visible.</td>
</tr>
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Operation: while (!(preceding_stores_globally_visible)) wait();

Description: Weakly ordered memory types can enable higher performance through such techniques as out-of-order issue, write-combining, and write-collapsing. Memory ordering issues can arise between a producer and a consumer of data and there are a number of common usage models which may be affected by weakly ordered stores: (1) library functions, which use weakly ordered memory to write results (2) compiler-generated code, which also benefit from writing weakly-ordered results, and (3) hand-written code. The degree to which a consumer of data knows that the data is weakly ordered can vary for these cases. As a result, the SFENCE instruction provides a performance-efficient way of ensuring ordering between routines that produce weakly-ordered results and routines that consume this data.

SFENCE uses the following ModRM encoding:

Mod (7:6) = 11B
Reg/Opcode (5:3) = 111B
R/M (2:0) = 000B

All other ModRM encodings are defined to be reserved, and use of these encodings risks incompatibility with future processors.

Numeric Exceptions: None

Protected Mode Exceptions: None

Real Address Mode Exceptions: None

Virtual 8086 Mode Exceptions: None

Additional Itanium® System Environment Exceptions: None

Comments: SFENCE ignores the value of CR4.OSFXSR. SFENCE will not generate an invalid exception if CR4.OSFXSR = 0
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